SOIピクセル検出器とその応用

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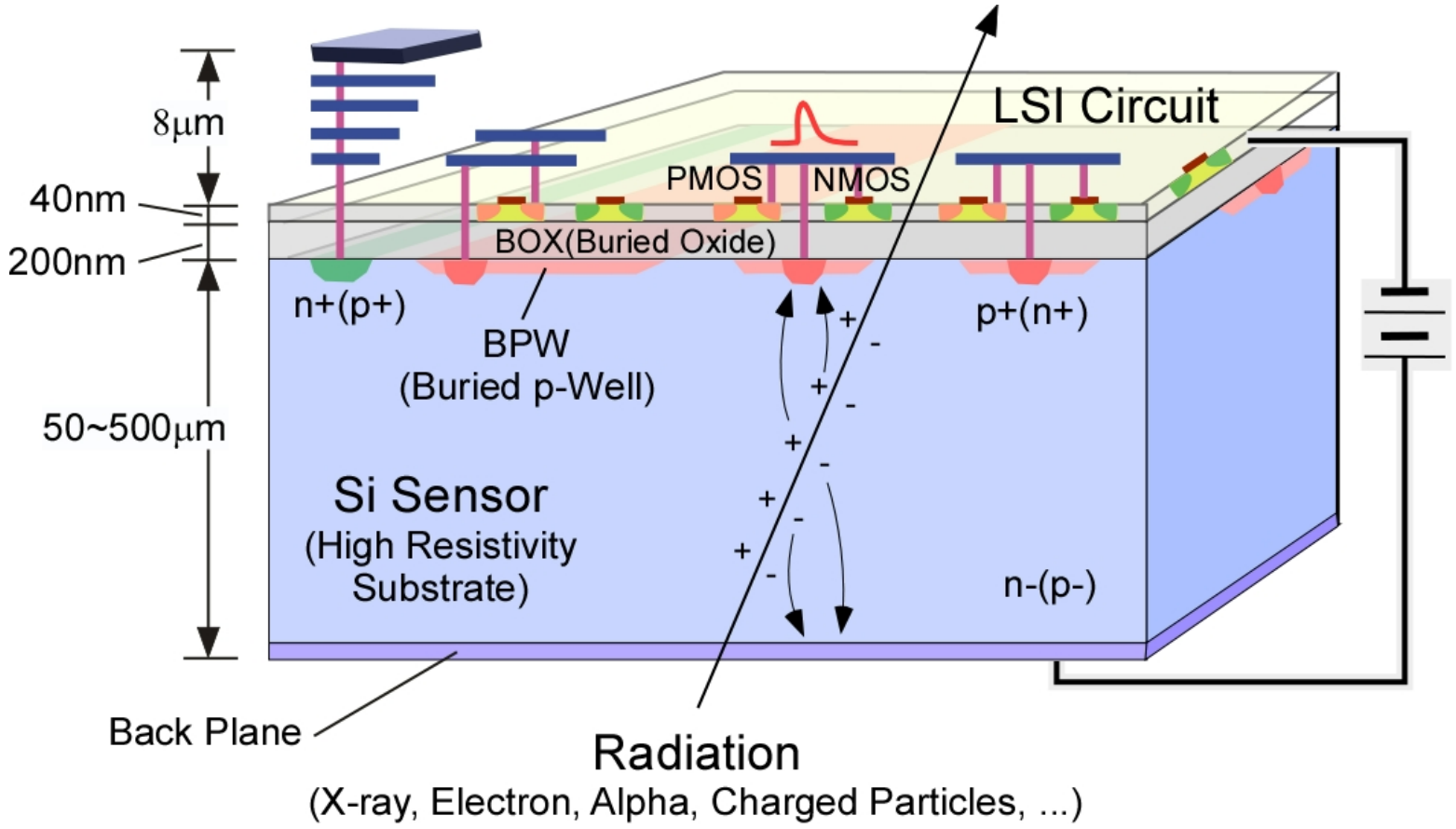
http://rd.kek.jp/project/soi/

I. Introduction

Silicon-On-Insulator Pixel Detector (SOIPIX)



Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.

Outline

I. Introduction

II. Recent Progress

***Layout Shrinking with NMOS-PMOS merge**

***Double SOI Wafer & Process**

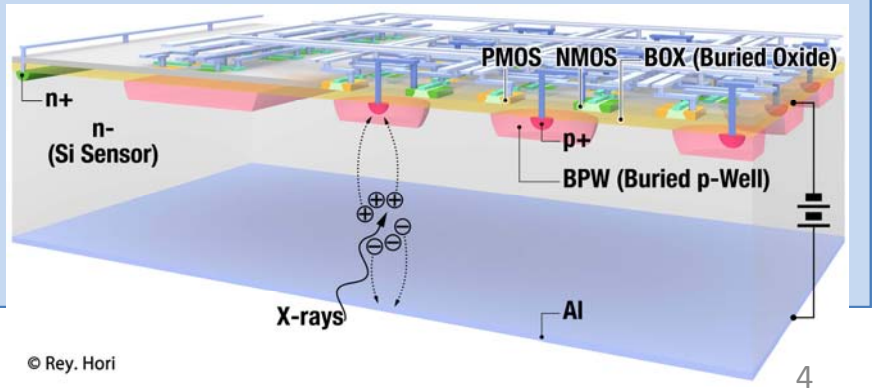
***Higher Dose LDD**

***Compensation with Tunneling**

III. Summary

SOI Pixel検出器の特徴

- 機械的接合がなく、半導体微細加工のみで製造。
  高信頼性、高分解能、低価格が望める。
- 超薄型センサ(~50μm)による、多重散乱を防ぐ荷電粒子検出。
  厚い空乏層(~500μm)による、X線・赤外線への高い感度。
- 高度信号処理回路やメモリーを持つインテリジェント・ピクセル
  が可能に。
- 過酷な環境（極低温、放射線）への強い耐性。
- 基本は産業界の標準技術。
  （技術発展の取り込みが容易）
  日本発の最先端技術。

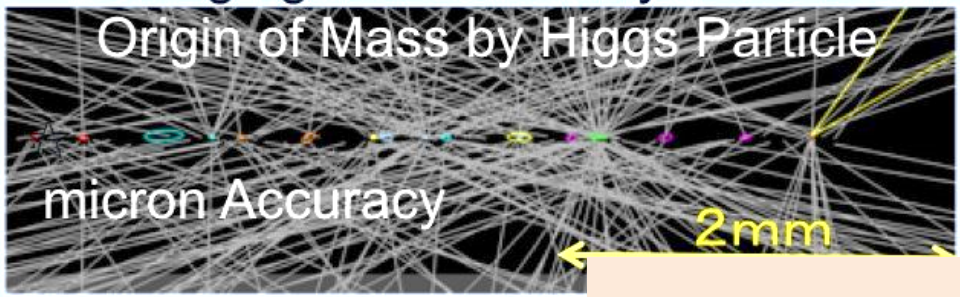


Lapis (*) Semiconductor 0.2 μm FD-SOI Pixel Process

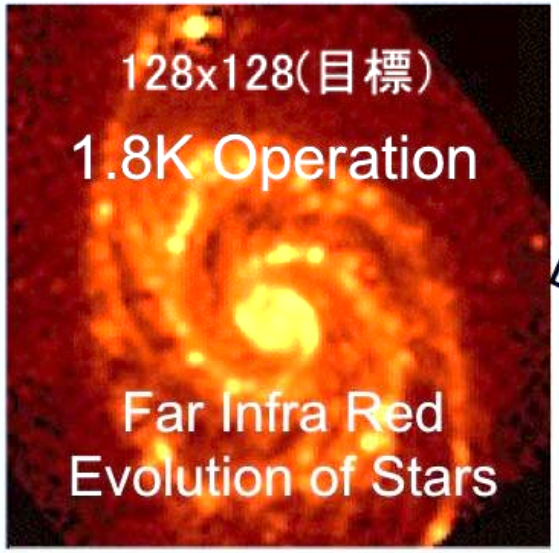
Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) ~7k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

(*) Former OKI Semiconductor Co. Ltd.

SOI Pixel Collaboration



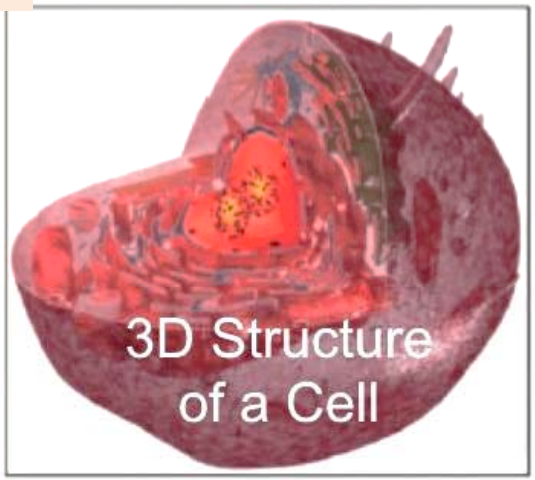
Imaging Mass Spectrometer Rapid Analysis



Superior Resolution

Harsh Environment

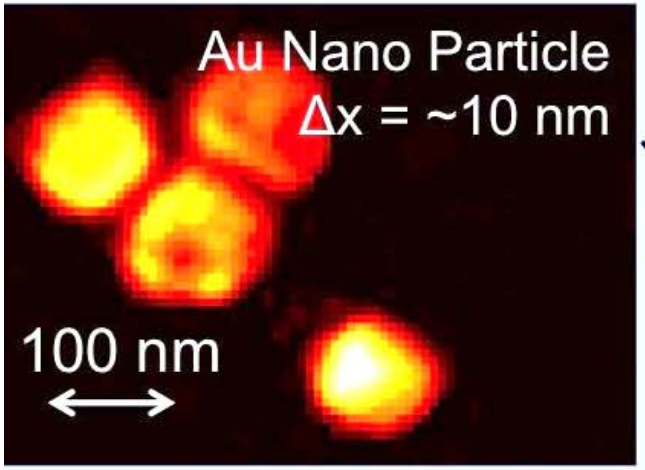
X-ray Imaging Synchrotron Radiation



SOI

High Intensity

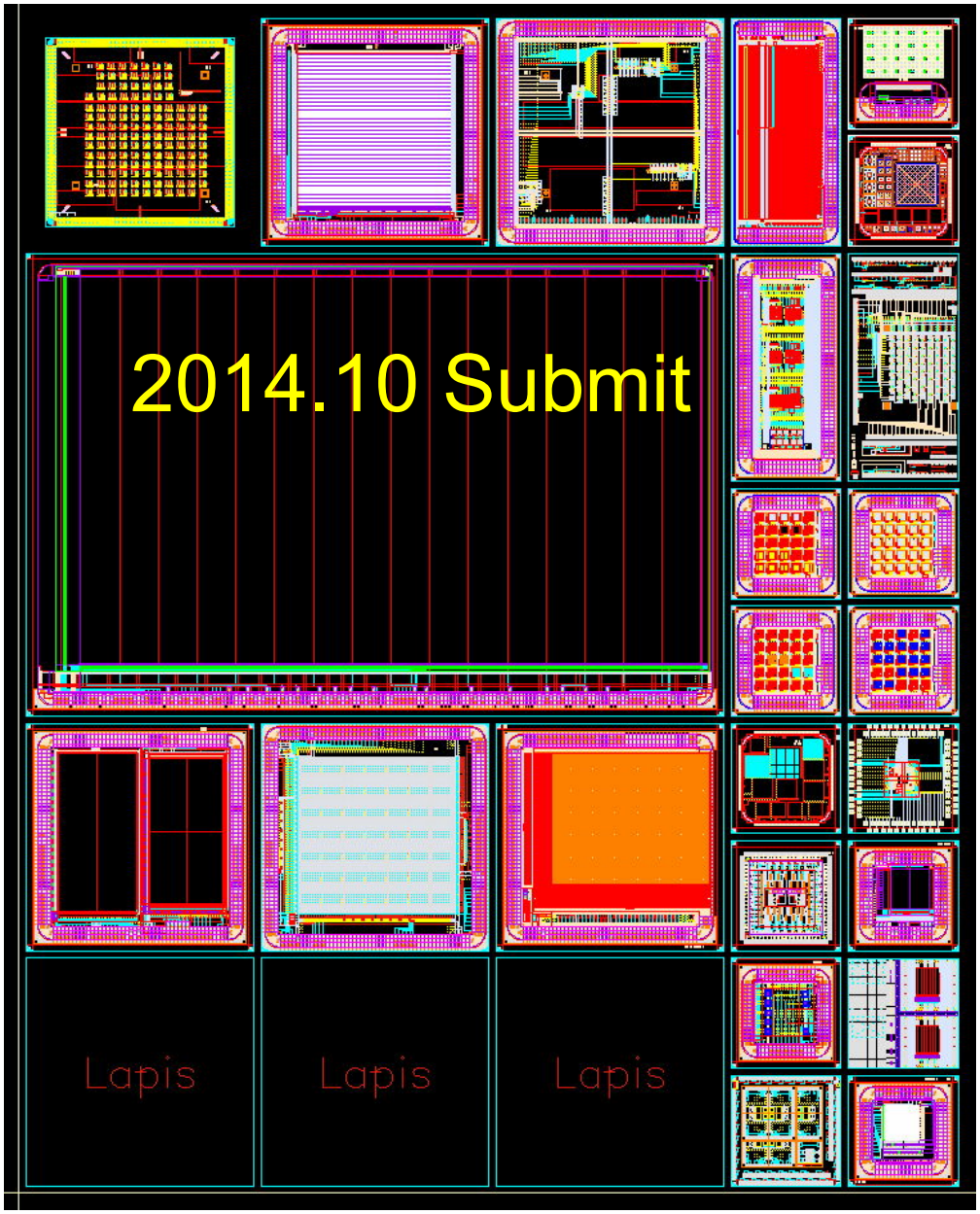
Precise Time Resolution

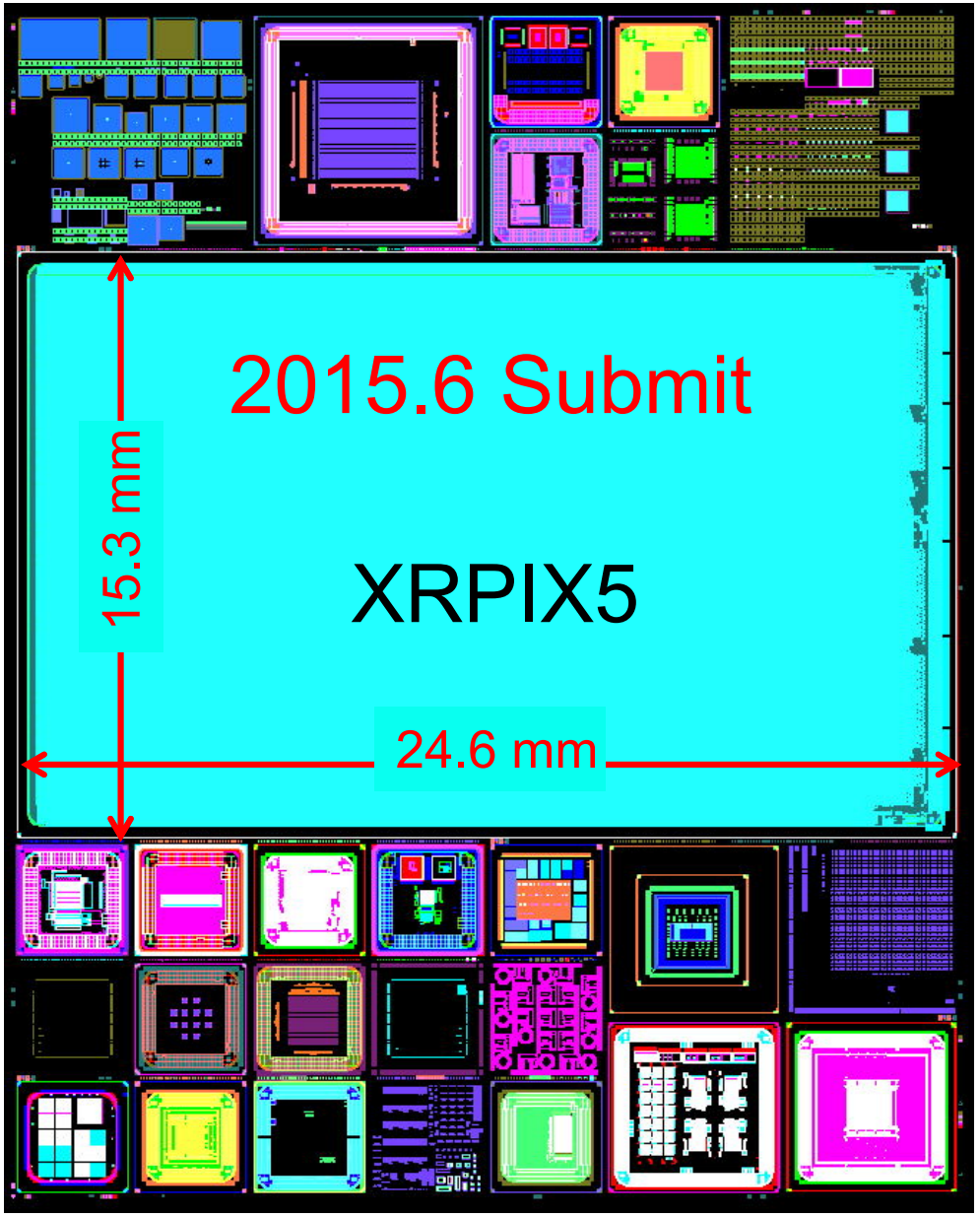


XFEL
femto Second
1nm Resolution

Exploration of Primitive Black Holes

Multi-Project Wafer (MPW) run.
(1~2 runs/year)





~25 Designes/Mask

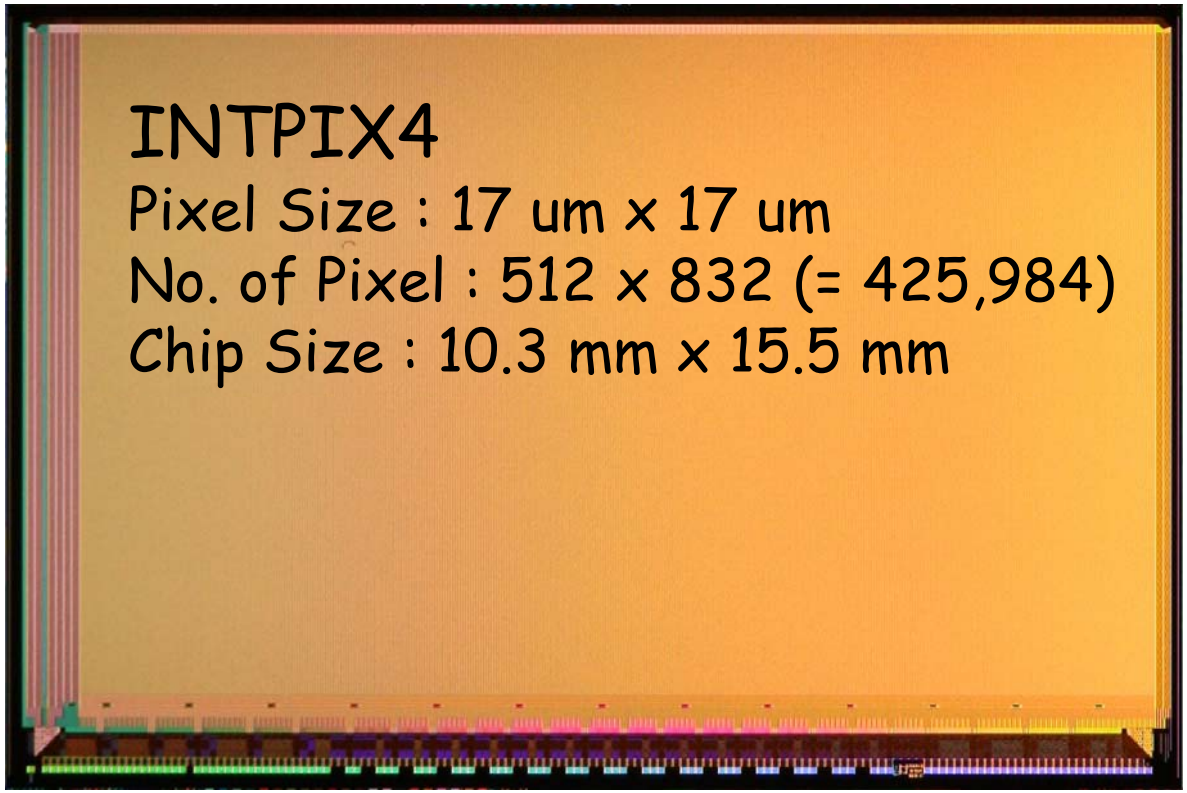
新学術領域研究(FY2013~2017)計画研究

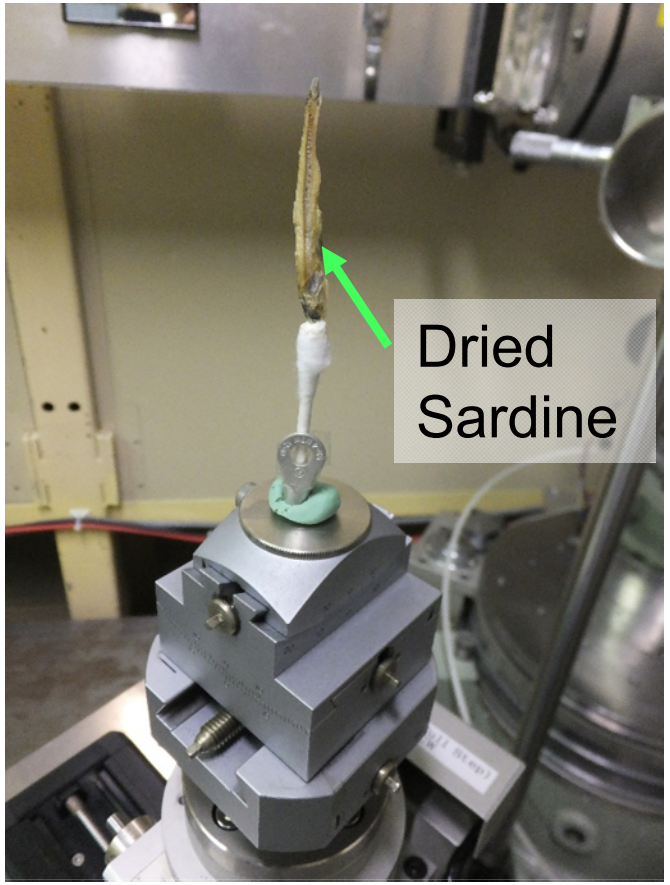
研究班	研究代表	研究課題名
A01	新井康夫 （KEK素核研）	SOI 3次元ピクセルプロセスの研究
A02	川人祥二 （静岡大）	SOI技術を用いた極低ノイズ・高速イメージングデバイスの研究
B01	鶴剛 （京大）	宇宙最初期ブラックホールの探査研究を実現する衛星搭載X線精密イメージングの開拓
B02	和田武彦 （宇宙科学研）	ダストに隠された宇宙の物質進化を暴く 極低温SOI赤外線イメージングの開拓
C01	坪山透 （KEK）	高輝度加速器実験のための素粒子イメージング
C02	初井宇記 （理研）	X線自由電子レーザーによる超高速ナノ構造解析用検出器
D01	岸本俊二 （KEK物構研）	放射光を用いた空間階層構造とダイナミクス研究のためのイメージング
D02	粟津邦男 （阪大）	投影型イメージング質量分析による迅速で高解像度な生体内分子イメージング

公募研究(FY2014~2015)

タイトル	研究代表	所属
PSS－SOI高分解能検出器の開発および応用	島添　健次	東京大学
ワイドレンジプラズモンフィルタを実装したSOI量子イメージセンサの開発	小野　篤史	静岡大学
軟X線用の背面反射回折環二次元イメージング機構の開発	佐々木　敏彦	金沢大
究極のエネルギー分解能を持つ大面積X線検出器の開発	石野　宏和	岡山大学
XRPIXの位置分解能向上とG2格子不要のX線タルボ干渉計の開発	林田　清	大阪大学
中性子星の磁場構造を解き明かすX線偏光イメージャーの開発研究	平賀　純子	東京大学
SOI技術を用いたイメージセンサの重粒子線への応用	松村　彰彦	群馬大学

3D Tomographi with Syncrotron X-ray





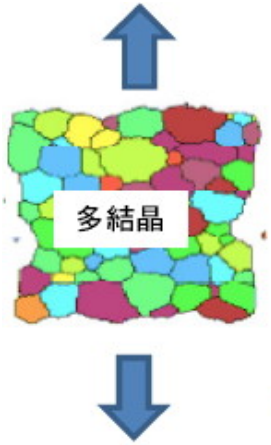
- Sensor : INTPIX4 FZn, Backside Illumination
- HV : 200V、Integration Time : 1ms、ScanTime : 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy : 9.5keV
- Took images for 0~180° at every 1 degree.

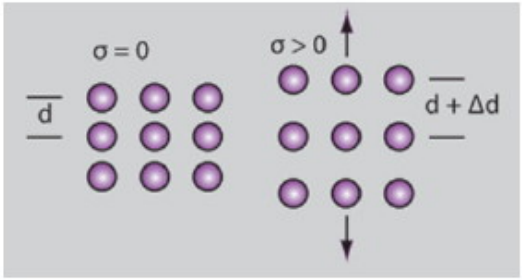
(by R. Nishimura, K. Hirano (KEK)

INTPIX4: Computed Tomography with Syncrotron X-ray

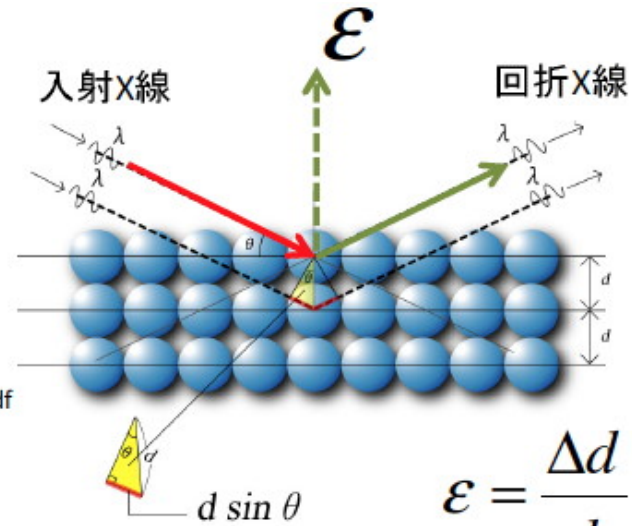
(by R. Nishimura, K. Hirano (KEK)

X線回折による金属の歪み測定





http://www.protoxrd.com/assets/automotive.pdf

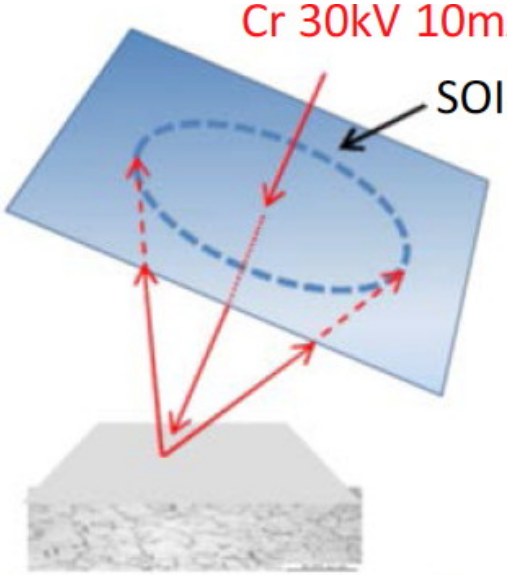


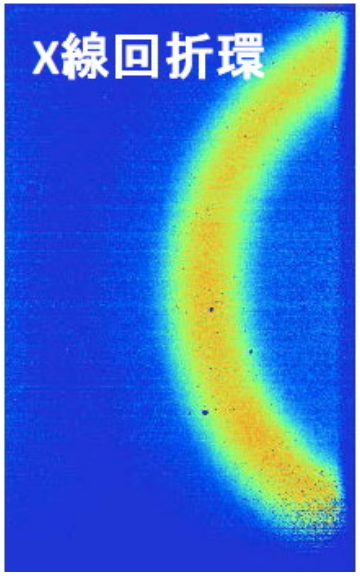
Braggの条件

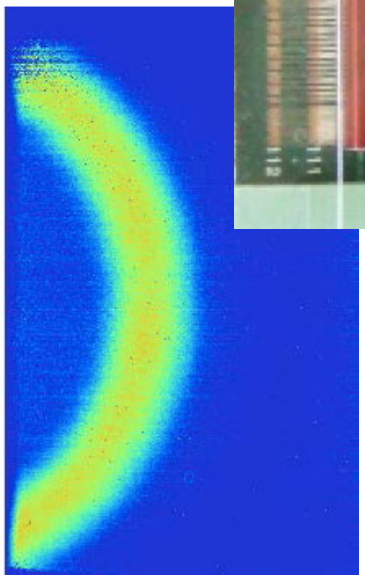
$$2d\sin\theta = n\lambda$$

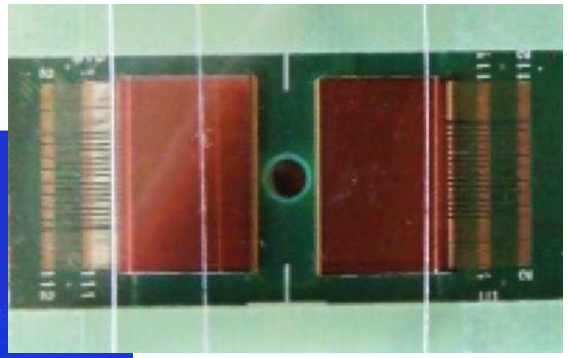
d ： 格子面間隔（未知数）
θ ： Bragg角 （測定値）
λ ： X線の波長（既知数）
n ： 回折次数 （n=1）

$$\varepsilon = \frac{\Delta d}{d} = -\Delta\theta \cdot \cot\theta$$









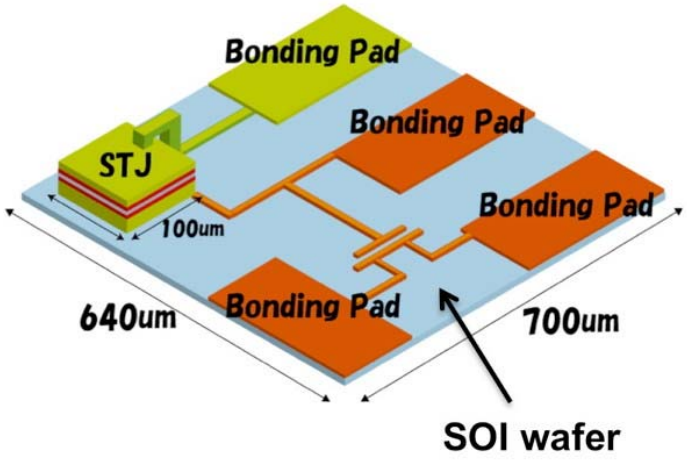
(協力：金沢大
佐々木敏彦 教授

STJ (Superconducting Tunnel Junction) on SOI

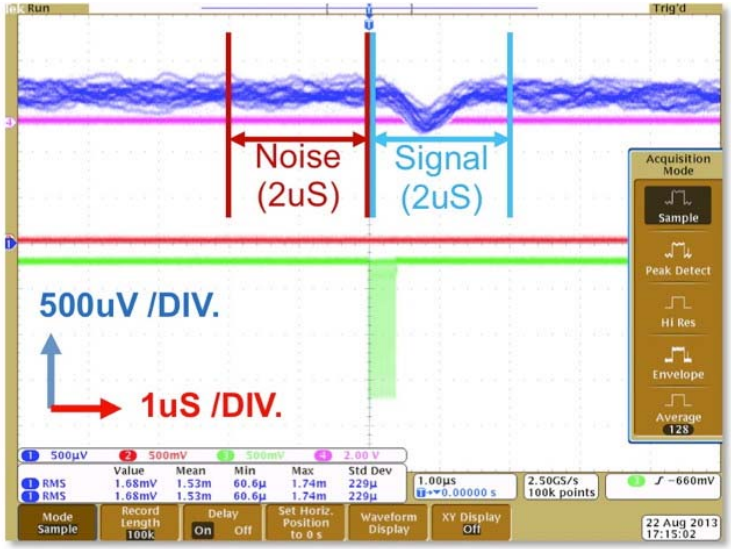
筑波大、KEK,、産総研(CRAVITY)、TIA

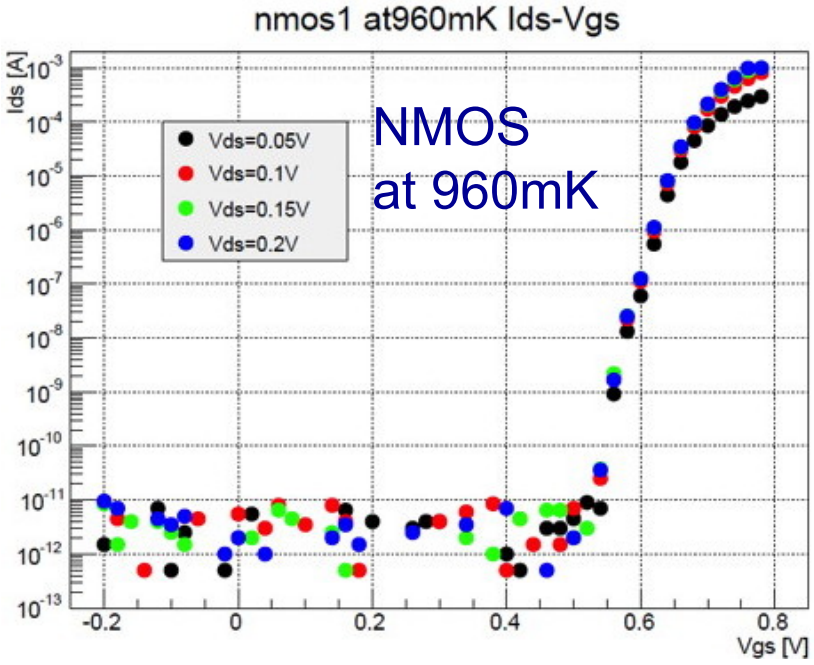
SOI transistors work at temperature below 1K.

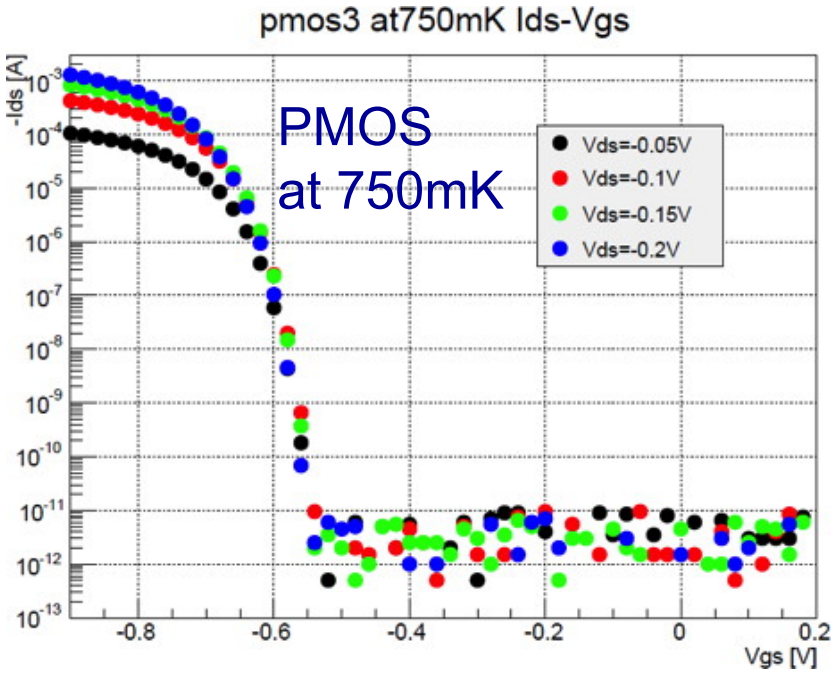
By building STJ sensors on SOI, multiple channel readout becomes possible!



Signal from Nb/Al STJ on SOI







II. Recent Progress

*Layout Shrinking with NMOS-PMOS merge

*Double SOI Wafer & Process

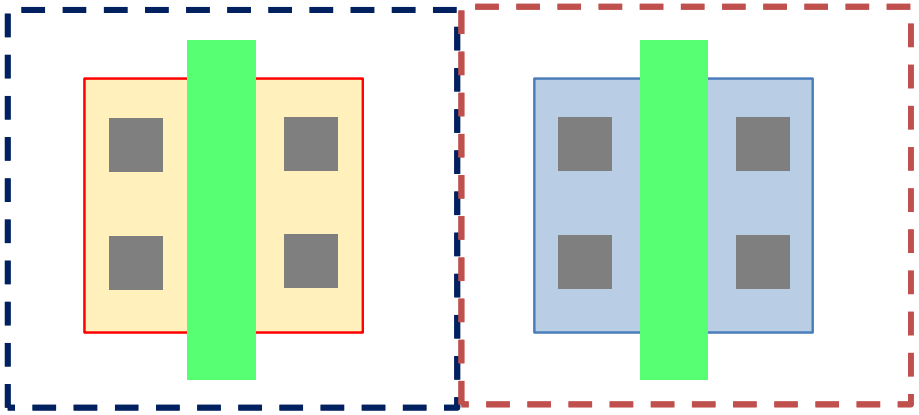
*Higher Dose LDD

*Compensation with Tunneling

Layout Shrink（Active Merge)

Bulk CMOS

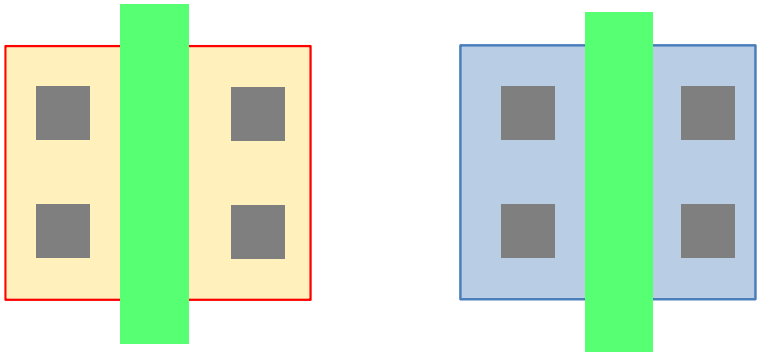
PMOS NMOS



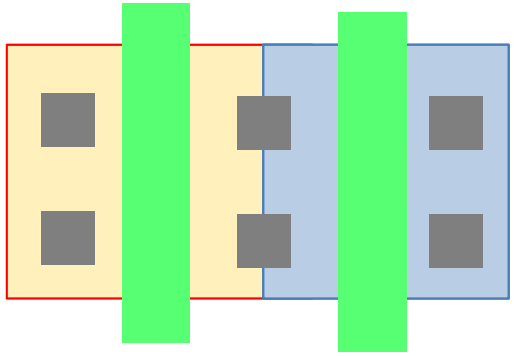
N-Well P-Well

SOI

PMOS NMOS



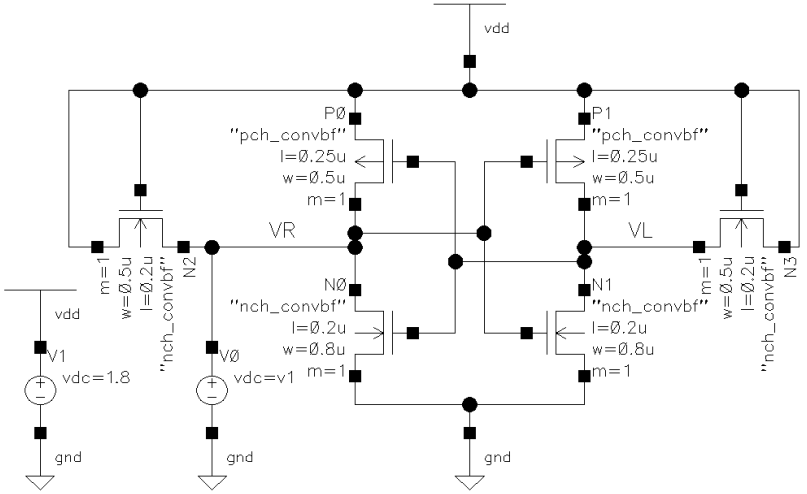
Share Contacts

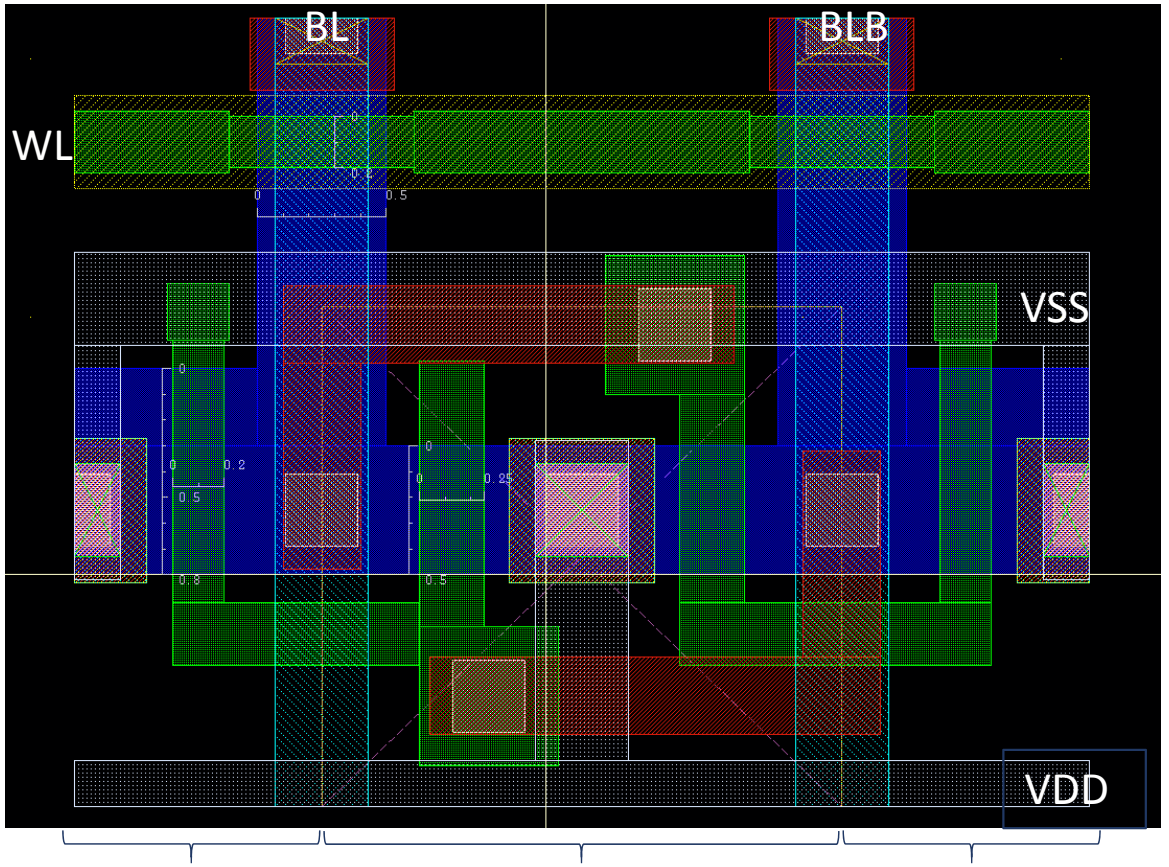


Salicide Connection

In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

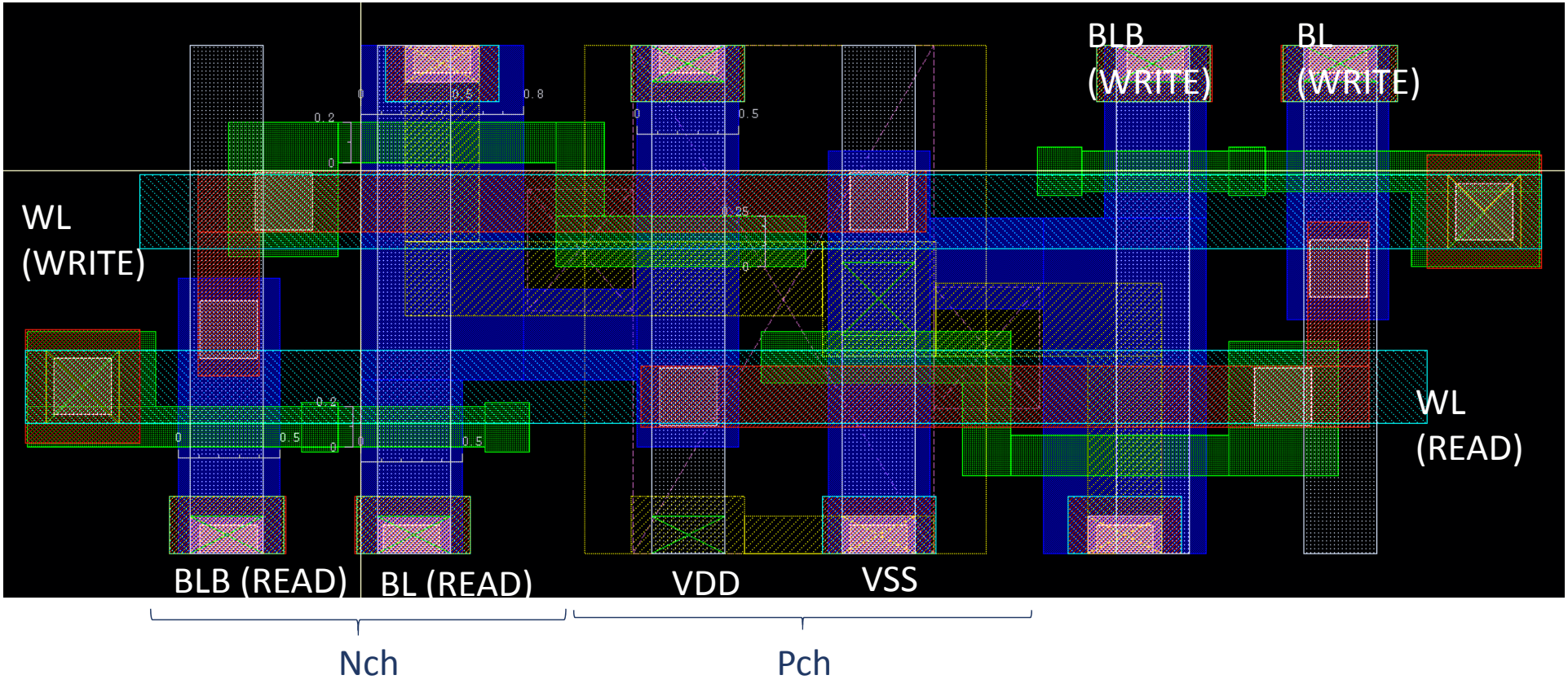
Single Port SRAM Bit Cell





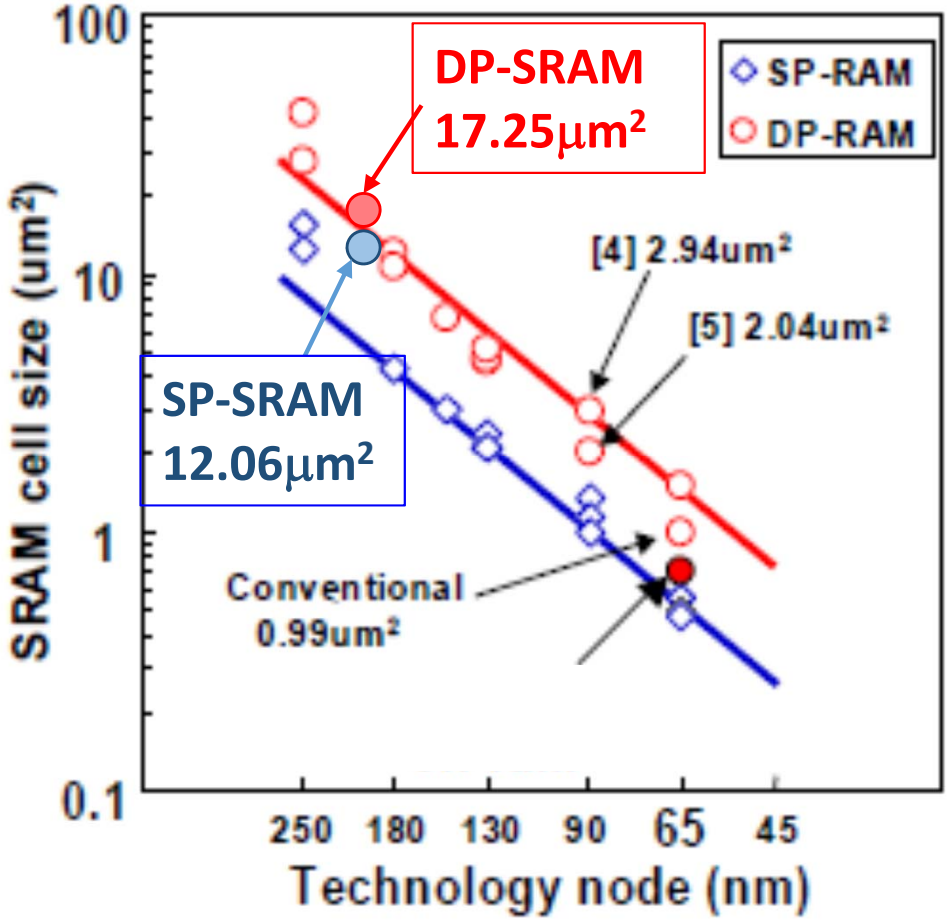
Cell Size : 3.94µm X 3.06µm = 12.06µm²

Dual Port SRAM Bit Cell



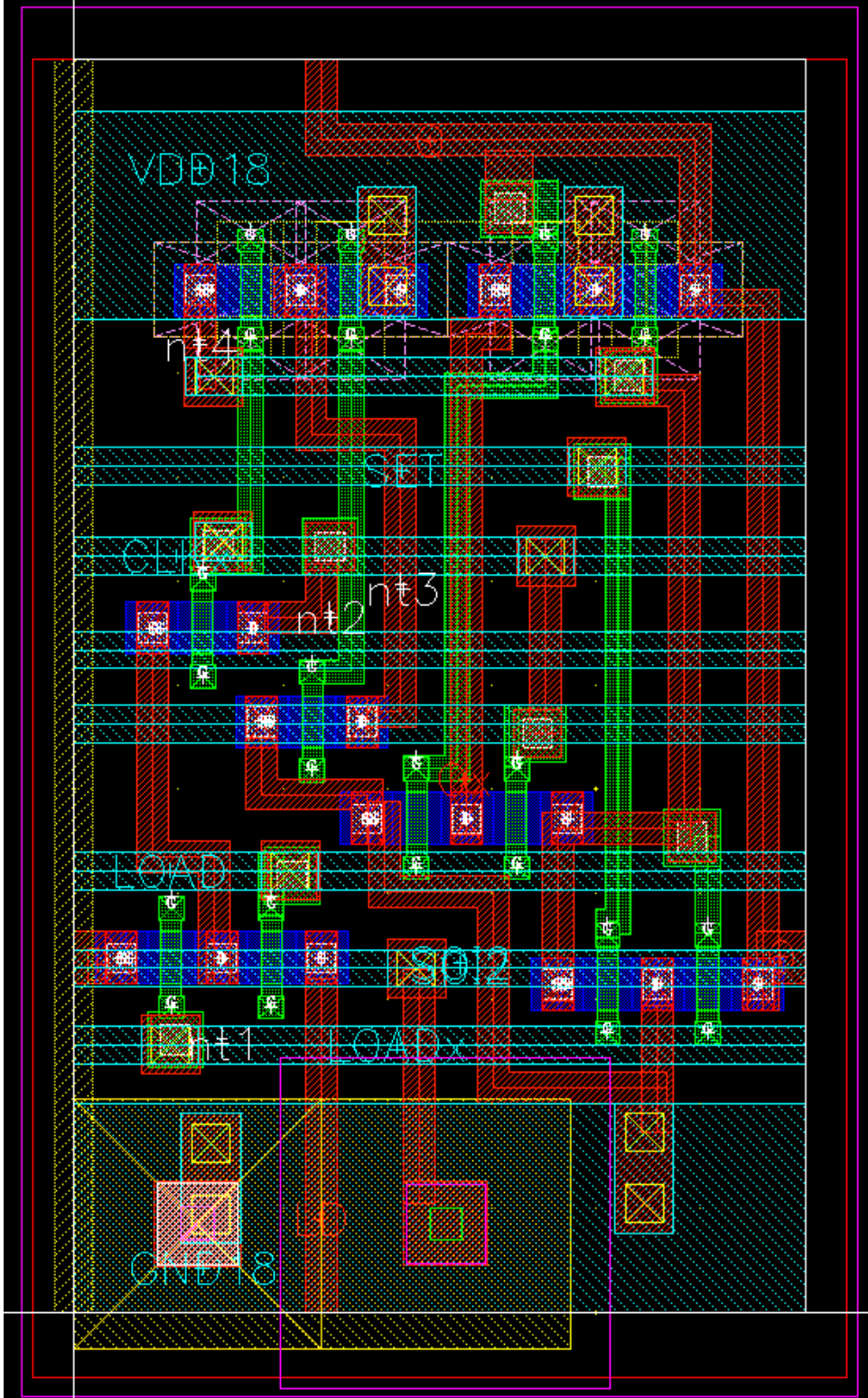
Cell Size : 6.90μm X 2.50μm = 17.25μm²

SRAM Cell Size Comparison



K. Nii, et al., Symp. VLSI Circuit Digst., PP. 130-131, 2006

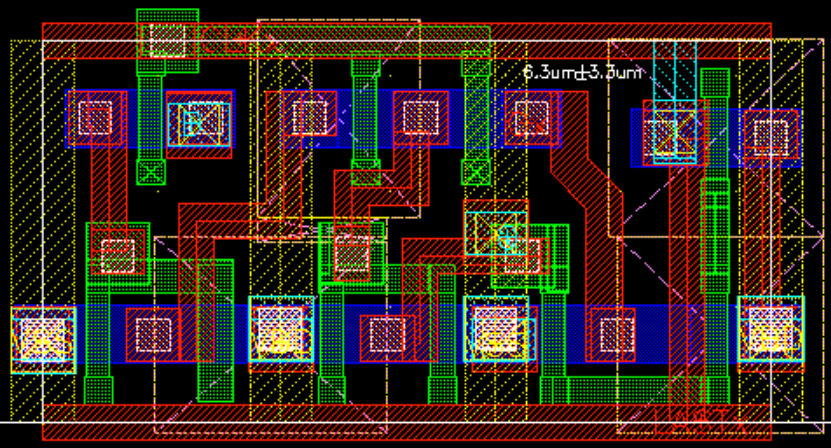
Cell size of the SP- and the DP-SRAM is almost comparable to that of advanced commercial products.



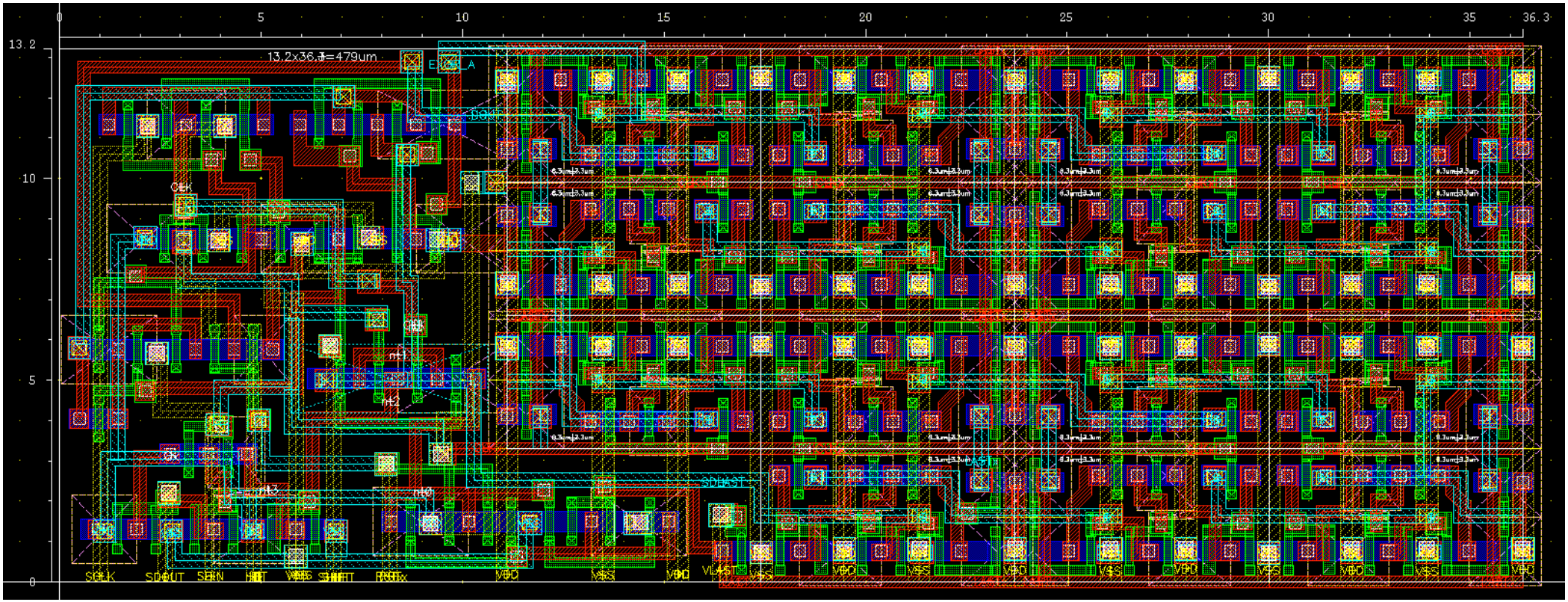
12x7=84um2

New D Flip-Flop
25% of Previous Cell

3.3x6.3=20.79um2



15bit Counter + Overflow bit with Serial I/O



13.2um x 36.3 = 479 um^2

II. Recent Progress

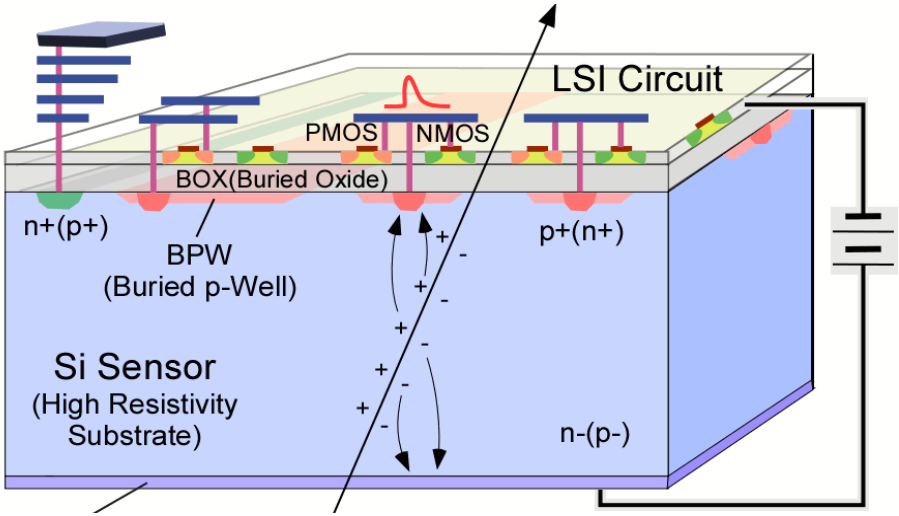
*Layout Shrinking with NMOS-PMOS merge

*Double SOI Wafer & Process

*Higher Dose LDD

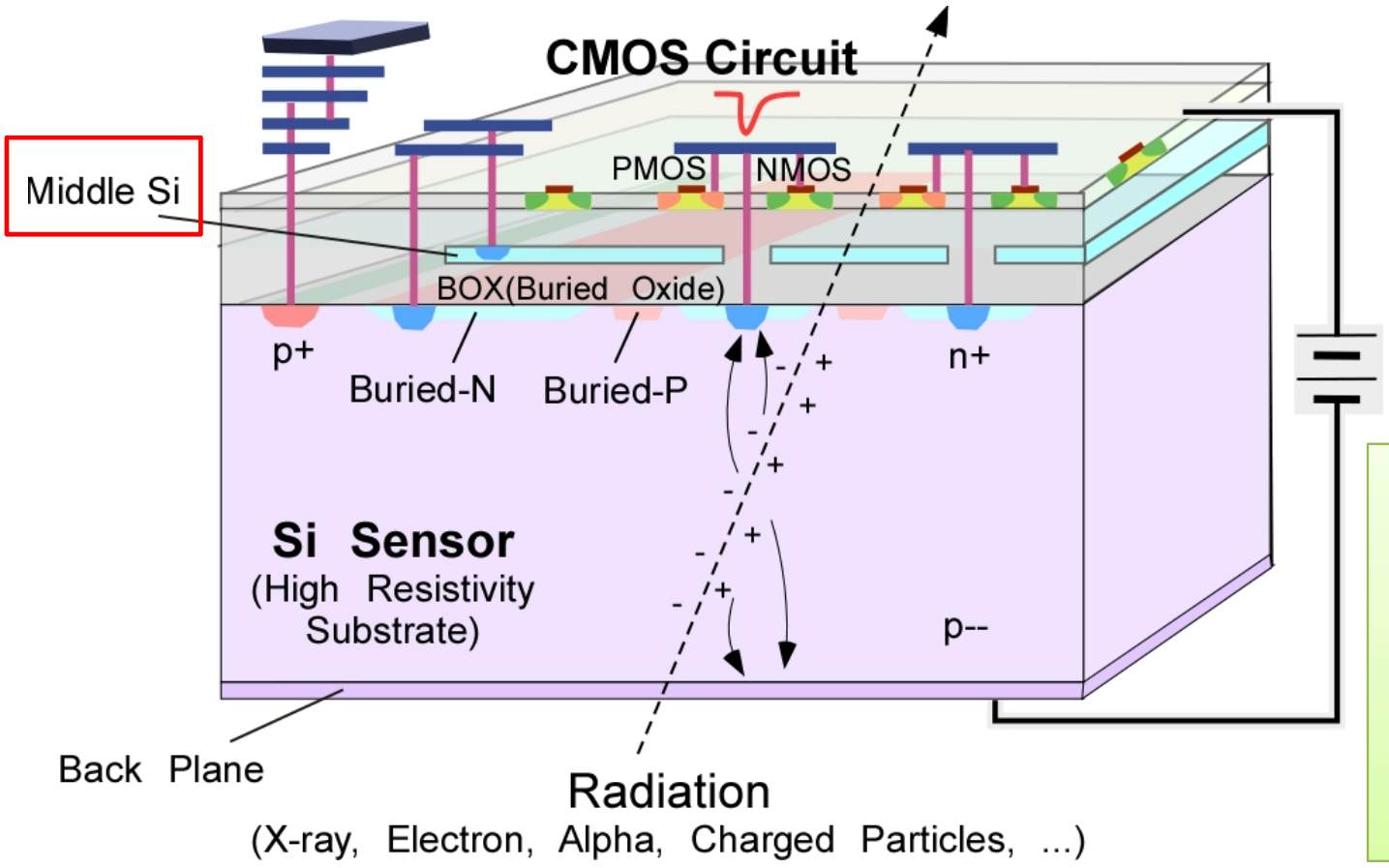
*Compensation with Tunneling

Single to Double SOI

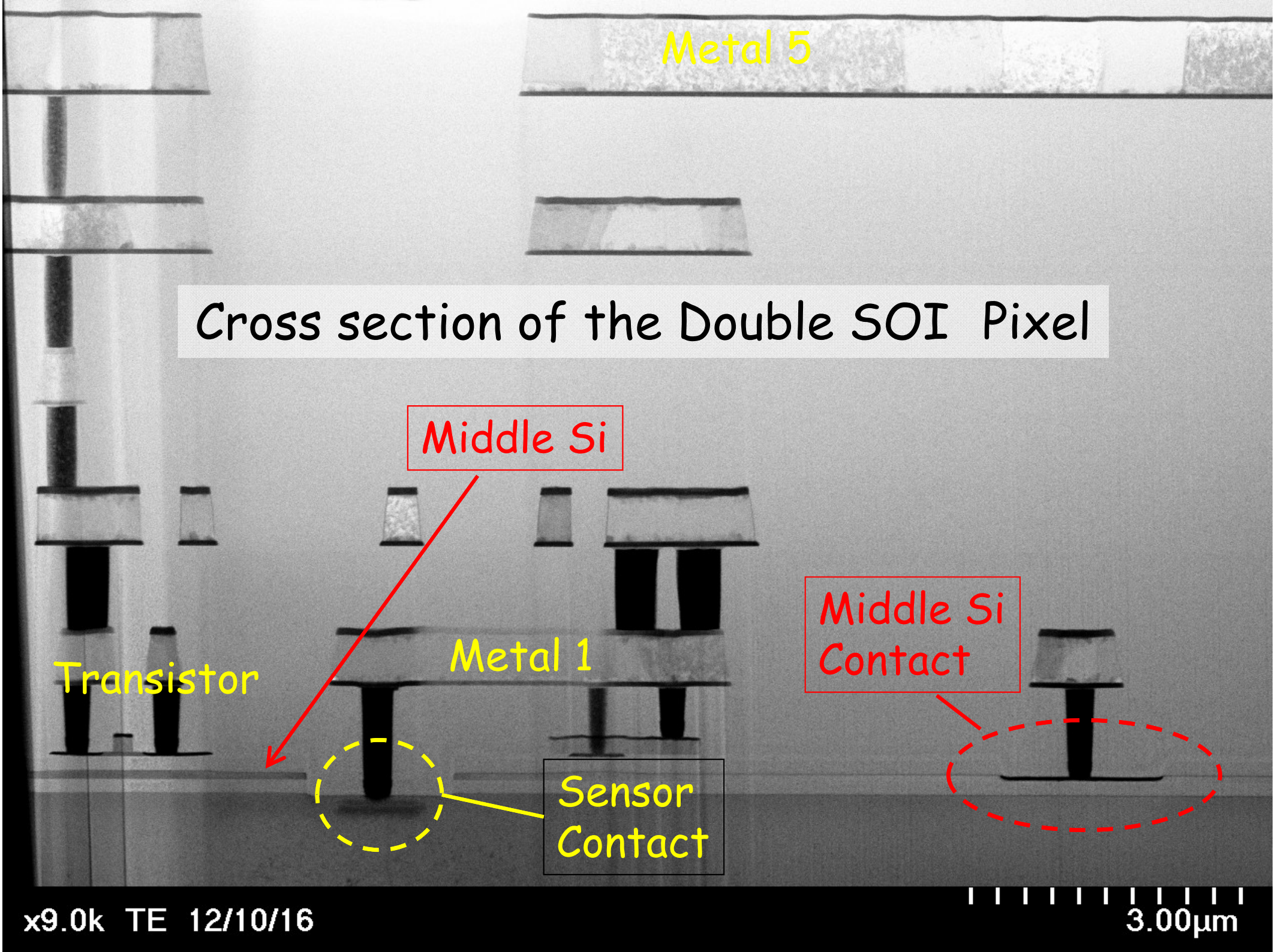


Single SOI

Double SOI



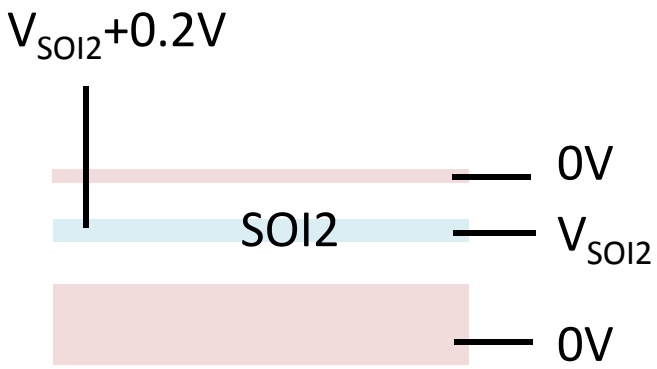
- Shield Sensor–Circuit Interference
- Compensate radiation induced oxide trap charge


Metal 5
Cross section of the Double SOI Pixel
Middle Si
Transistor
Metal 1
Middle Si
Contact
Sensor
Contact
x9.0k TE 12/10/16
3.00µm

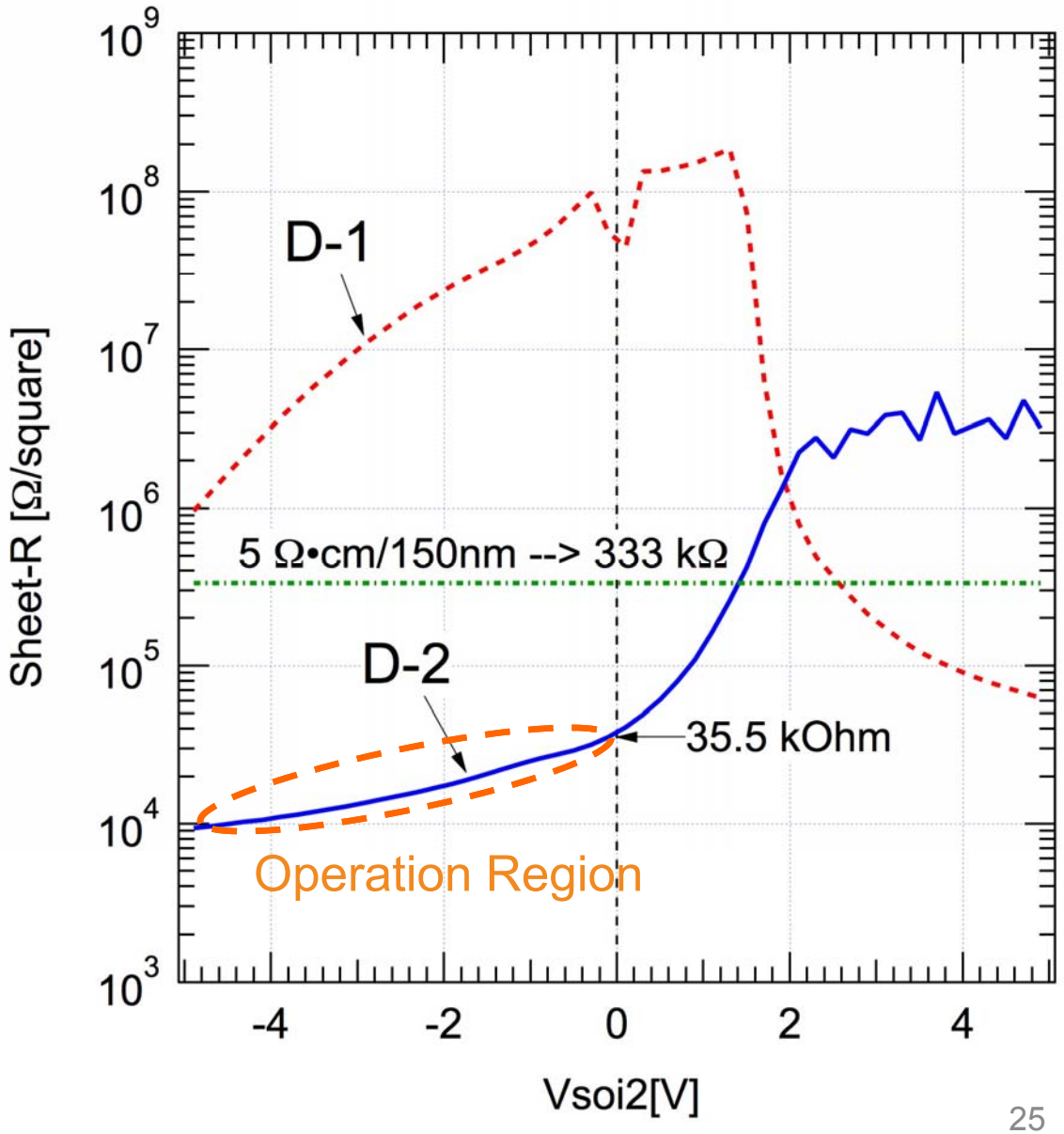
Structure of 2 kinds of Double SOI wafer

Layer	D-1	D-2
SOI1	p-type 88 nm, <10 Ω•cm	p-type 88 nm, <10 Ω •cm
BOX1	145 nm	145 nm
SOI2	p-type 88 nm, <10 Ω •cm	n-type 150 nm, <10 Ω •cm
BOX2	145 nm	145 nm
Substrate	n-type CZ, 725um, >700 Ω •cm	p-type Low Oxygen CZ, 725um, >1.0 k Ω •cm

Sheet Resistance of the Middle Si (SOI2)

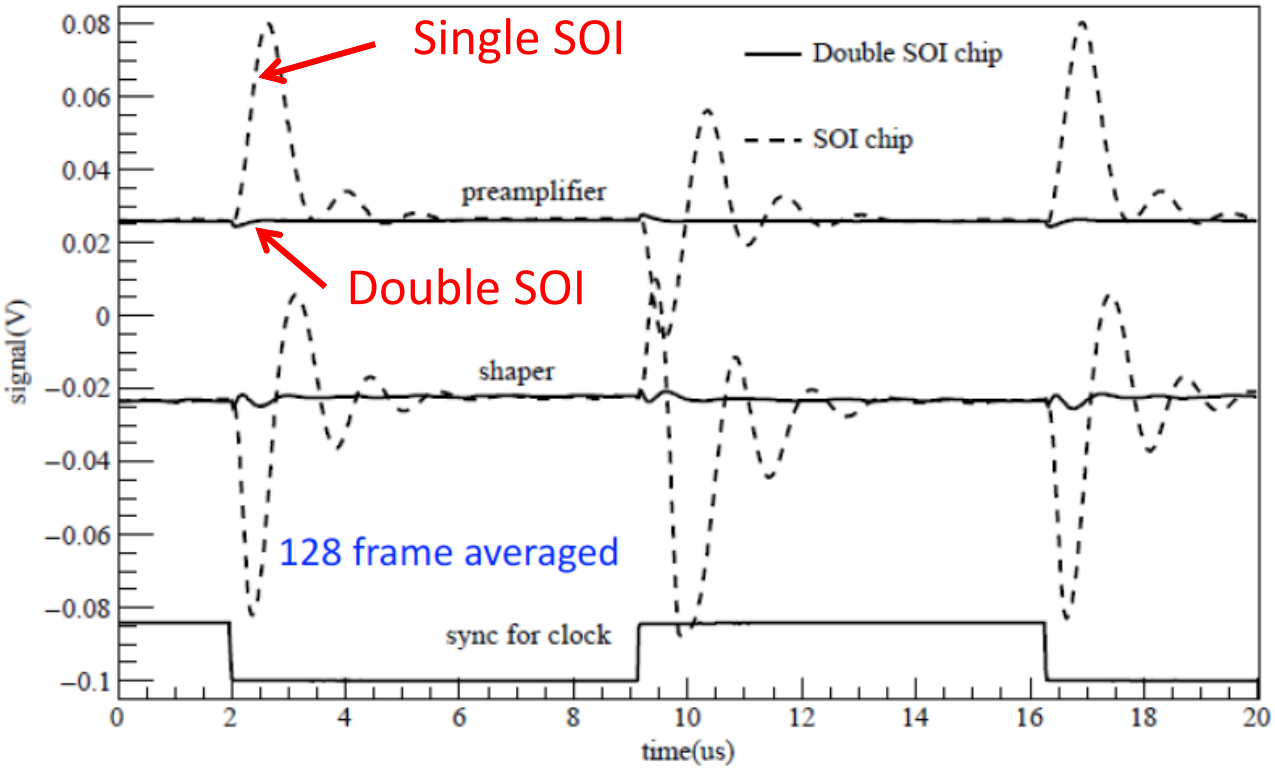


Sheet resistance of the middle Si changes depend on its potential.
D-2 wafer has lower resistance in operation region.



- Crosstalk from counter
  - 5mV @ shaper output for DSOI (74 e^- referred to input charge), negligible when superimposed with noise (ENC ~ 113e^-)
  - 95mV for normal SOI (note the gain of shaper reduced)
  - Compelling proof of shielding effectiveness

By using Double SOI wafer, Cross Talk between Circuit and Sensor is reduced to 1/20.



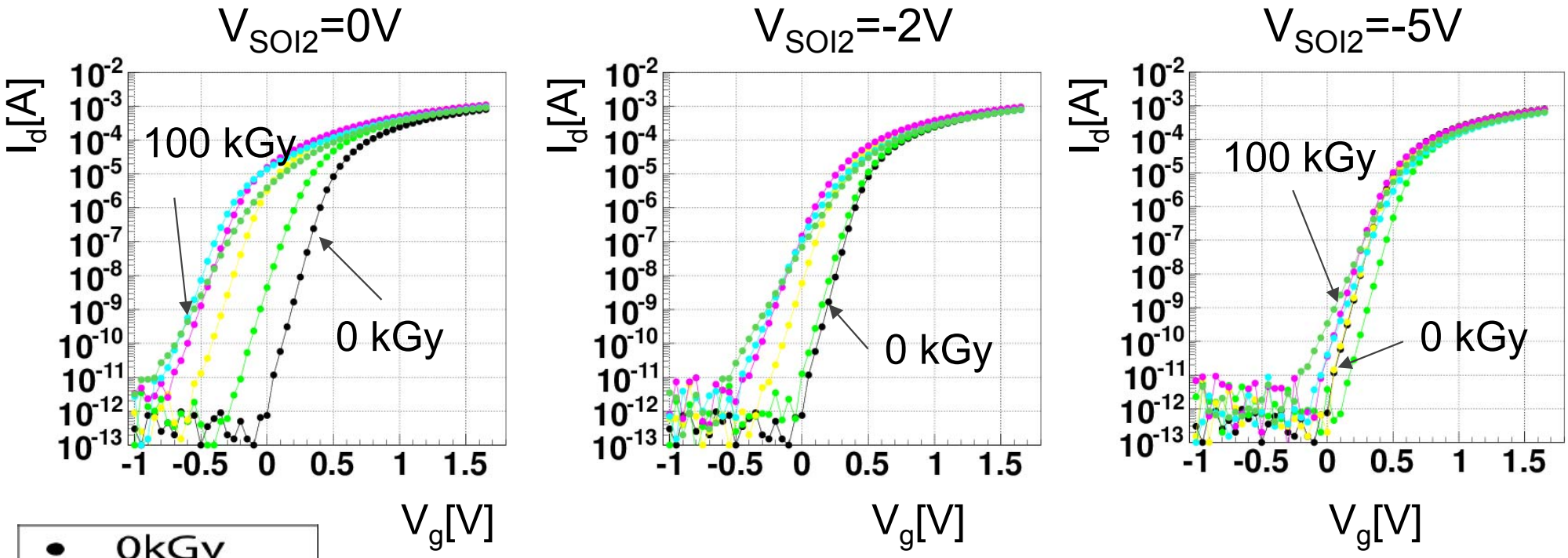
	Double-SOI	Normal SOI
Preamp output(peak to peak)	3.7mV	60mV
Shaper output(peak to peak)	5mV	100mV

(by Lu Yunpeng (IHEP))

Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS



By setting Vsoi2 ~ -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si)

(by U. of Tsukuba)

II. Recent Progress

*Layout Shrinking with NMOS-PMOS merge

*Double SOI Wafer & Process

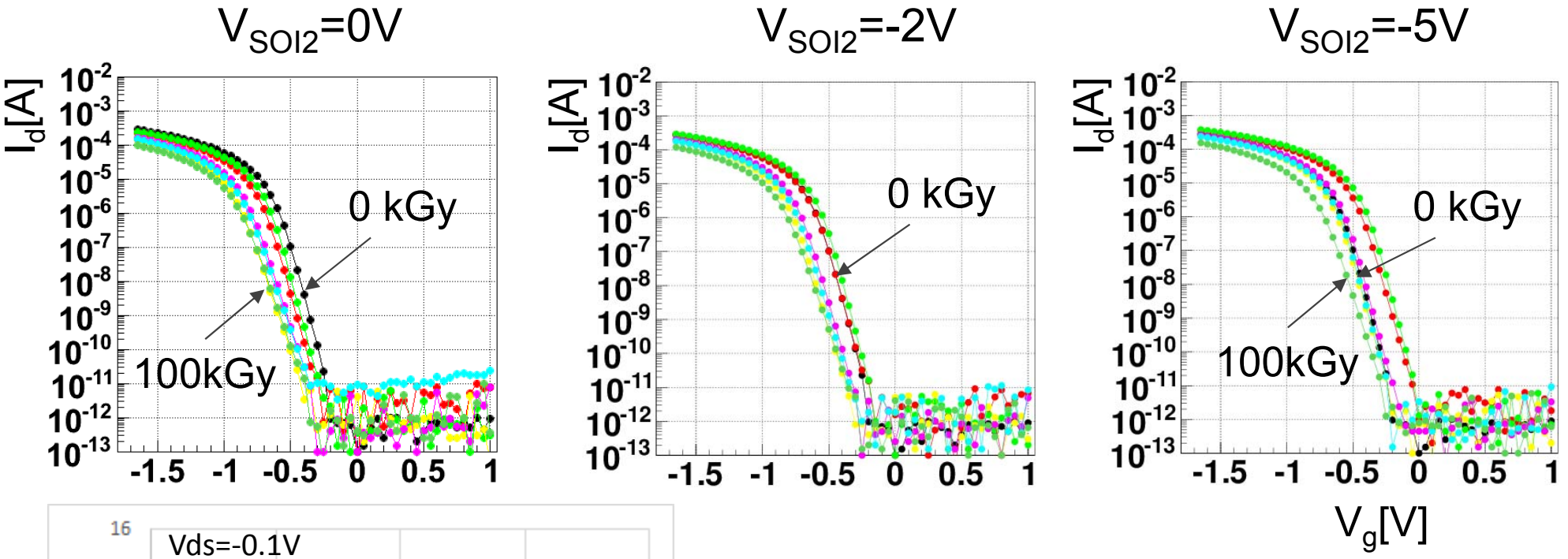
*Higher Dose LDD

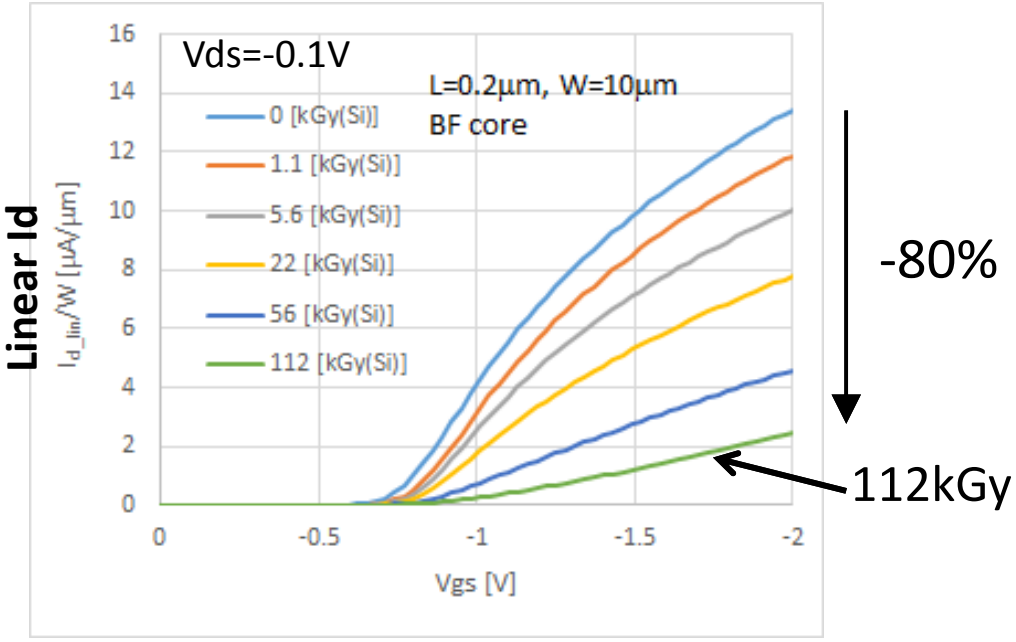
*Compensation with Tunneling

Variation of Id-Vg Characteristics and Effect of SOI2 Potential

PMOS

I/O Normal Vt
Source-Tie
L/W =0.35um/5um

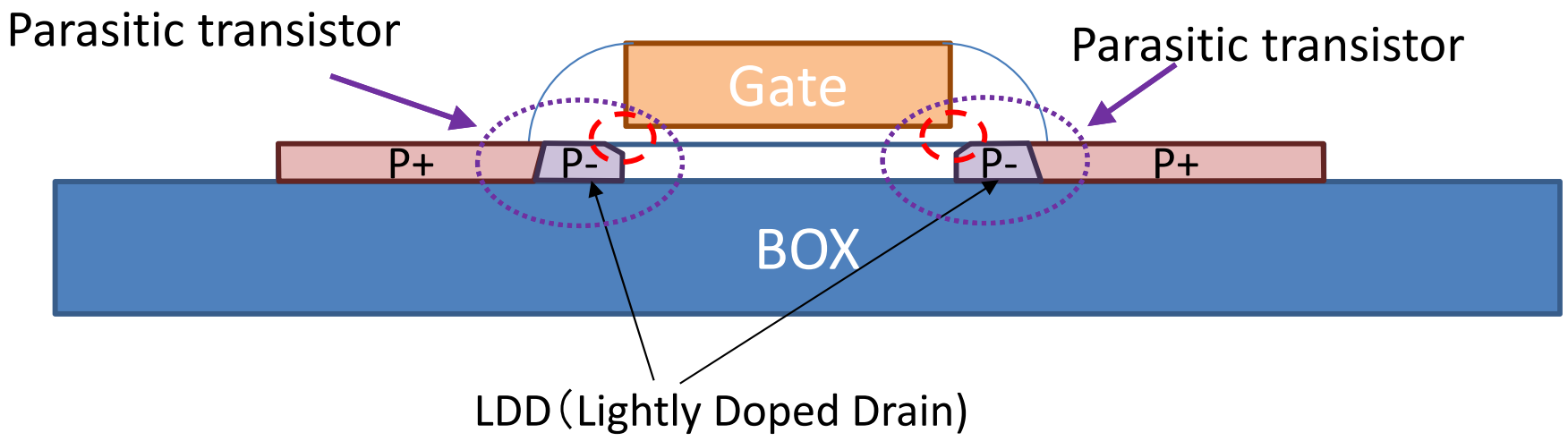




Threshold voltage shift is not so large in PMOS, but Drain Current decreases much .

Dose Increase in Lightle Doped Drain (LDD) Region

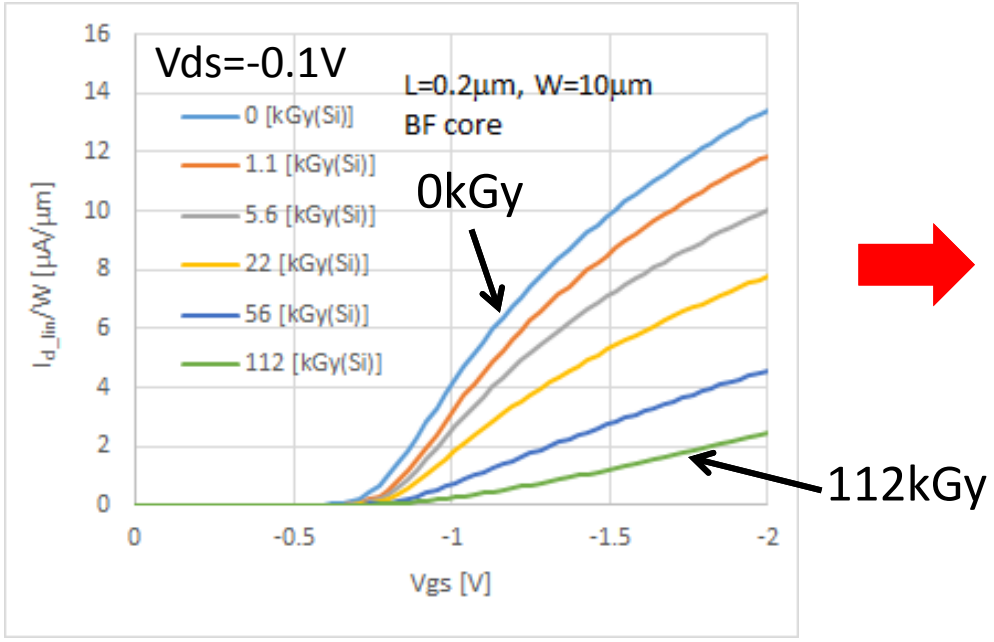
- Major cause of the drain current degradation by radiation is Vt increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the Vt of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.



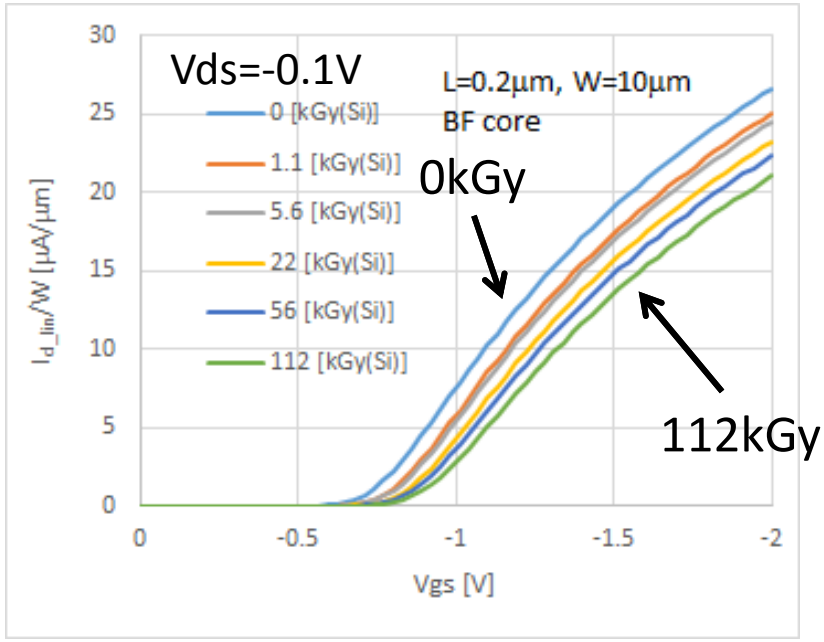
(by I. Kurachi)

Id-Vg Characteristics in Triode Region

Present Process



LDD Dose x 6

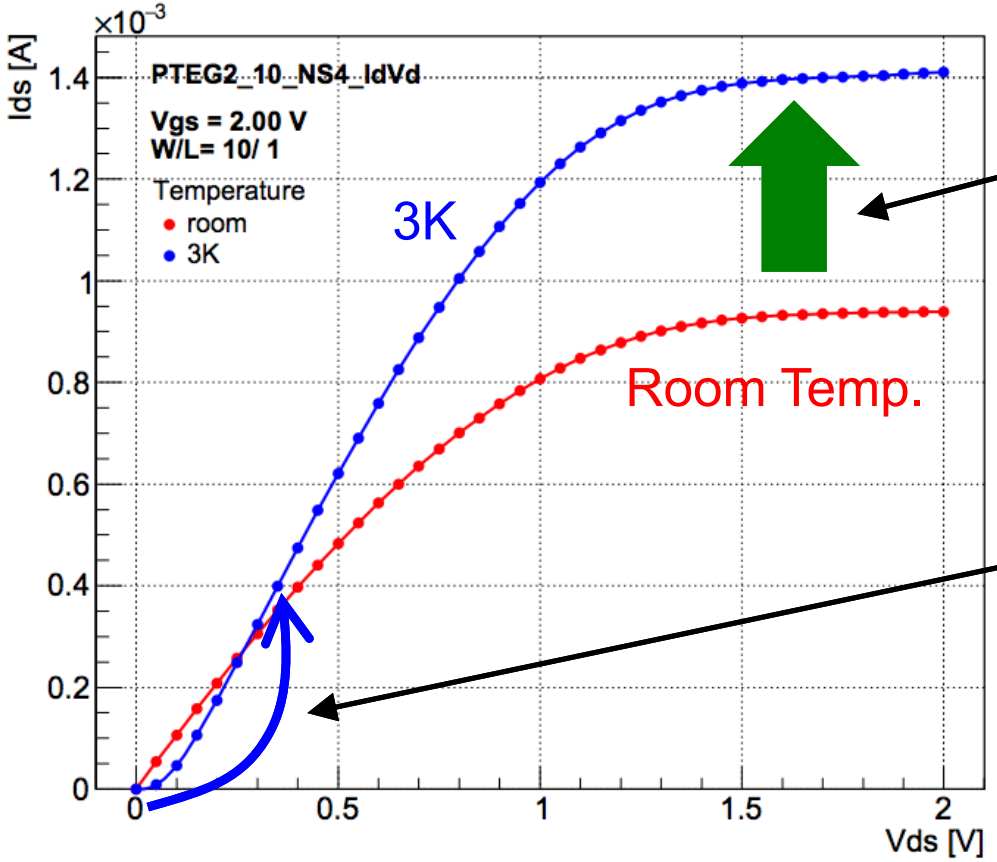


With increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 krad(Si).

Ref.) I. Kurachi, et al. "Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs, IEEE Trans. on Elec. Dev. Vol. 62, Aug. 2015, pp. 2371-2376.

Ultra-Low Temperature Operation

One of the feature in SOI transistor is operation capability in ultra-low temperature.

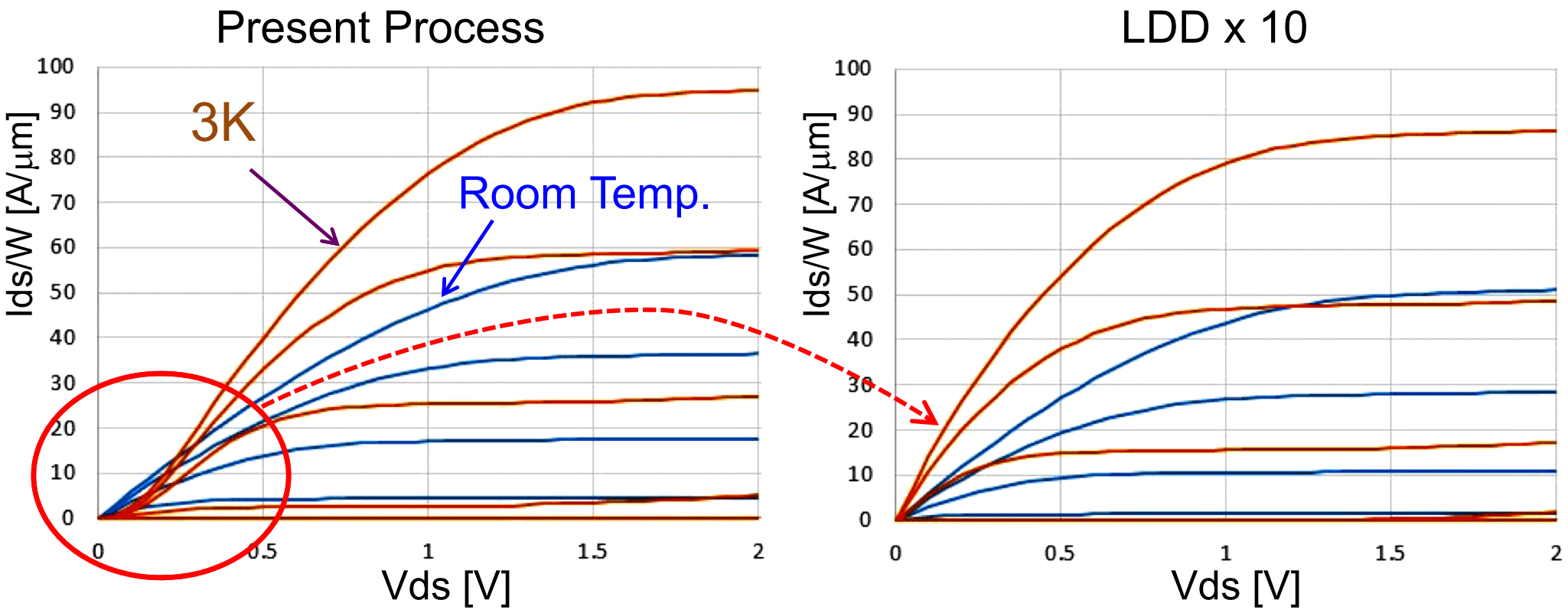


Drain Current Increase due to increase of carrier mobility

Slow rise in low Vds region!

Improvement in Ultra-Low Temperature

Pch Transistor
Source-Tie type 2
L=1um, W=10um



By increasing the LDD dose 6~10 times, characteristic of the transistors becomes smooth in Ultra-Low Temperature.

II. Recent Progress

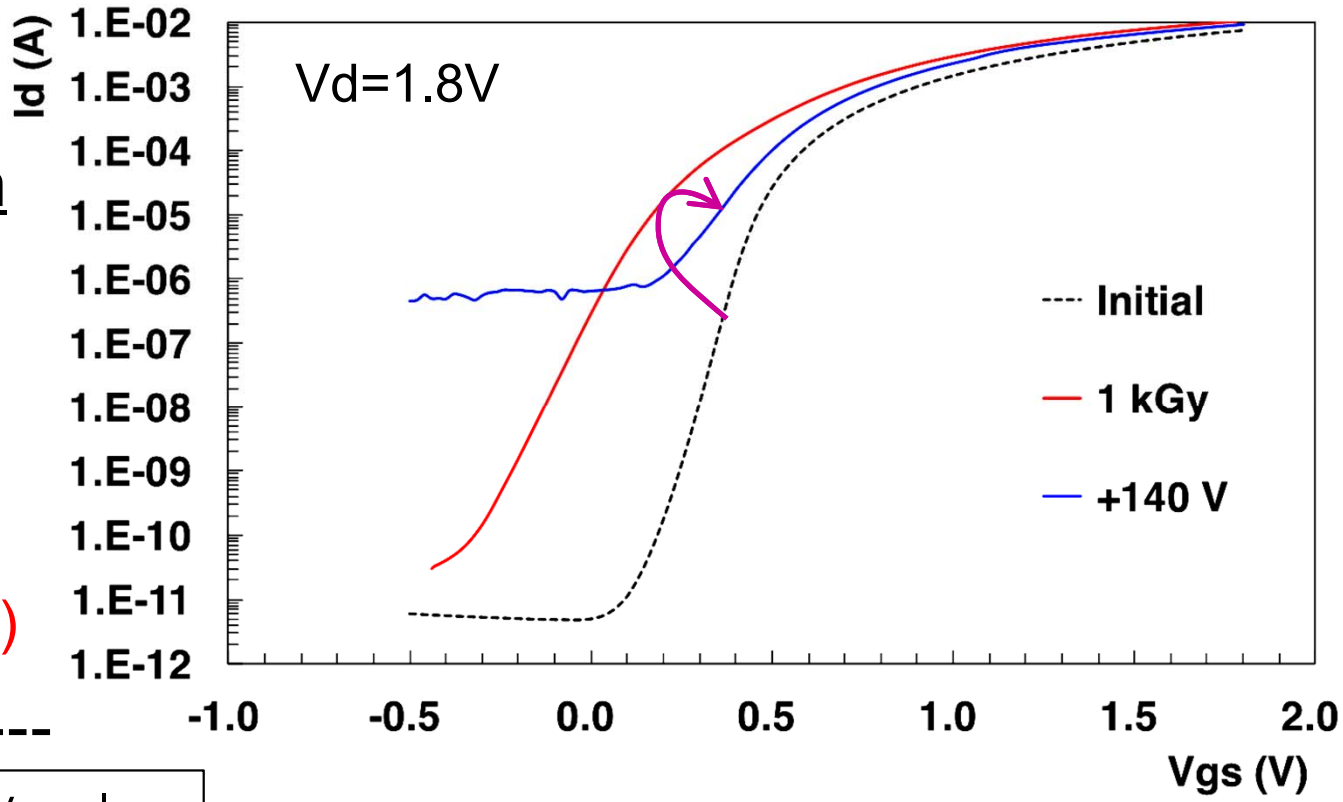
*Layout Shrinking with NMOS-PMOS merge

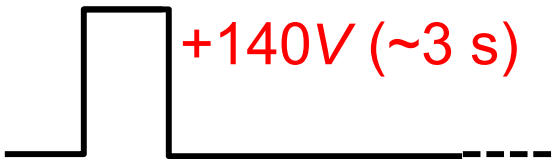
*Double SOI Wafer & Process

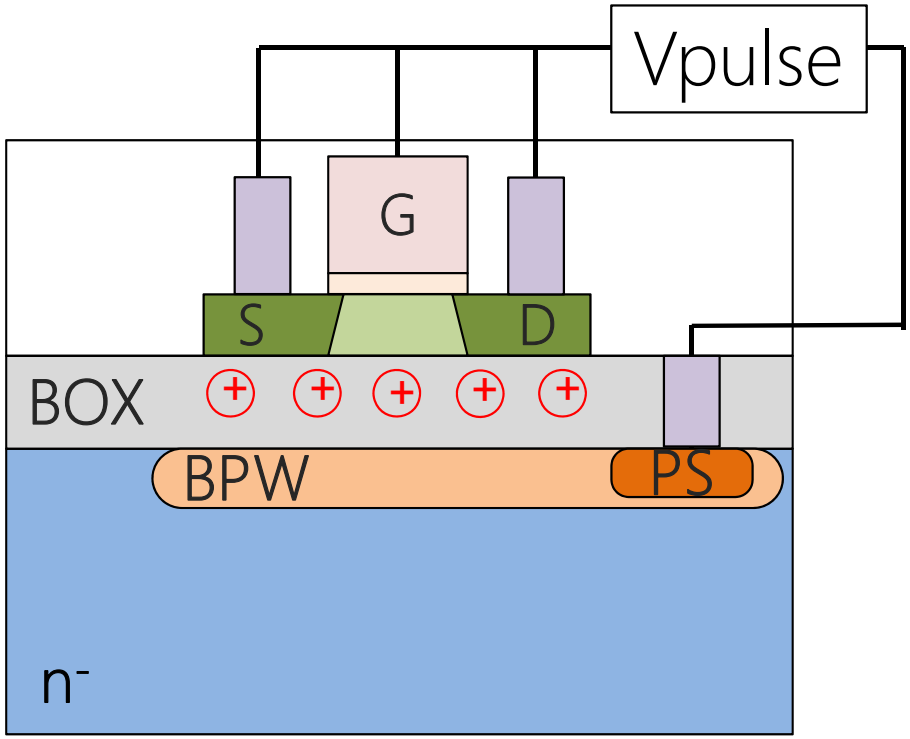
*Higher Dose LDD

*Compensation with Tunneling

HV Impulse Application

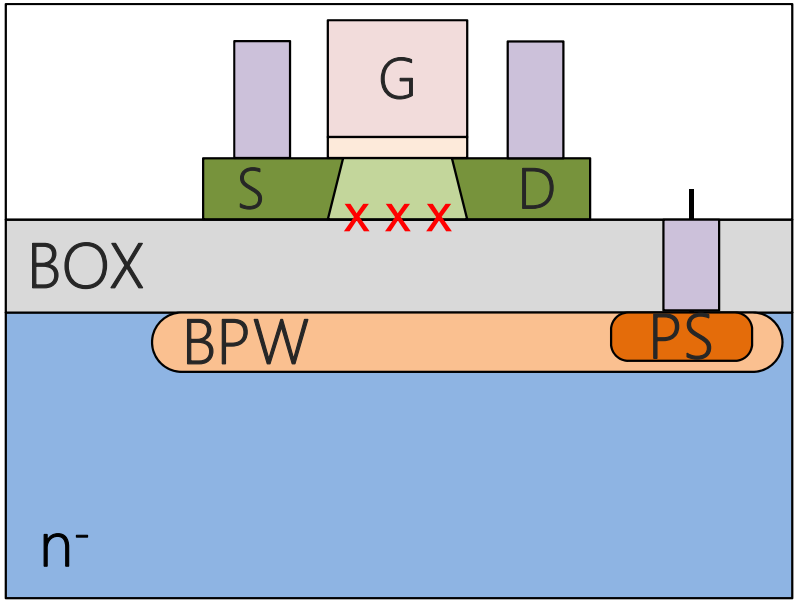


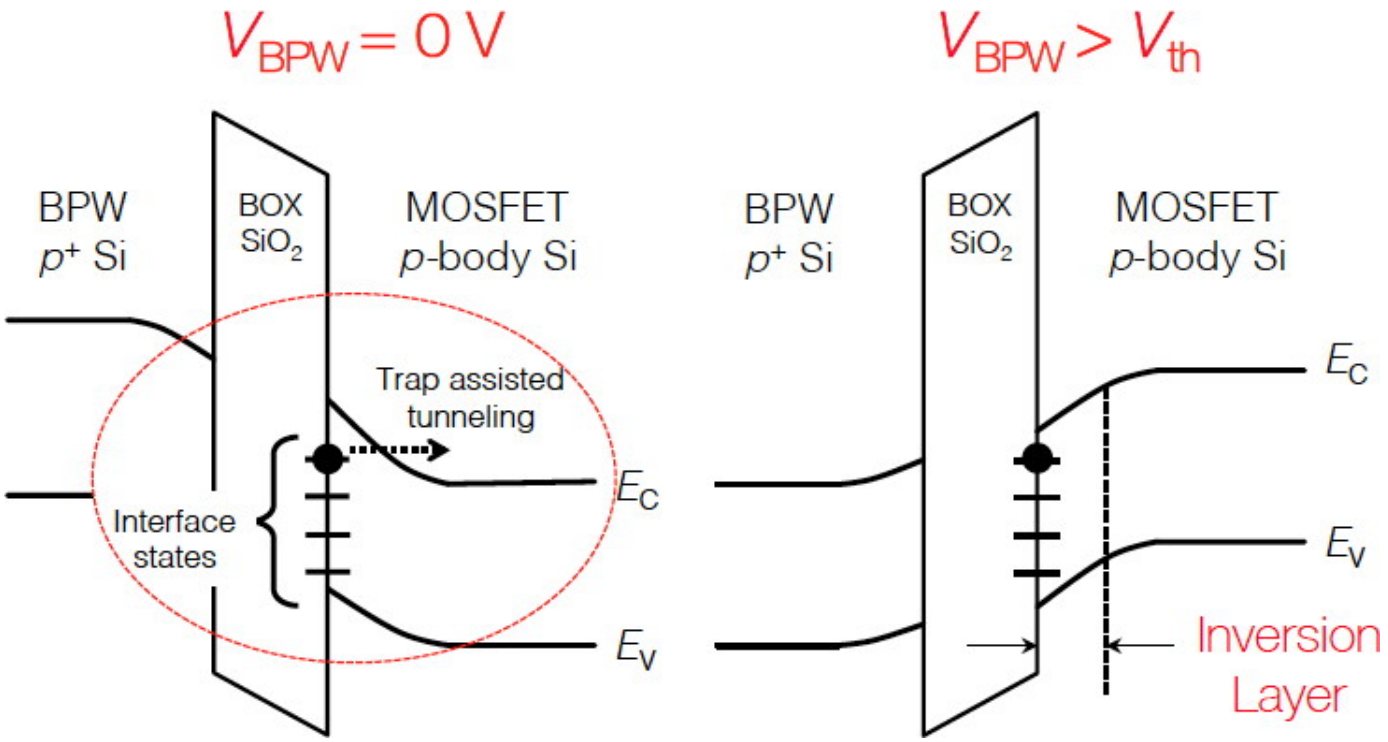




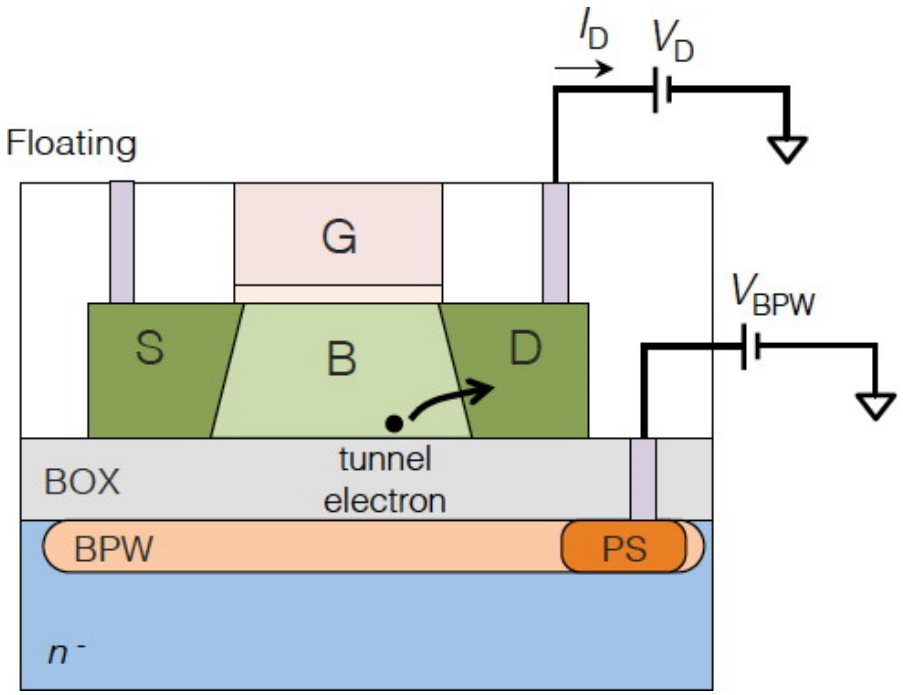
Threshold shift with radiation is recovered by applying a HV pulse to under-layer (SOI2 or BPW) of transistor.
However, Leakage current was increased.

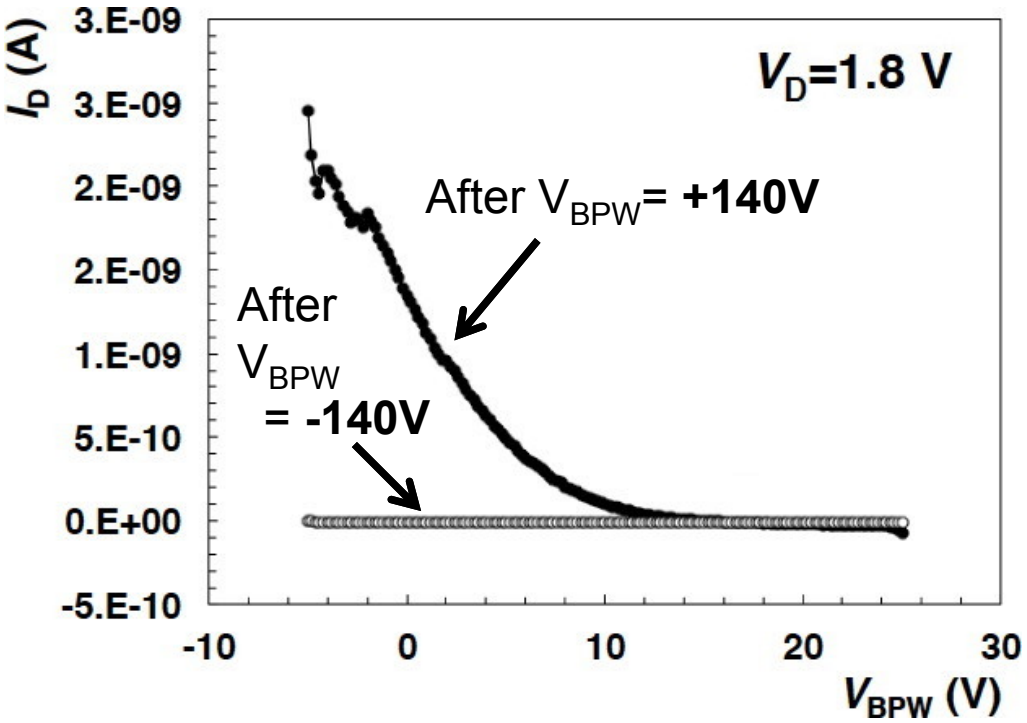
We assumed the origin of the leakage current is Trap Assisted Tunneling.
If so, the leakage current should disappear when an inversion layer is generated at the bottom of the transistor.





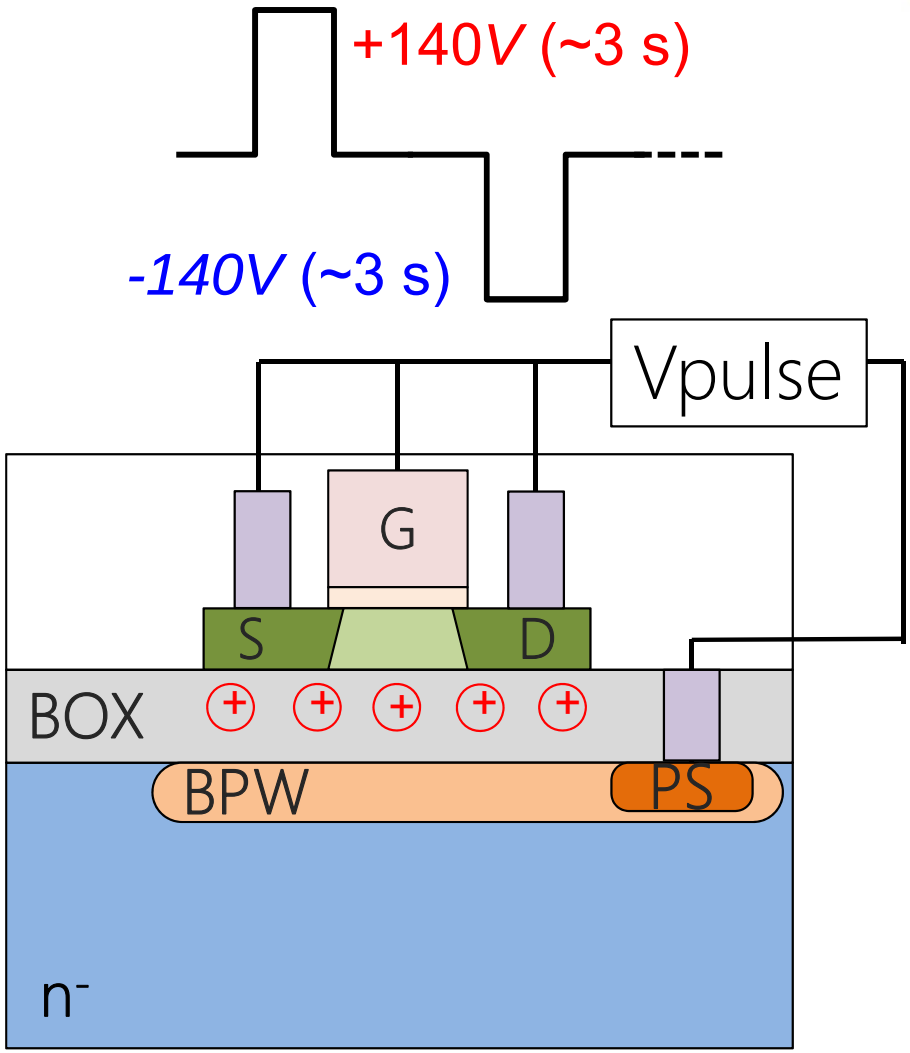
Confirmation of the Trap Assisted Tunneling

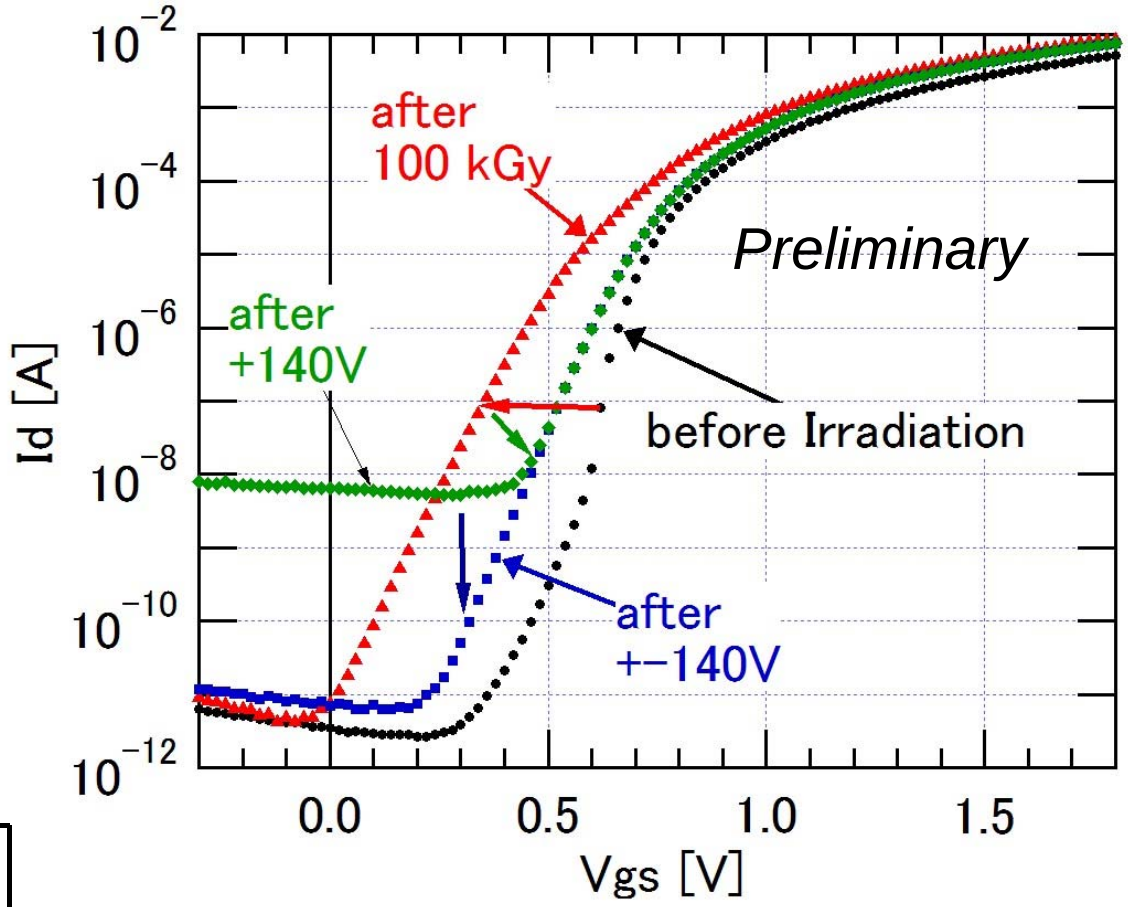




After generating an inversion layer at the bottom of the transistor by applying negative pulse to the BPW layer, drain current become insensitive to the back gate (BPW) voltage.

Removing Radiation Induced Oxide Charge with FN Tunneling





Radiation damage is recovered by applying Plus-Minus HV pulses to under-layer of transistor.

Summary of Solutions in SOI pixel detector

	Back Gate Effect	Sensor Circuit Interference	Vt Shift by radiation	Un-isotropic damage by radiation	Id degradation by radiation	Id slow rise @Low Temp.
Buried Well	○	X	△	△	-	-
Nested Well	○	△	△	△	-	-
Double SOI	○	○	○	△	-	-
Higher LDD Dose	-	-	-	-	○	○
FN Tunneling	-	-	○	○	-	-

III. Summary

- SOI Pixel 検出器は放射線センサーと読み出し回路とを一体化したモノリシック・センサー。
- SOI Pixelの相乗りプロセス(MPW run)を年1~2回行い、様々な検出器を開発している。
- 新学術領域研究では、高エネルギー物理以外の、X線天文、放射光、宇宙遠赤外線、イメージング質量分析、等様々な分野の研究者が参加している。
- Double SOIウエハーや、新センサー構造、STJ等のさまざまな提案があり、放射線耐性の向上、複雑な機能の内臓、感度の向上等に向け新たな研究が進んでいる。
- 次回MPWランは5月中旬締切。次回研究会を6月28-29日北大で行う。