Development of cryogenic SOI amplifier for COBAND experiment

Workshop for Unification and Development of the Neutrino Science Frontier (2017)

Rena Wakasa (Univ. of Tsukuba)
For COBAND collaboration

COBAND Experiment
COsmic BAckground Neutrino Decay

- Cosmic Background Neutrino Decay
  - The emitted photon energy

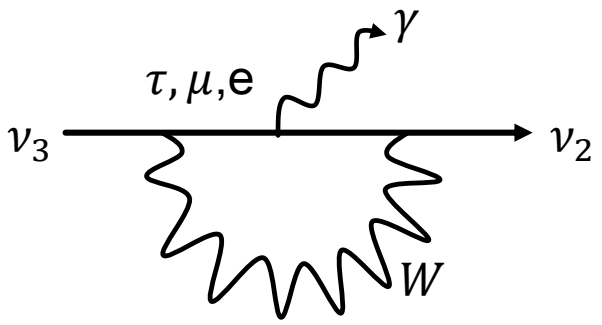
$$E_\gamma = \frac{|m_3^2 - m_2^2|}{2m_3}$$

The expected

$$E_\gamma \sim 25\mathrm{meV}$$

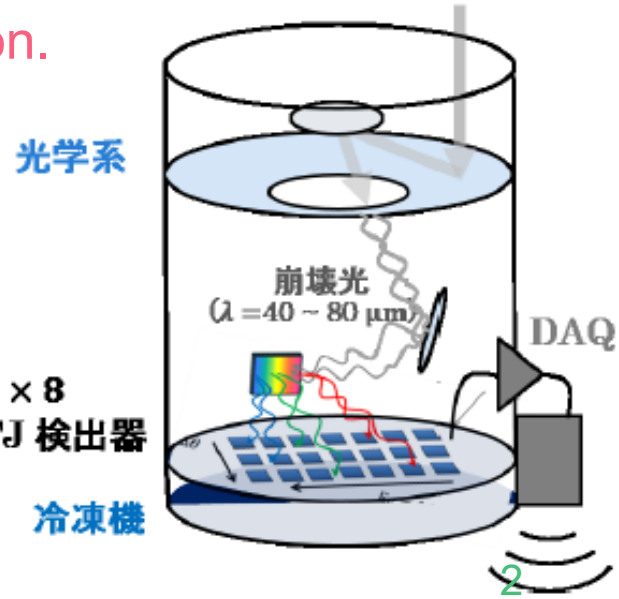
(λ=50μm, $m_3 = 50\mathrm{meV}$).

$|\Delta m_{32}^2| = (2.44 \pm 0.06) \times 10^{-3}\mathrm{eV}^2$
$\Delta m_{21}^2 = (7.52 \pm 0.18) \times 10^{-5}\mathrm{eV}^2$
by neutrino oscillation exp.



ニュートリノ崩壊光探索の概要図

高度200km, 約5分の観測



We use the superconducting tunnel junction.

- Rocket experiment
  - The diffraction grating splits the far inferred photons have wave length $40\mu\mathrm{m} - 80\mu\mathrm{m}$.
  - We count number of photons inputted the 50×8 array of the Nb/Al-STJ respectively and measure the energy spectrum.

Development of cryogenic SOI amplifier

- Introduction of cryogenic amplifier
  - Requirement for the leak current of Nb/Al-STJ.
    $I_{\mathrm{leak}} \sim 100\mathrm{pA}$
    →It is already achieved!!

STJ size	I_{leak} @300mK
50μm×50μm	224±29pA
20μm×20μm	39±13pA
10μm×10μm	14±7pA

  - However we have not been able to detect the far-inferred single photon yet, because of the large noise from the refrigerator's readout line.

Amplify the STJ signal by cryogenic amplifier placed near STJ.

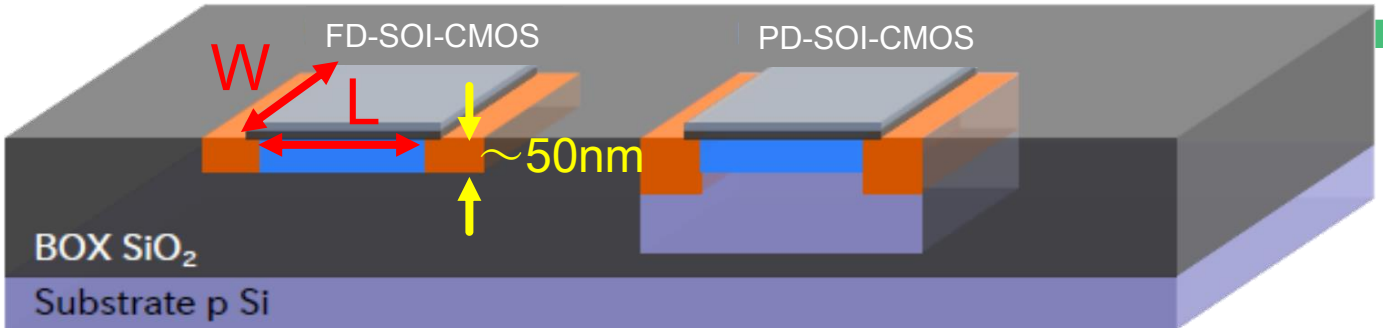
- Requirement for the cryogenic amplifier
  - Operation at cryogenic temperature (<3K)
  - Fast response speed (width of signal <10μs)
  - Low power consumption

	@4.2K	@300mK
Cooling power	250mW	100μW

Develop the amplifier using MOSFET under FD-SOI process.

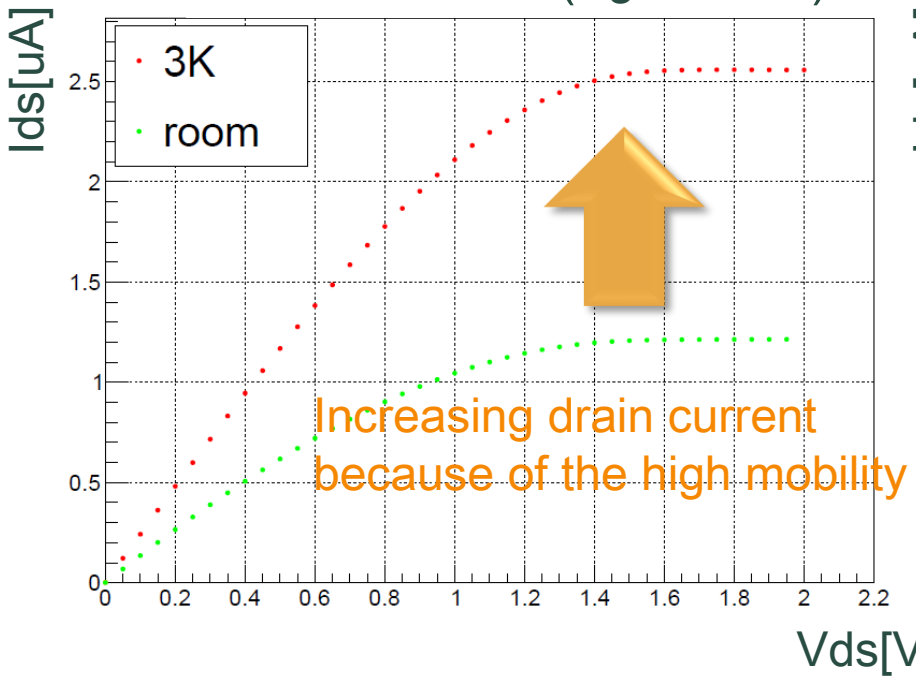
※JAXA/ISAS confirmed working of MOSFET under FD-SOI process at 4K.
T. Wada et al., J. Low. Temp. Phys. 167, (2012) 602

FD-SOI-MOSFET

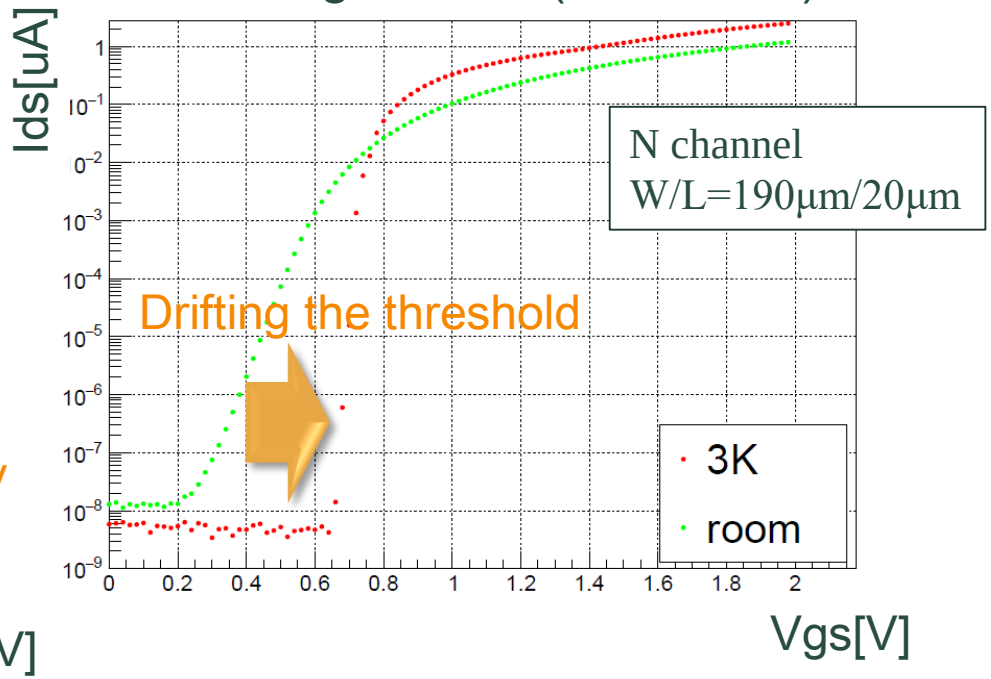


- FD-SOI
  Fully Depleted – Silicon On Insulator
  - Low power consumption
  - Suppress charge-up of the body

Ids-Vds Curve (Vgs = 2.0V)



Ids-Vgs Curve (Vds = 1.8V)



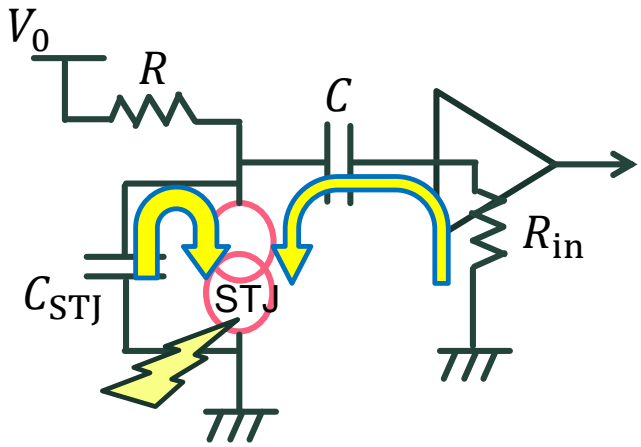
We can use FD-SOI-MOSFET with suitable bias voltages at low temperature.

Comparison between new and old SOI amplifiers

SOI-STJ4

- Common source circuit
- Input impedance
  $R_{\mathrm{in}} \sim 20\mathrm{k}\Omega$

The signal charges transferred to SOI amplifier is ~1/6 of the total since the STJ has capacitance of 40pF in parallel (@20μm sq.).

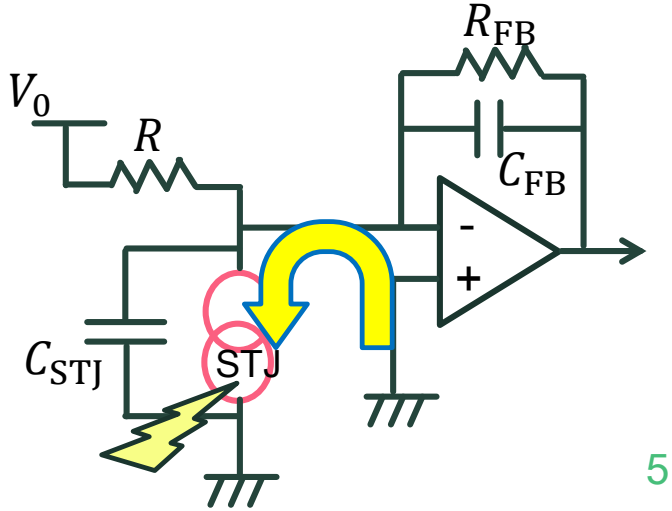


SOI-STJ5

Circuit

- Charge integrating operational amplifier with negative feedback
- Low input impedance caused by negative feedback（ideally, 0Ω）

Almost all signal charges are transferred to the SOI amplifier.

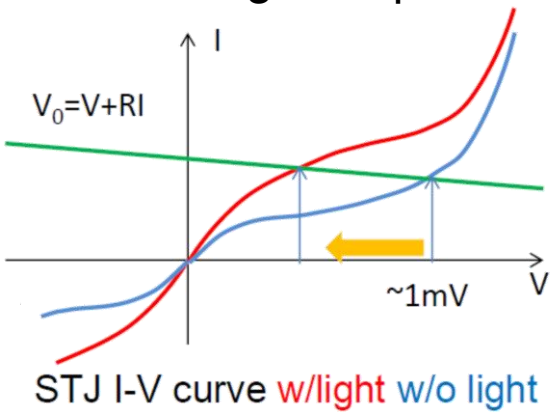


Comparison between new and old SOI amplifiers

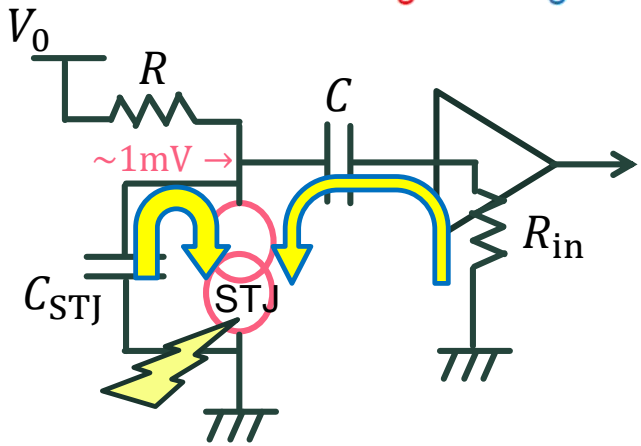
SOI-STJ4

- Constant current mode

SOI-STJ4 amplifies the variation of voltage from the light response of STJ.



STJ I-V curve w/light w/o light

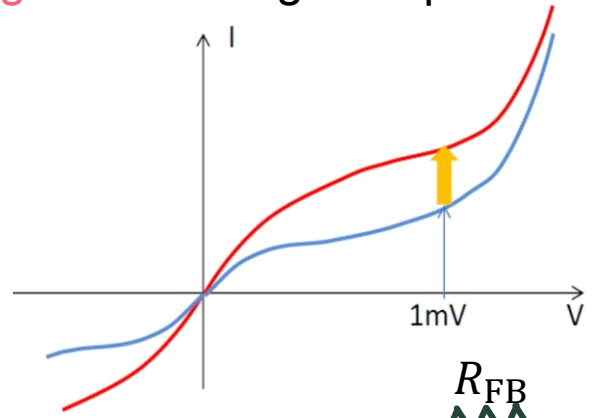


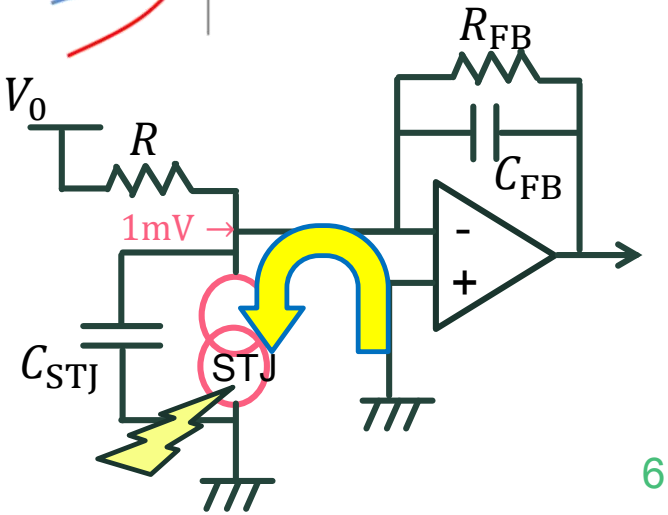
SOI-STJ5

Operation method

- Constant voltage mode

SOI-STJ5 amplifies the variation of charge from the light response of STJ.





Comparison between new and old SOI amplifiers

SOI-STJ4

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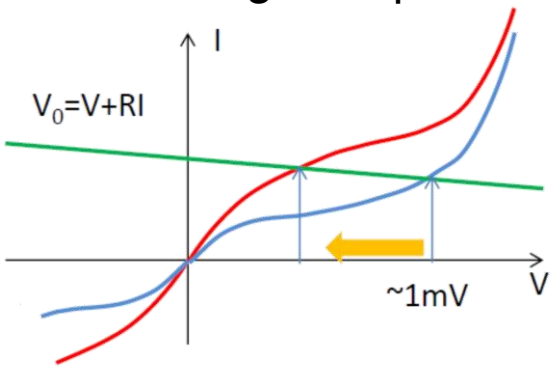

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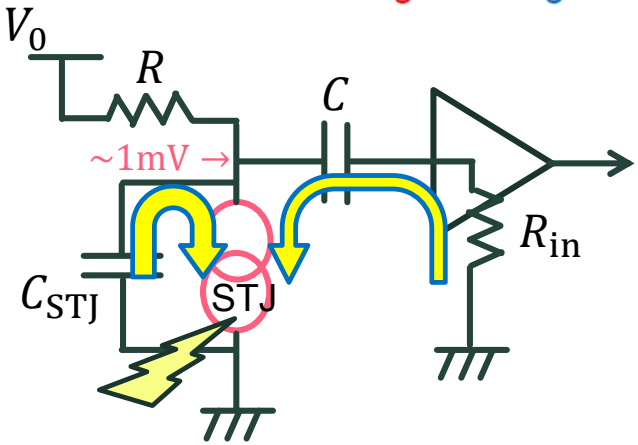
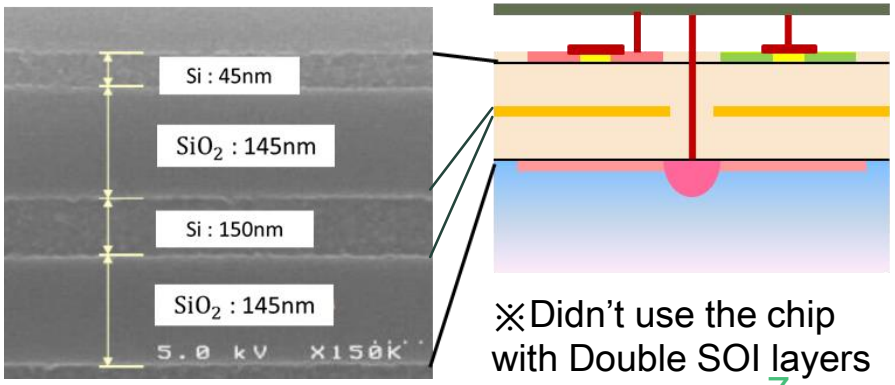


SOI-STJ5

Others

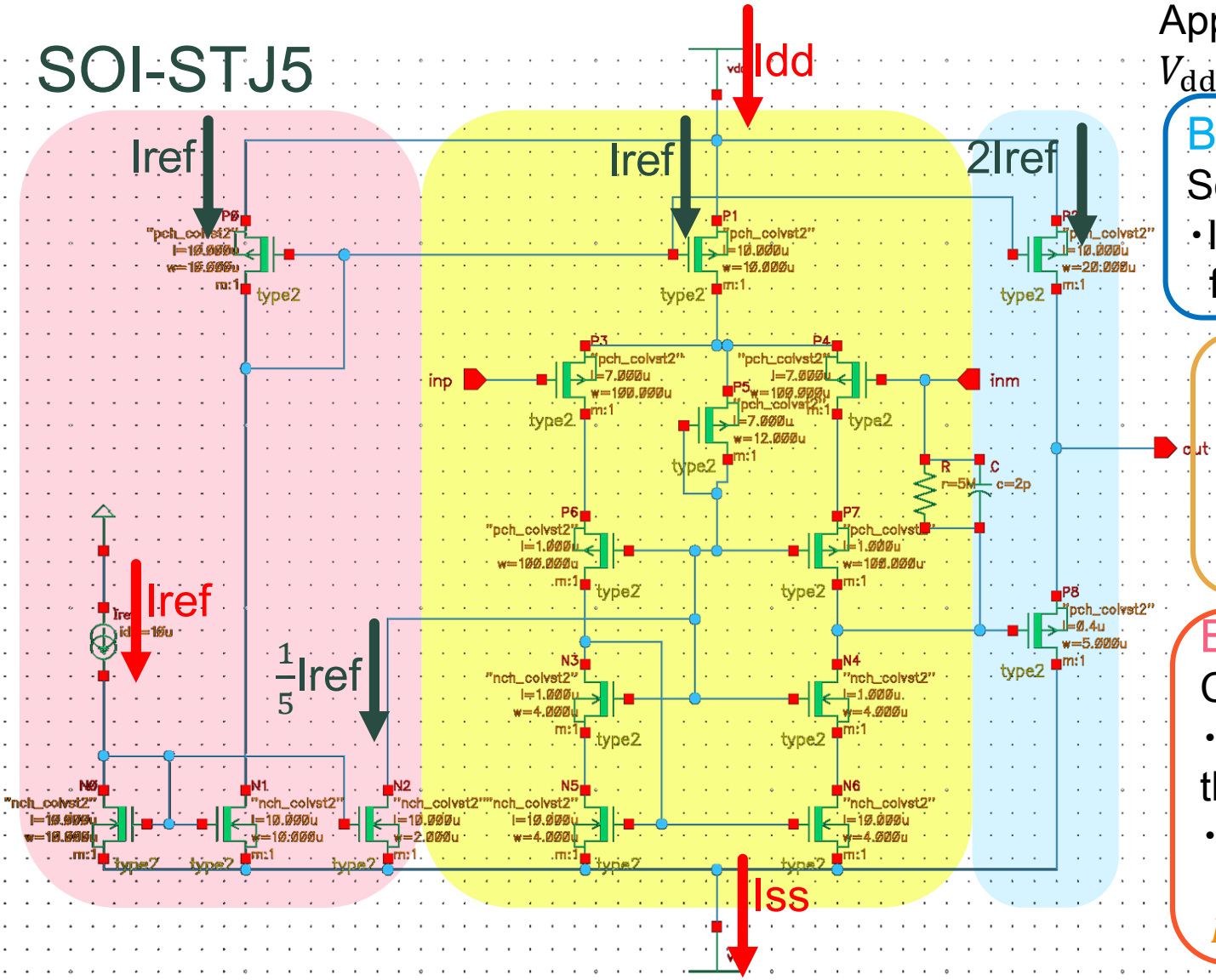
- FET with large-size W and L
  - Expect to suppress 1/f noises in proportion to $1/\sqrt{W \cdot L}$
- Double SOI layers
  - Expect to shift the threshold of FET by backgate

Suppress the power consumption



※Didn't use the chip with Double SOI layers in this time.

Circuit of SOI-STJ5



Applying Voltages

$V_{\mathrm{dd}} = 1.5\mathrm{V}\,, V_{\mathrm{ss}} = -1.5\mathrm{V}$

Buffering Stage

Source Follower Circuit

・Improvement of frequency band

Amplifying Stage

Op-Amp with Negative Feedback

・Lowering input impedance

Bias Circuit

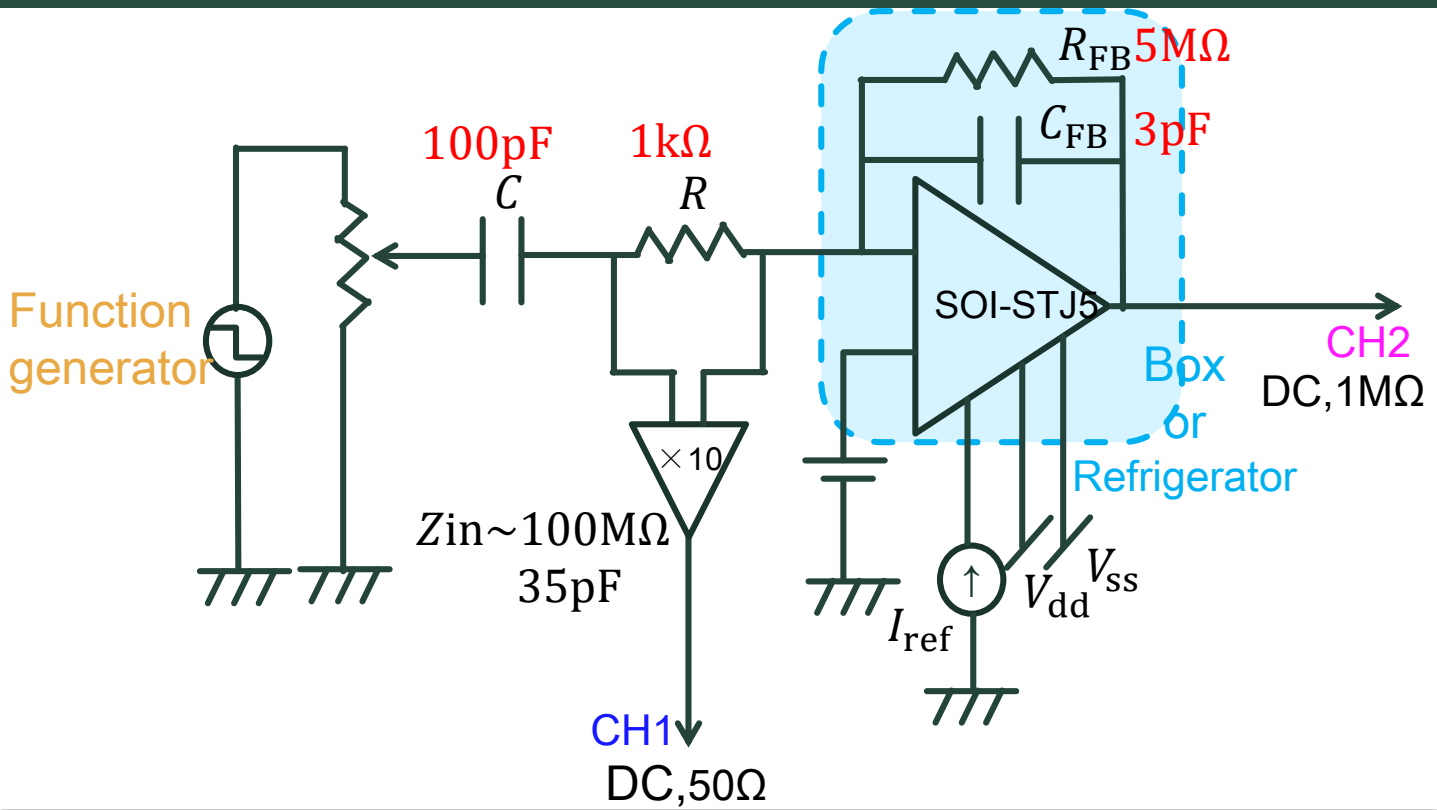
Current Mirror Circuit

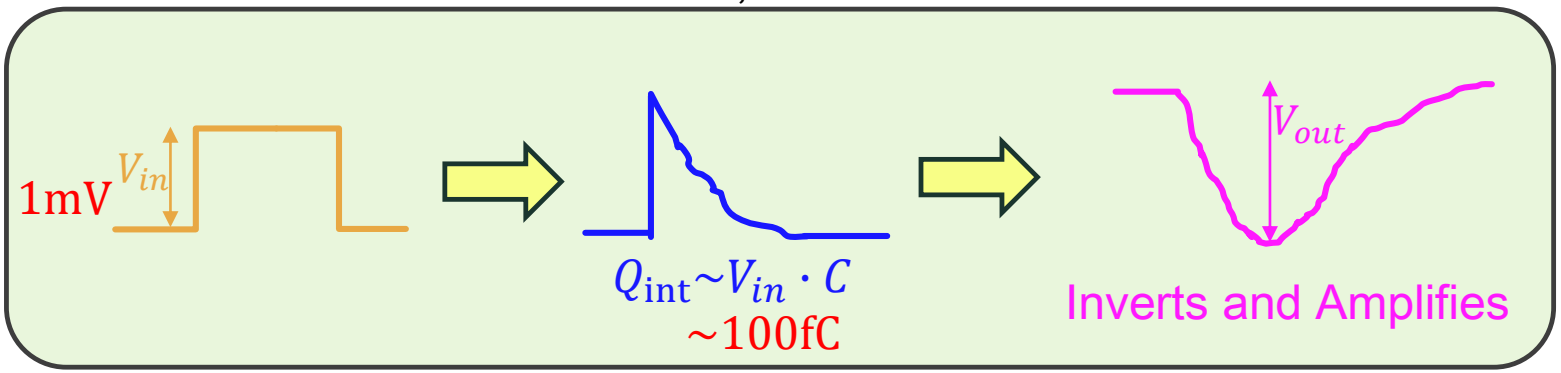
・Cope with array of the detector

・Applying $I_{\mathrm{ref}} = 10\mu\mathrm{A}$, We observe

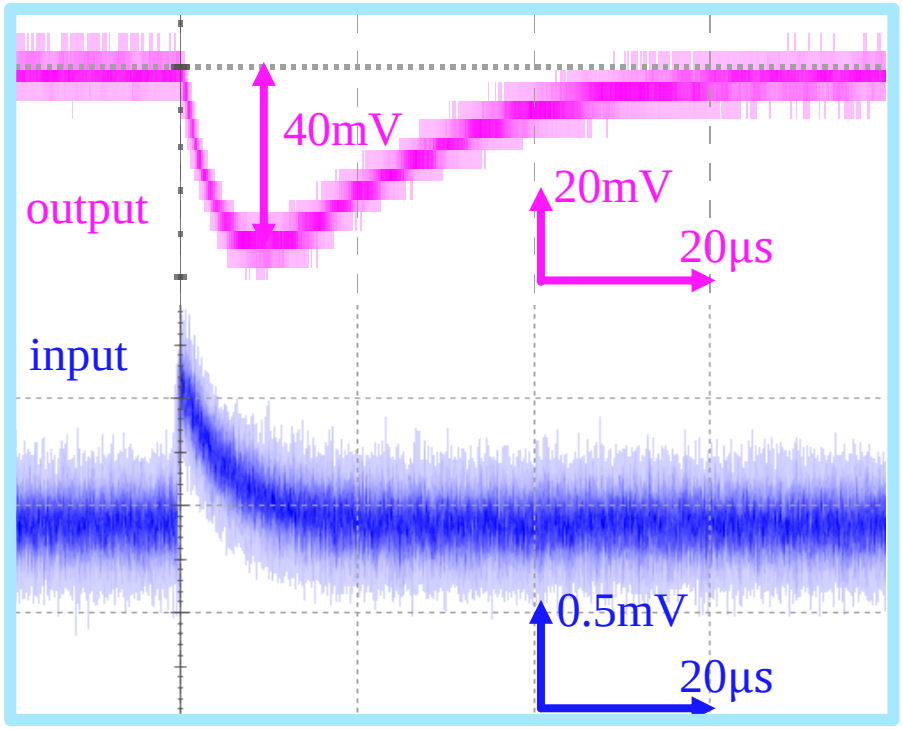
$I_{\mathrm{dd}} = 40\mu\mathrm{A}, I_{\mathrm{ss}} = -50\mu\mathrm{A}$

Test of charge amplification





Result of the test at room temperature



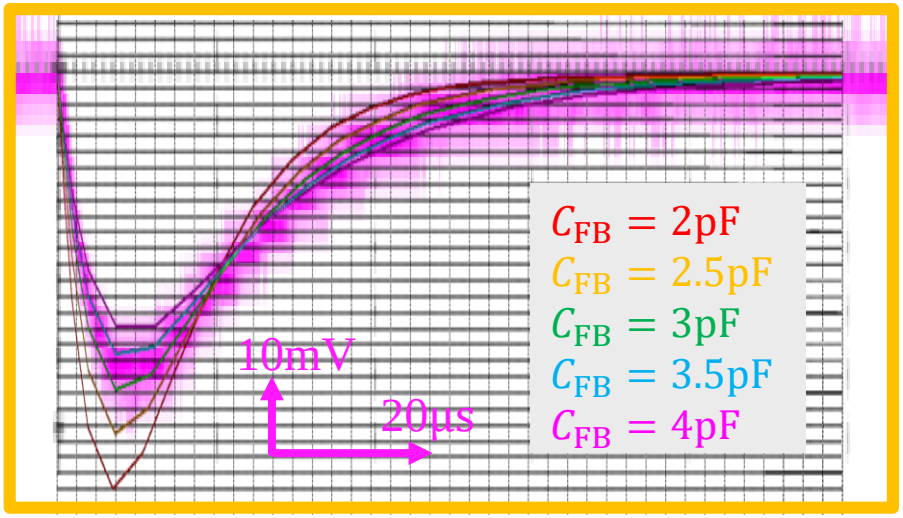
Applied and observed bias

$V_{dd} = 1.5\text{V}$ $\quad I_{dd} = 40.8\mu\text{A}$

$V_{ss} = -1.5\text{V}$ $\rightarrow$ $I_{ss} = -50.2\mu\text{A}$

$I_{ref} = 10\mu\text{A}$ $\quad V_{ref} = -0.555V$

Comparison between Observation and Simulation



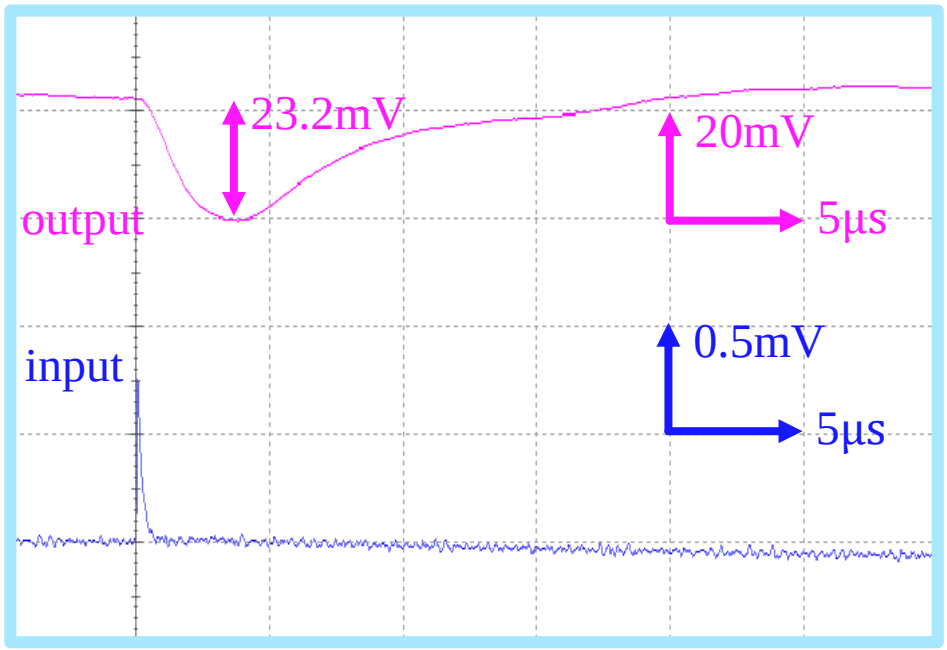
Measurement of Resistance in Feedback

$R_{FB} = 5.36\text{M}\Omega$

This comparison results in $C_{FB} = 3\text{pF}$.

The SOI-STJ5 works correctly!

Result of the test at 3K



※Ave. 1000

- The magnitude of output signal is about 23.2mV.

It is nearly half of the magnitude at room temperature. However, the SOI-STJ5 can amplify the signal charge at 3K!

Applied and observed bias

$V_{\mathrm{dd}} = 1.5\mathrm{V}$ $\quad I_{\mathrm{dd}} = 142.3\mu\mathrm{A}$

$V_{\mathrm{ss}} = -1.5\mathrm{V}$ $\rightarrow$ $I_{\mathrm{ss}} = -151.7\mu\mathrm{A}$

$I_{\mathrm{ref}} = 10\mu\mathrm{A}$ $\quad V_{\mathrm{ref}} = -0.560\mathrm{V}$

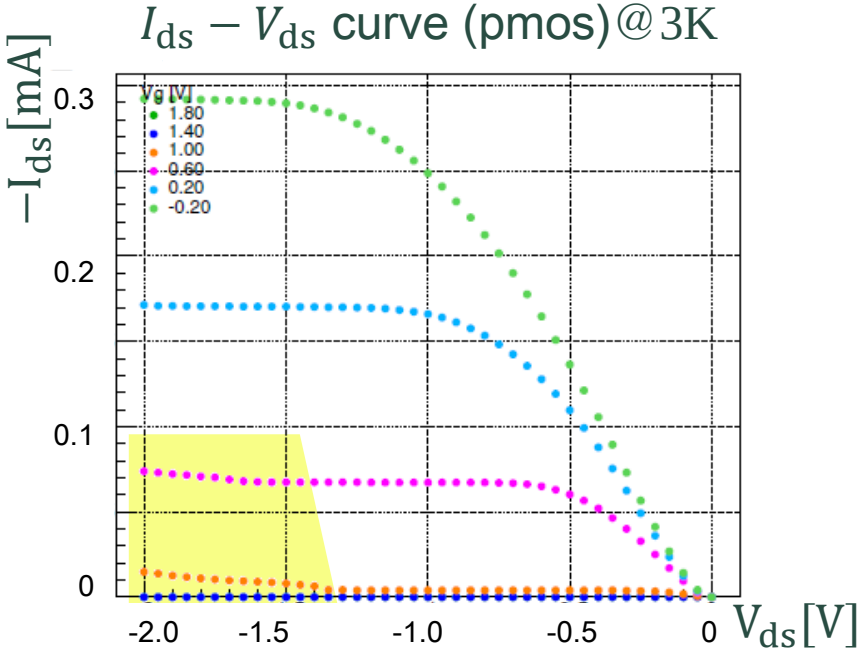
Expected

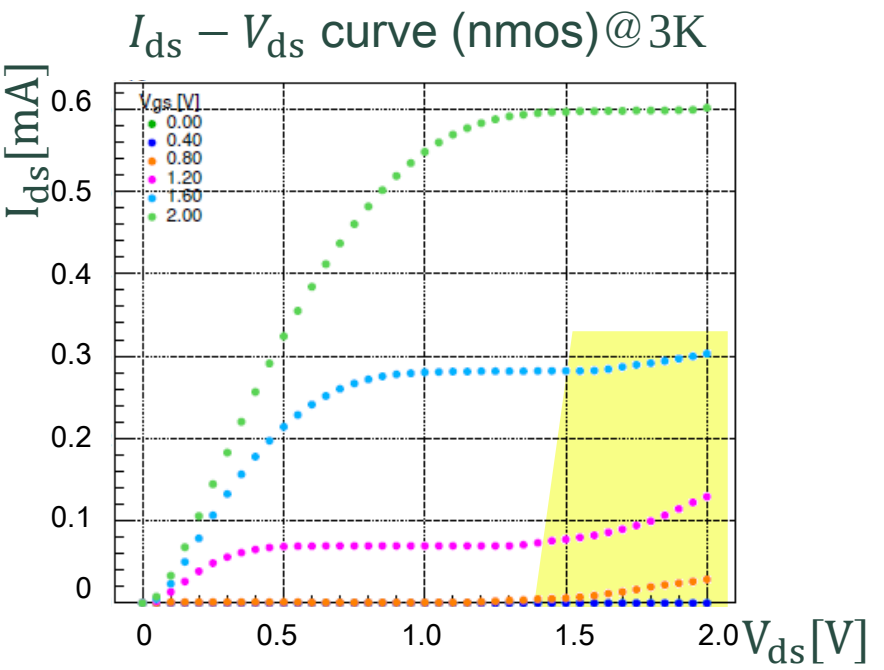
$$I_{\mathrm{dd}} = 40\mu\mathrm{A}$$
$$I_{\mathrm{ss}} = -50\mu\mathrm{A}$$

The current mirror circuit in the SOI-STJ5 didn't work correctly. The reason is increasing drain current I_{ds} in MOSFETs from kink effects.

Kink effect

W/L=10μm/5μm



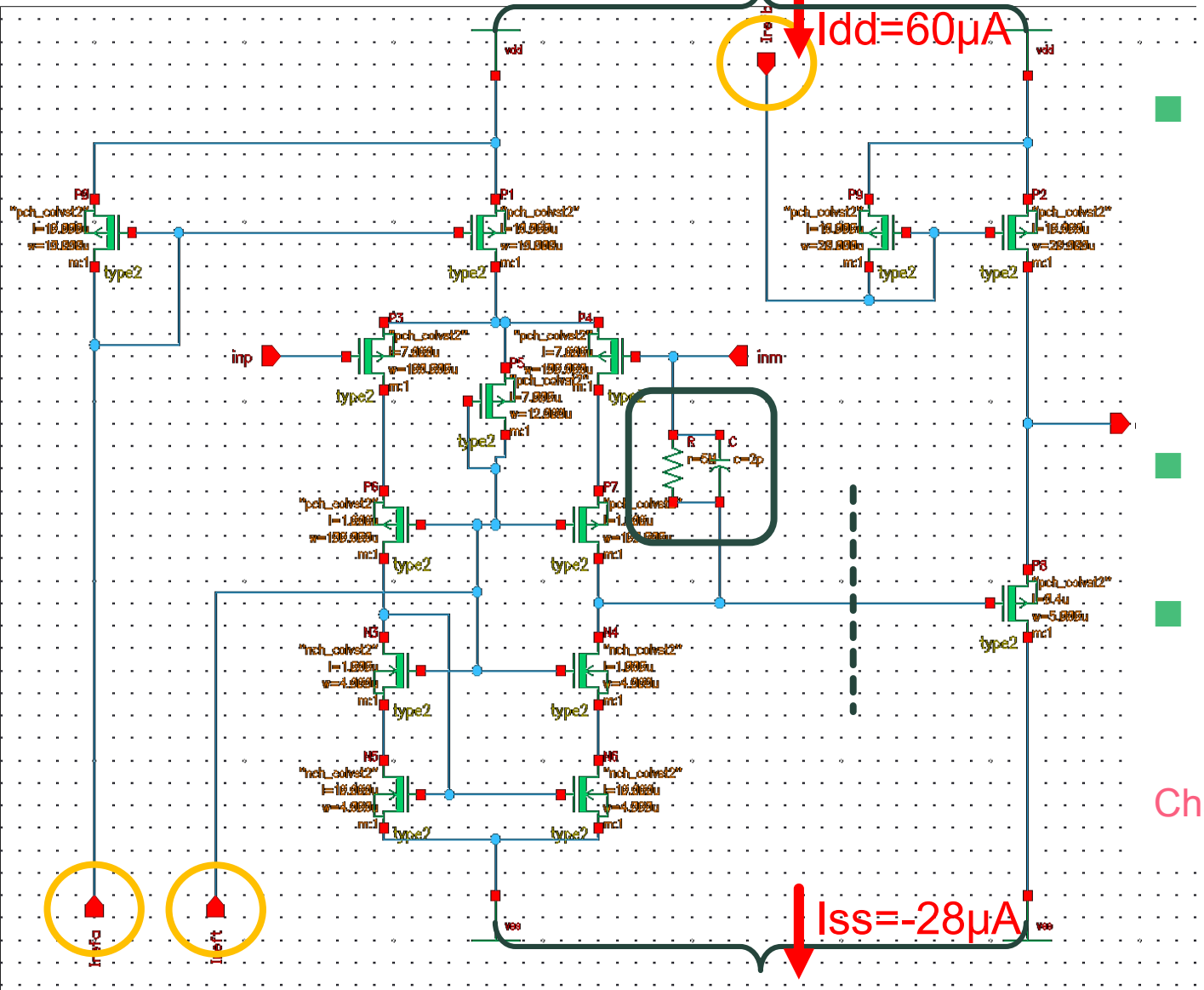


※M_Thesis of Yagi

- I_{ds} is rapidly increasing at $|V_{gs}| < |V_{ds}|$. This property called “kink effect”.
- We found the two MOSFETs are working in these ranges by simulation.

Verify the charge amplification without the bias circuit.

SOI-STJ5 without the bias circuit

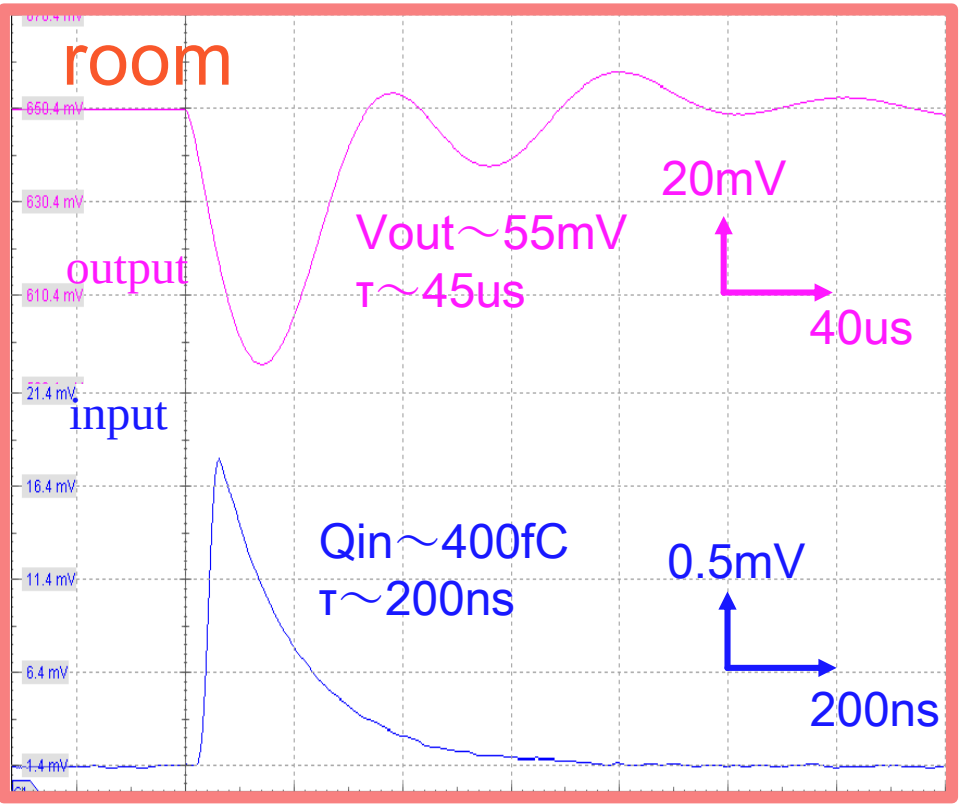


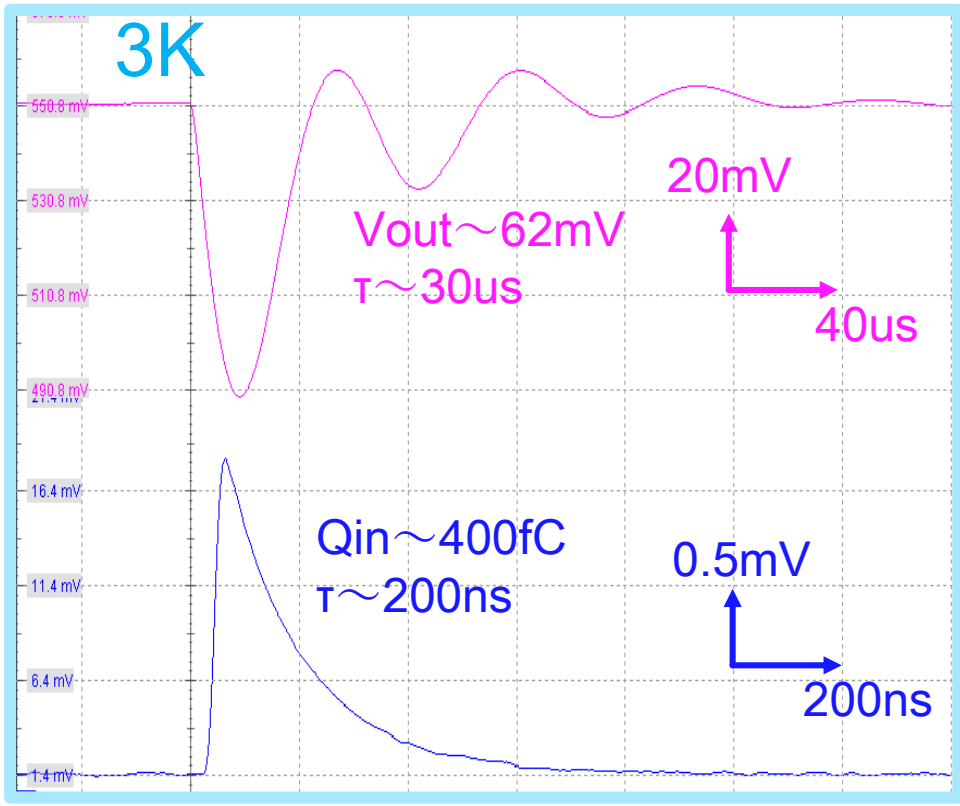
- Applied bias currents
  $I_{\mathrm{refa}} = -10\mu\mathrm{A}$
  $I_{\mathrm{reft}} = -2\mu\mathrm{A}$
  $I_{\mathrm{refb}} = -20\mu\mathrm{A}$
  ↓
  Expected currents
  $I_{\mathrm{dd}} = 60\mu\mathrm{A}$
  $I_{\mathrm{ss}} = -28\mu\mathrm{A}$
- R_{FB} and C_{FB} are on chip. Then they were bonded by Al wires.
- The amplifying stage is bonded to the buffering stage.

↓

Changing the effective C_{FB}

Result of the test without bias circuit





The observed currents

$I_{dd} = 59.4\mu A$

$I_{ss} = -26.8\mu A$

The observed currents

$I_{dd} = 58.7\mu A$

$I_{ss} = -26.2\mu A$

Found similar output signals and currents.

→ Working correctly!!

To improve…

- Cascade connection circuit

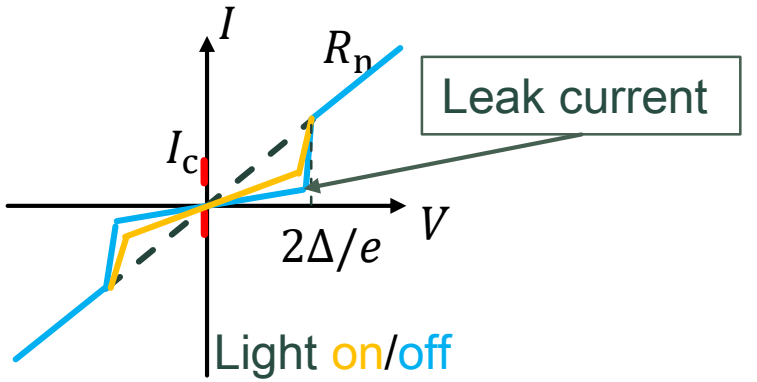
Summary

- To search for neutrino decay, we are researching & developing
  - Superconducting Tunnel Junction (STJ)
  - SOI-STJ (this is an amplifier using FD-SOI-MOSFET which can be operated at cryogenic temperature.)
- We tested the new charge integrating amplifier (SOI-STJ5).
  - We observed the current abnormality at 3K.
  - The abnormality is caused by kink effect.
- In the future
  - Amplifying the signal from STJ by SOI-STJ5 amplifier without bias circuit
  - Introducing the cascade circuit to fix the current abnormality

Backup

STJ
Superconductor Tunneling Junction

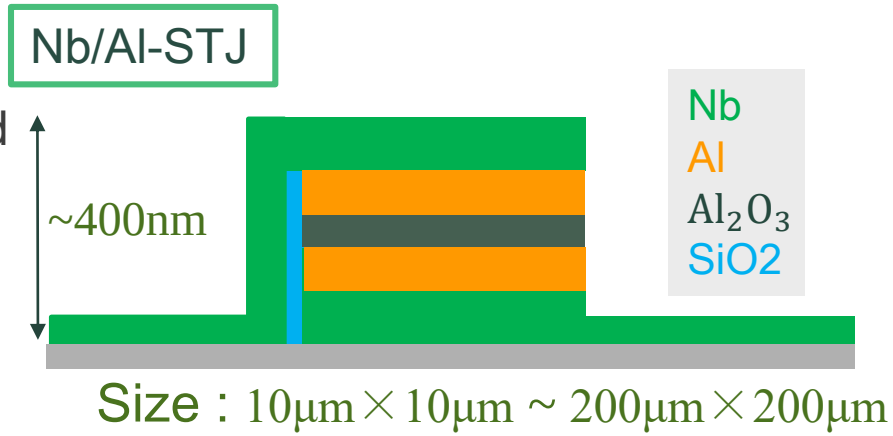
- Working principle of STJ
  - An incident photon breaks cooper pairs into quasi-particles in the superconductor.
  - Applying a bias voltage, the quasi-particle tunnel through insulators, and we can detect the current.



- Nb/Al-STJ
  - The number of quasi-particles generated by 25meV single photon (Al:70nm).

$$N_e = G_{\mathrm{Al}} \cdot \frac{E_\gamma}{1.7\Delta} \sim 250$$

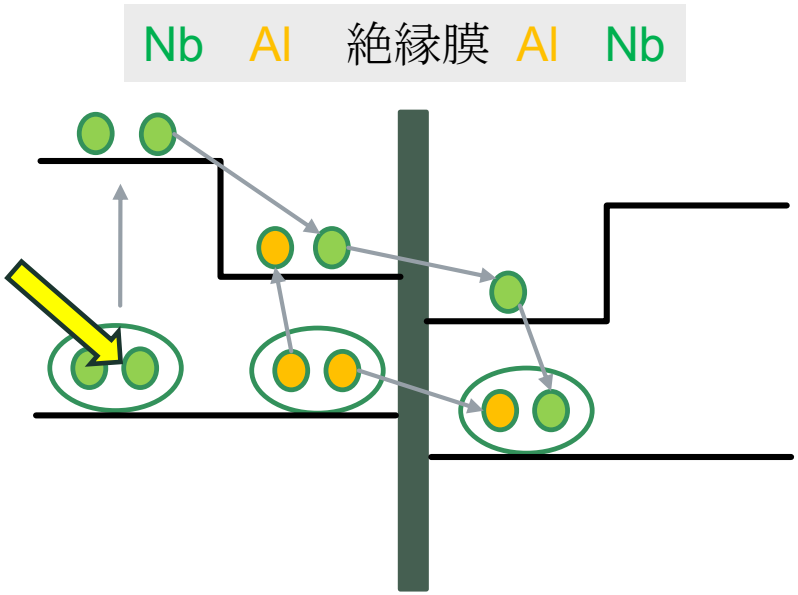
  - The signal width of Nb/Al-STJ is a few micro seconds.
  - Our Nb/Al-STJ is fabricated at AIST CRAVITY facility.



Size : $10\mu m \times 10\mu m \sim 200\mu m \times 200\mu m$

G_{Al}: trapping gain ~10
E_γ: energy of incident photon
Δ: band gap ~0.57meV

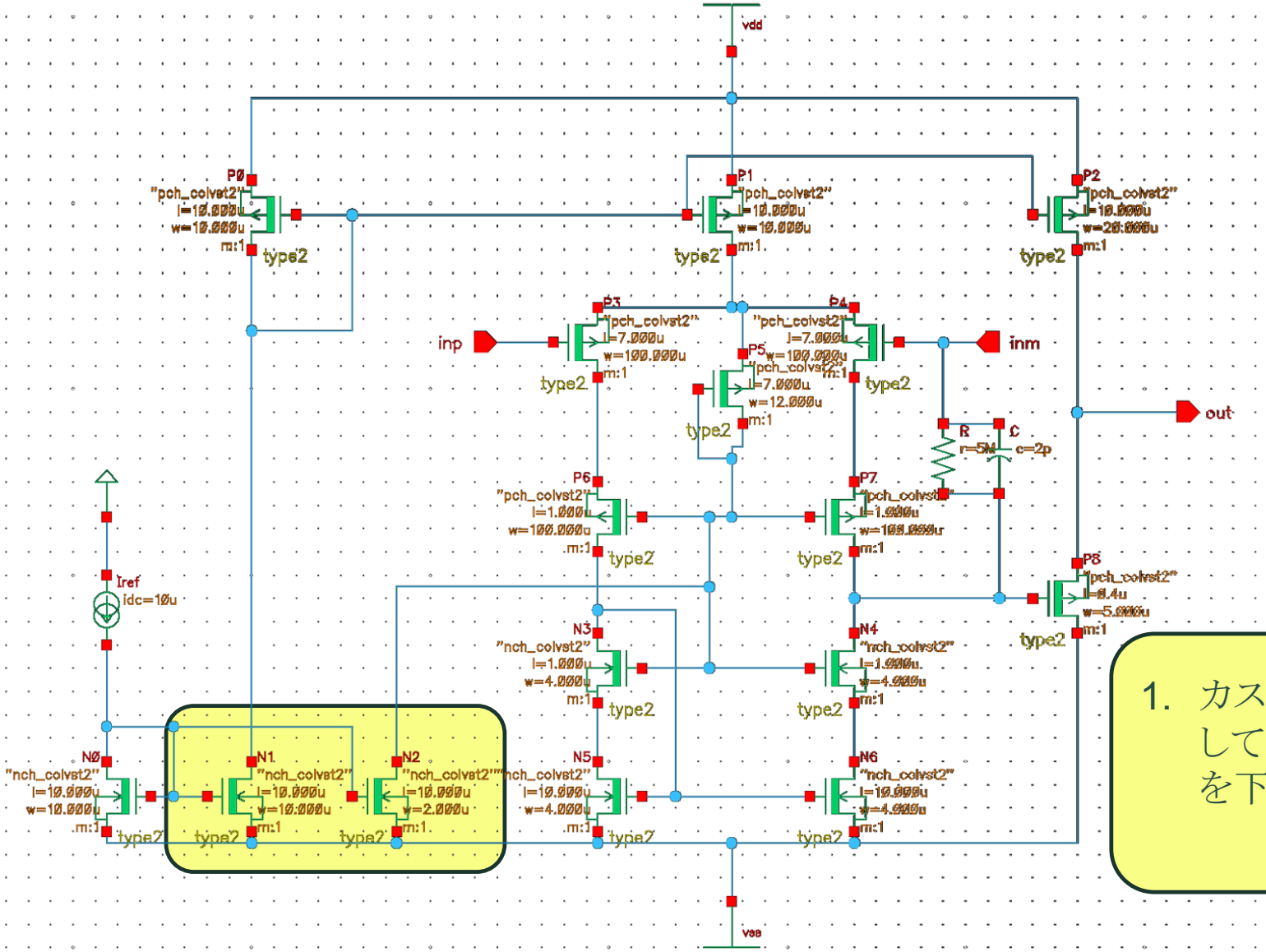
バックトンネリング効果



- バックトンネリングの仕組み
  - ✓ Nb層に光が入射し、クーパー対が励起して準粒子を生成
  - ✓ 生成された準粒子内あるものはそのままトンネル
  - ✓ トンネルしなかった準粒子はAl層での準粒子の存在確率を高める
  - ✓ トンネルした準粒子がAl層のクーパー対の片割れとクーパー対を作る
  - ✓ その際に余った電子が準粒子としてAl層で励起

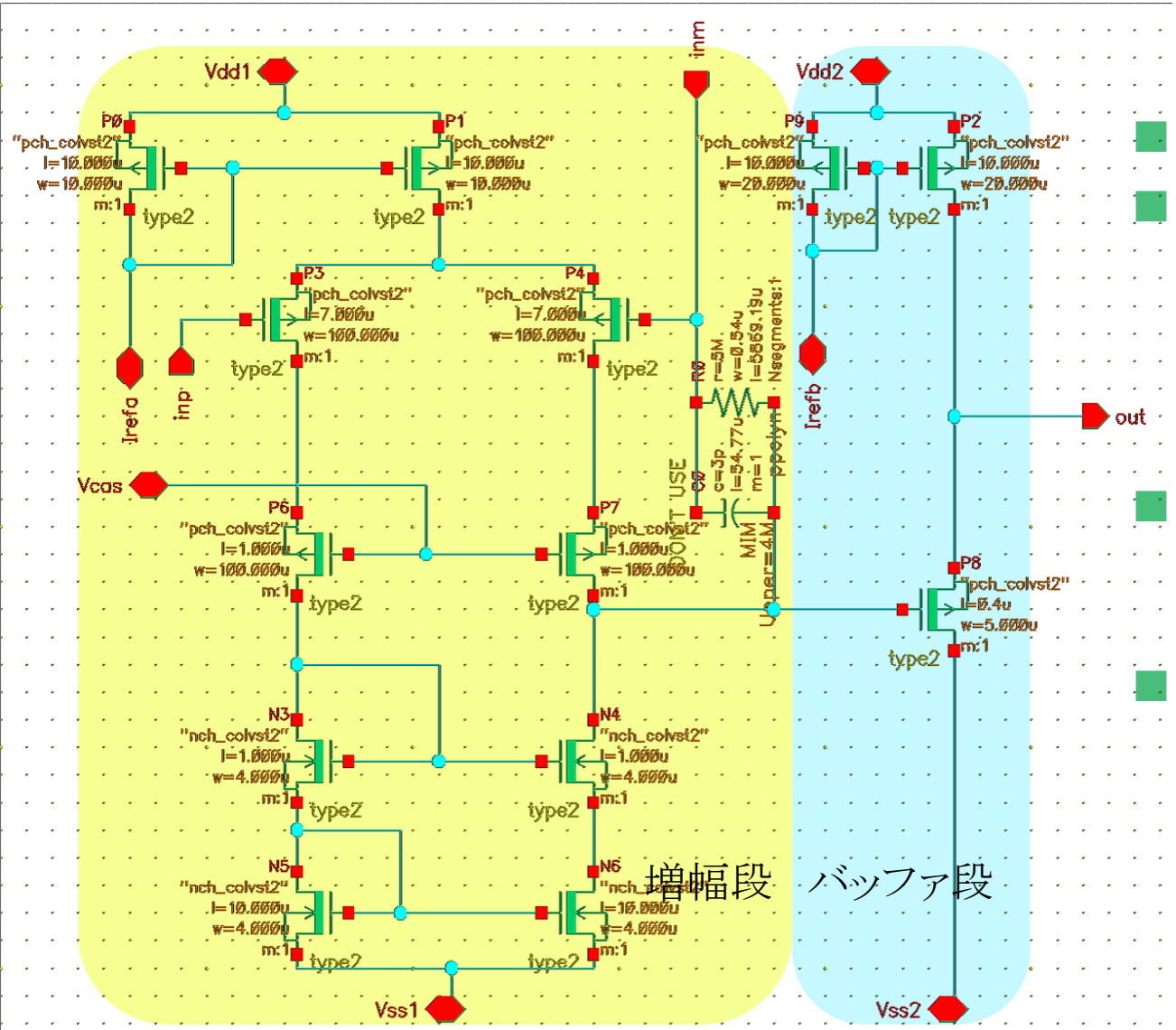
- Nb/Al-STJではG~10

バイアス回路の改良案



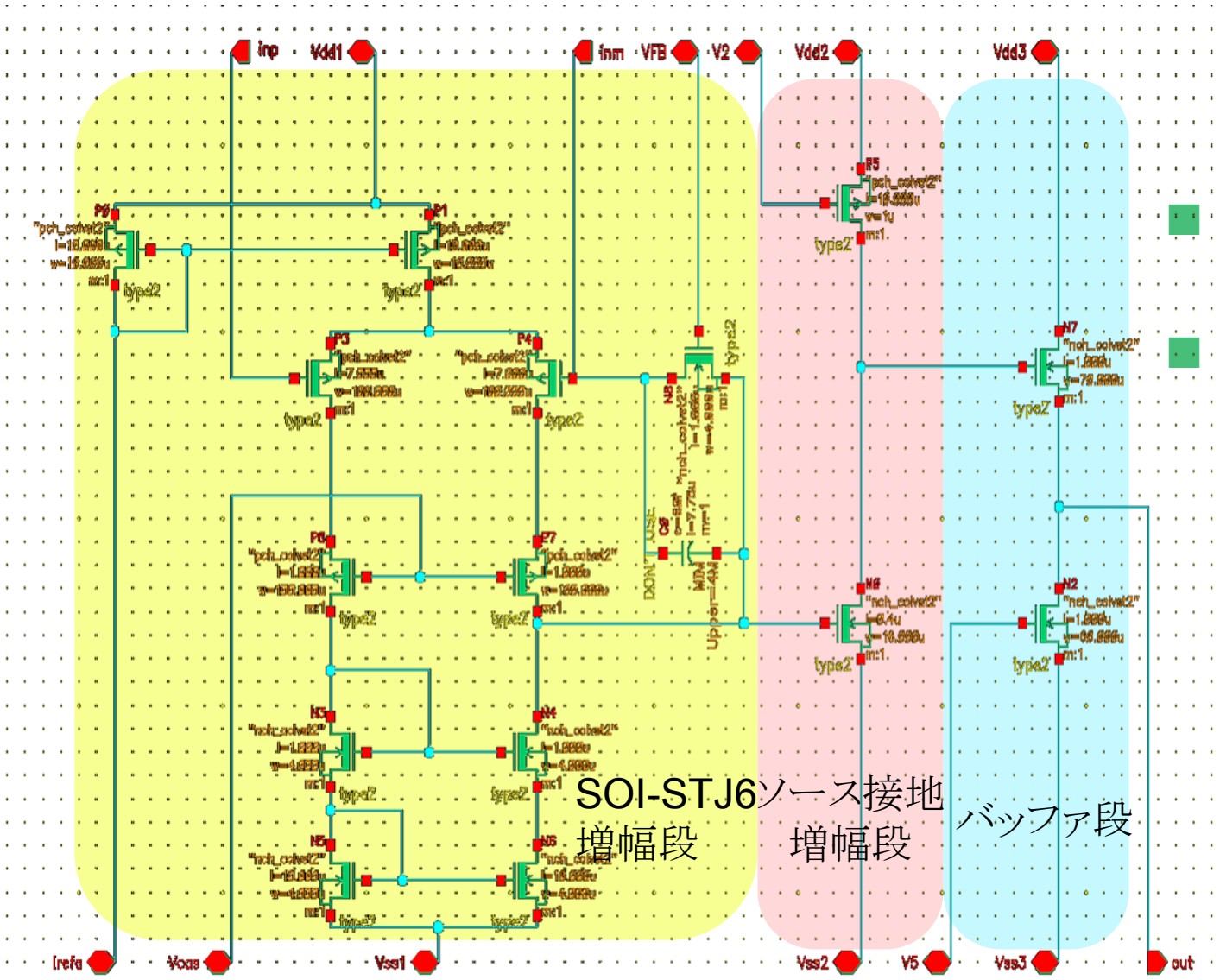
1. カスコード接続にしてドレイン電圧を下げる。

SOI-STJ6の設計



- バイアス回路を削除。
- 消費電力への制限を緩くし増幅段のカスコード部分のダイオード接続の仕方を変更。
  →SOI-STJ5よりもより高い周波数帯域を持つ。
- $V_{dd1} = -V_{ss1} = 2\mathrm{V}$
  $V_{dd2} = -V_{ss2} = 1.5\mathrm{V}$
  で使用予定。
- FBの容量は3pF, 300fF, 60fF
  のものを用意。
  それぞれ時定数が15μsになるよう抵抗 or FETのr_0を調節。

SOI-STJ6+ソース接地増幅回路



- フィードバック容量 60fC
- 25meV, 1光子(0.003fC)に対して3~40mVの出力を得る設計