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Evaluation of test structures for the novel n$^+$-in-p pixel and strip sensors for very high radiation environments

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ABSTRACT

Radiation-tolerant n$^+$-in-p silicon sensors were developed for use in very high radiation environments. Novel n$^+$-in-p silicon strip and pixel sensors and test structures were fabricated, tested and evaluated, in order to understand the designs implemented. The resistance between the n$^+$ implants (interstrip resistance), the electric potential of the p-stop, and the punch-through-protection (PTP) onset voltage were measured before and as a function of fluence after irradiation. The technology computer-aided design (TCAD) simulations were used to understand the radiation damage and fluence dependence of the structures. The decrease in the interstrip resistance is a consequence of increased leakage current. The decrease in the electric potential of the p-stop results from a build-up of positive charge in the silicon–silicon oxide interface. The decrease and subsequent increase in the PTP onset voltages results from the interface charge build-up and an increase in acceptor states.

1. Introduction

We have developed n$^+$ readout in p-type bulk silicon, so called n$^+$-in-p, silicon planar pixel and microstrip sensors with high radiation tolerance. These sensors have applications in high radiation environments such as the high-luminosity large hadron collider (HL-LHC) [1].

The signal readout from n$^+$ implants in p-type bulk has a number of benefits such as collecting electrons, no type-inversion of the bulk (see Section 2), as opposed to conventional p$^+$ readout or n-type bulk sensors. There are, however, issues. The main issue is isolating the n$^+$ implants together with operating at high voltage. The isolation is achieved by a positive ion implantation between the n$^+$ implants. In addition, the pixel and strip sensors require other structures to make them a practical sensor. These include a biasing structure and associated punch-through-protection (PTP) structures.

To work effectively in high radiation environments the structures must be robust against radiation damage and high voltage. Change in behaviors resulting from radiation damage needs to be understood. In this paper, we present experimental results showing the inter-strip resistances, the electric potential of the p-stop implants, and the PTP onset voltages of our structures as a function of fluence of particles. The results are understood using TCAD simulations.

2. n$^+$-in-p sensors and test structures

The radiation species considered in HL-LHC include charged particles (e.g., protons and pions), γs and neutrons. Particle fluence is on the order of 10^{16} 1-MeV neutron equivalent particles per centimeter squared (n_{eq}/cm^2) in charged particles, 3×10^6 Gray dose in γs equivalent, and 5×10^{14} n_{eq}/cm^2 in neutrons. Charged

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particles can cause radiation damage in bulk silicon and at the interface between silicon (Si) and silicon oxide (SiO_2). γs cause radiation damage at the Si–SiO_2 interface and neutrons cause damage in bulk silicon.

n^+-in-p sensors have a number of benefits: n^+-in-p sensors have a high tolerance against radiation damage in their bulk silicon. The radiation damage acts to increase acceptor-like levels, making the p-type bulk to become more p-type [2]. The n^+ implants are always being the p–n junction and collecting electrons. The signals induced in the n^+ implants are larger due to the stronger electric field in the junction, the faster electrons, and reduced trapping of the faster electrons. n^+-in-p sensors are cheaper. Lithographic patterning is required only on the readout side (single-side process). The single-side process allows more foundries and capacity to be available worldwide. Large 6-in. p-type wafers with high resistivity, e.g., >3 kΩ cm, are more readily available in industry than the n-type wafers. n^+-in-p sensors are robust against handling and testing as no lithographic patterning is required on the backside of the sensor.

The major issue of n^+-in-p sensor is isolating the n^+ implants. The interface between the silicon and the silicon oxide (SiO_2) layer becomes positively charged after the sensor-fabrication process and from radiation damage by charged particles or γs. The positive charges at the interface attract negative carriers in the bulk to the surface of the silicon wafer, creating an inversion layer, short-circuit the n^+ implants, and destroy the isolation required for the segmented sensors. A p^+ ion implantation is required to mitigate the inversion layer. This can be made with the form of a confined pattern known as a p-stop structure made by using a mask or with implantation over the wafers known as p-spray. The implantation structure is designed so that breakdown occurs at a higher voltage than the operation bias voltage, e.g., up to 1000 V.

In addition to the specific n^+-in-p structure, the sensor requires other structures to make it useful for practical applications. A biasing structure is needed so that the bias voltage is applied to the implants at high resistance. The high resistance is required to keep the isolation of the implants. For an AC-coupled strip sensor, where the implant is coupled to the readout metal with a capacitor, a protection structure can be integrated to limit the drop of the potential of the implant. When high numbers of charges are deposited into the bulk due to accidental splashing of beam particles into the silicon bulk, a large current is induced, which flows through the bias resistor and generates a large voltage drop at the implant. The readout metal is grounded so a large voltage drop may result in capacitor breakdown. The PTP structure keeps the implant voltage low, by flowing the current though the structure at the bias voltage greater than the PTP onset voltage, avoiding breakdown.

Novel n^+-in-p strip and pixel sensors were fabricated at Hamamatsu Photonics [3] using 6-in., p-type, float-zone, ⟨100⟩ silicon wafers with a resistivity of ~7 kΩ cm and a thickness of 320 μm [4,5]. A number of miniature 1 cm × 1 cm sensors were included for irradiation and testbeam studies along with large 9.75 cm × 9.75 cm area sensors with a 4 segment strip arrangement: two axial strips (1282 strips each, 74.5 μm pitch) and two stereo strips (40 mrad inclined) segments [4]. The miniature sensors were using common or individual p-stop, or p-spray isolation structures and polysilicon resistor biasing structure. A number of ATLAS FE-I3 [6] and FE-I4 [7] ASIC compatible pixel sensors were implemented using p-stop (common- or individual-type) or p-spray isolation structures and a polysilicon resistor biasing structure or a punch-through dot at 4-corner of pixels [5]. A number of test structures were made to investigate the electric potential of the p-stop and the PTP behaviors. These were generated in batch 1 at the positions (30–57, 77–89) and (58–71) (see Fig. 1(a) of Ref. [5]). The typical sample parameters are summarized in Table 1.

Table 1
n^+-in-p silicon sensor test structure parameters.

Parameters	Samples	TCAD (2D)
Silicon wafer		
Wafer type	6-in., p-type, FZ	–
Crystal orientation	⟨100⟩	–
Resistivity	~7 kΩ cm	–
Doping concentration	–	4.7×10^{12} cm^{-3}
Thickness	320 μm	150 μm
Basic geometry		
Strip pitch	74.5 μm	74.5 μm
Readout metals	AC coupled, grounded	AC coupled, grounded
Readout metal width	22 μm	22 μm
n^+-implants	Grounded through bias resistance	Grounded
n^+-implant width	16 μm	16 μm
Isolation	Common p-stop	Common p-stop
p-stop	~4×10^{12} cm^{-2}	4×10^{12} cm^{-2}
P-stop width	6 μm	6 μm
Bias resistance	~1.5 MΩ	–
Geometries of the electrical potential of the p-stop		
Isolation	Common or Individual p-stop	–
Strip pitch	30–100 μm	–
Geometries of the PTP		
n^+(strip)–n^+(bias rail) distance	20 μm	20 μm
p-stop width	6 μm	6 μm
Field plate	Grounded	Grounded
Field plate coverage	No or full	No or full

3. Test structure measurements

3.1. Irradiation at CYRIC

The test structures were irradiated with 70 MeV protons at Cyclotron and Radioisotope Center (CYRIC) [8], using the 32 course and fluences of 5.2×10^{12}, 1.1×10^{13}, 1.2×10^{14}, 1.2×10^{15}, 1.2×10^{16} n_{eq}/cm^2 [9] and 1.1×10^{14}, 1.2×10^{15}, 5.7×10^{15}, 1.2×10^{16} n_{eq}/cm^2 [10]. The irradiations were carried out in an irradiation box, cooled to approximately −10 °C inside. A number of test structures, 5–10 pieces, were grouped and stacked using paper and polyimide sheets as separators, and wrapped with polyimide films. Because of this arrangement, little cooling was expected, despite the assembly being placed in the cooled environment. During the irradiation, the samples increased in temperature. Melting of the polyimide sheets was observed for samples irradiated at a fluence of 10^{16} n_{eq}/cm^2. After the irradiation the samples were kept in a freezer at −20 °C.

3.2. Interstrip resistance

The resistance between the strips, the interstrip resistance (R_{int}), was measured using one of the miniature sensors, which had a strip pitch of 74.5 μm and a common p-stop 6 μm wide. The electric potential of the center strip V^0 was varied between ±5 V. The potential of the two adjacent neighbors that were shorted externally V^1) was measured while changing the potential of the backplane V^b. The interstrip resistance was calculated using the following equation:

$$R_{int} = R_b(V_0 - V_1)/V_1 \quad (1)$$

where R_b is the resistance of the bias resistor. R_b was measured to be ~1.5 MΩ. The interstrip resistances calculated for the non-irradiated samples and for samples irradiated at fluences of up to 1.2×10^{15} n_{eq}/cm^2 are shown in Fig. 1. The interstrip resistance is plotted as a function of bias voltage. The resistance of the

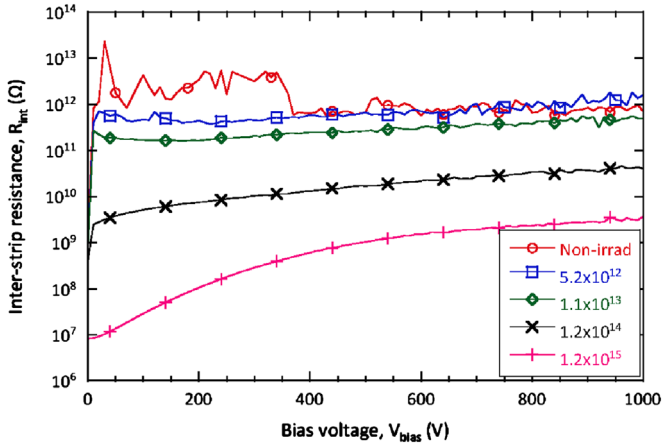

Fig. 1. Interstrip resistance as a function of bias voltage for non-irradiated samples (circle) and samples irradiated at 5.2×10^{12} (square), 1.1×10^{13} (diamond), 1.2×10^{14} (cross), and 1.2×10^{15} (plus).

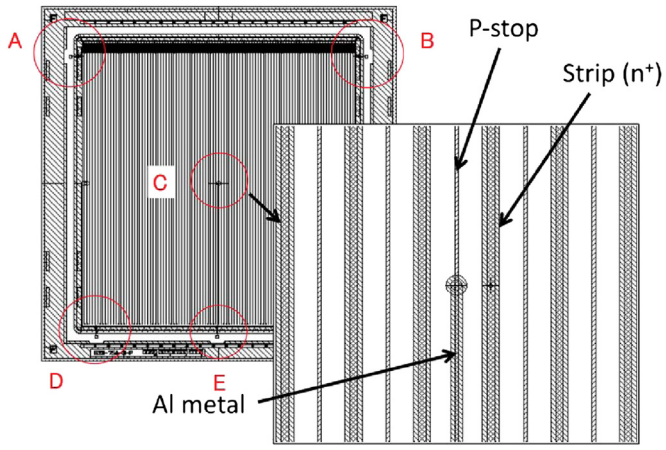

Fig. 2. Schematic diagram of the miniature sensor used to measure the electric potential of the p-stop. The inset shows the metal probe connection of the center-probe point.

non-irradiated sample is seen to fluctuate. This fluctuation is most likely due to an unknown noise source, since V^1 was typically on the order of μV. The interstrip resistance is seen to decrease from ~1000 GΩ to ~1 GΩ as the fluence increases.

3.3. Electric potential of the p-stop

The electric potential of the p-stop was measured using test structures with both common and individual p-stops with various strip pitches. An example of the test structure used is shown in Fig. 2. Integrated probing contact is shown in the inset. Measurements were made using a digital voltmeter and a tera-ohm resistor. The measured electric potential values of the p-stops are shown in Fig. 3. The backplane bias voltage was −500 V. For non-irradiated samples the potential increases with increasing pitch width and a larger potential is observed for individual p-stops compared to common p-stops. For increasing fluence, the potential is seen to decrease and eventually saturates between 30 and 40 V.

3.4. PTP onset voltage

The PTP onset behavior has been measured in various PTP structures [11,12]. The classical PTP structure is to have a gap between the bias-rail implantation (n^+) and the strip implantation

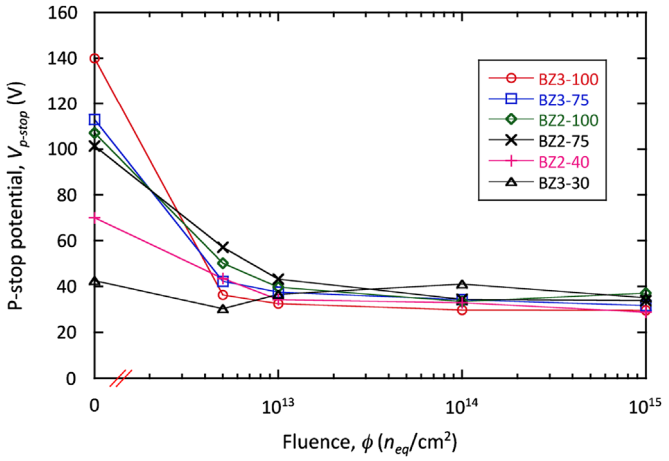

Fig. 3. Electric potential of the p-stop as a function of fluence for a strip pitch and p-stop isolation of 100 μm and common (BZ3-100, circle), 75 μm and common (BZ3-75, square), 30 μm and common (BZ3-30, triangle), 100 μm and individual (BZ2-100, diamond), 75 μm and individual (BZ2-75, cross), 34 μm and individual (BZ2-40, plus). The backplane bias voltage is −500 V.

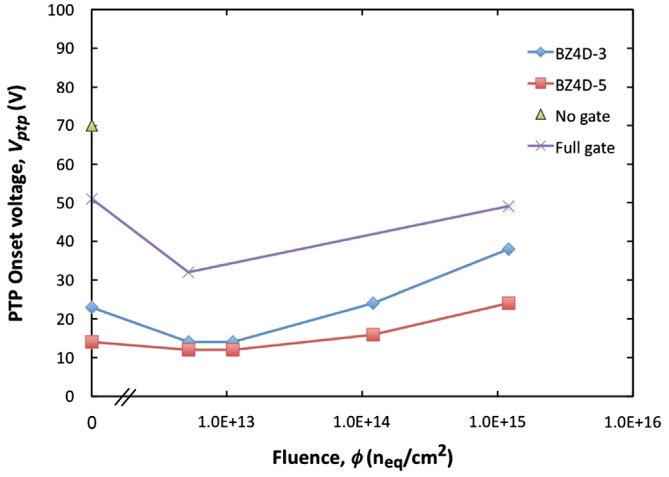

Fig. 4. PTP onset voltage as a function of fluence for BZ4D-3 (no-gate, diamond) and BZ4D-5 (full-gate, square) structures, and TCAD simulations with no-gate (non-irradiated; triangle) and full-gate (3 points of NB∗LT∗LC, NB∗HT∗LC, and DB∗HT∗HC; cross) structures.

(n^+) small enough that the voltage difference between the two implantations results in a current flow above the punch-through onset voltage. Our novel PTP structure has an added field-plate, which goes from the bias-rail over the PTP gap. This enhances the electric field in the PTP structure due to the electric potential of the bias-rail: a gate effect. The variation of the onset voltage as a function of the fluence is shown in Fig. 4. The BZ4D-3 sample is the classical PTP structure with no field plate (no gate). The BZ4D-5 sample is the novel PTP structure with a field plate covering the whole PTP gap (full gate). The results show that PTP onset voltage decreases by almost half when the field plate is added. The same results are seen both before and after irradiation. This shows that the novel PTP structure is effective in inducing onset at lower voltages. As the fluence increases the PTP onset voltage decreases first and then increases once the fluence reaches approximately 1×10^{13} n_{eq}/cm^2.

4. TCAD simulations

Semiconductor industries have developed sophisticated semiconductor process and device simulation systems [11]. The

simulation systems are known as Technology Computer-Aided Design (TCAD) tools and are based on finite element methods. We used the simulation tool, Environment for Exploration of Semiconductor Simulation version 5.5 (ENEXSS 5.5) [13]. ENEXSS does not include a microscopic model to simulate the irradiated silicon devices. Instead, the effective characteristics of the irradiated silicon are approximated: (1) The increase in acceptor state with increasing Boron doping concentration (N_{eff}). The doping concentration N_{eff} defines the resistivity of bulk silicon, which is the resistance of the non-depleted silicon bulk. (2) The increase in leakage current with increasing generation–recombination rate. This is simulated by tuning the parameters (A_n and A_p) of the generation–recombination model. (3) The increase in interface charge with increasing interface fixed charge (Q_{fix}). The TCAD parameters used to approximate the non-irradiated and irradiated (~1×10^{15} n_{eq}/cm^2) silicon devices are summarized in Table 2. The TCAD simulations were made for 2-dimensional cross-section of the device with a thickness of 1 μm. For simulations, mainly the basic geometry described in Table 1 was used. The bias voltage of the backplane was set to −200 V.

4.1. Shockley–Reed–Hall model

In the ENEXSS simulations, the continuity equations of the electron and hole current densities, J_n and J_p, are given by

$$\frac{\partial n}{\partial t} - \mathrm{div}\left(\frac{\mathbf{J}_n}{q}\right) = U, \frac{\partial p}{\partial t} - \mathrm{div}\left(\frac{\mathbf{J}_p}{q}\right) = U \quad (2)$$

The generation–recombination term U given by the Shockley–Reed–Hall (SRH) model [14] is given by

$$U_{SRH} = \frac{n_i^2 - np}{\tau_p(n + n_i) + \tau_n(p + n_i)} \quad (3)$$

where

$$\tau_n \propto A_n, \quad \tau_p \propto A_p \quad (4)$$

and n, p, and n_i are the electron, hole, and intrinsic carrier densities, respectively. A_n and A_p are scaling parameters.

Table 2
TCAD parameters used to simulate the non-irradiated and irradiated conditions.

Parameters	Non-irradiated	Irradiated
Doping concentration (N_{eff})	4.7×10^{12} cm^{-3}	1.5×10^{13} cm^{-3}
Leakage current (SRH A_p,A_n)	1.0	1×10^{-8}
Interface fixed charge (Q_{fix})	1×10^{10} cm^{-2}	1×10^{12} cm^{-2}

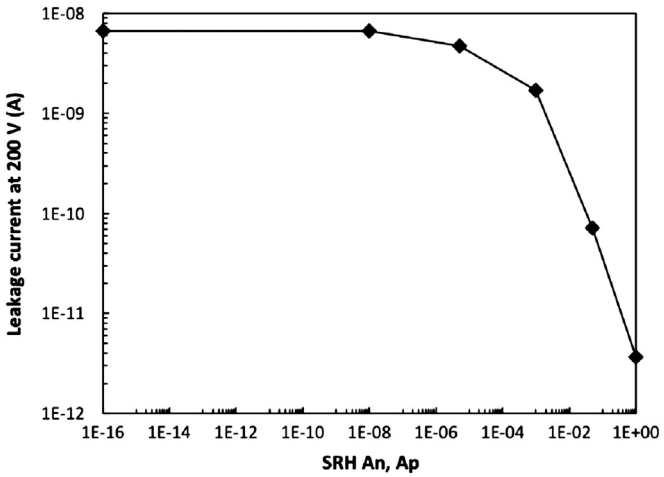

Fig. 5. TCAD simulated leakage current as a function of the A_n and A_p SRH scaling parameters.

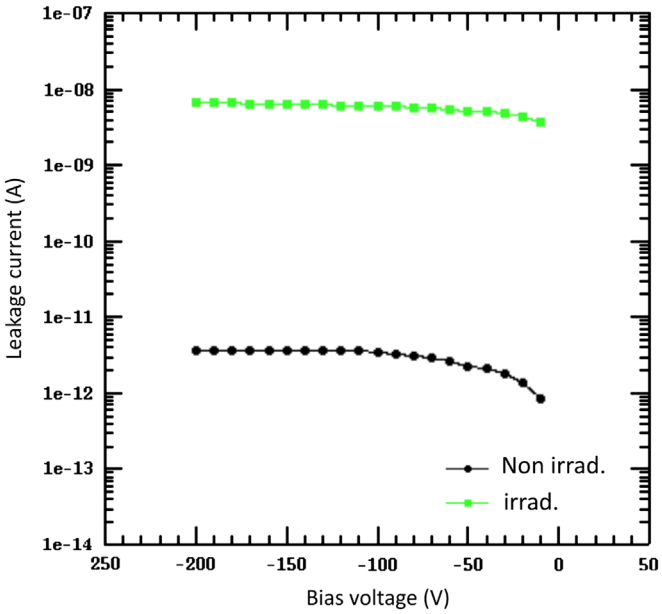

Fig. 6. TCAD simulated leakage current as a function of bias voltage for the non-irradiated and irradiated conditions.

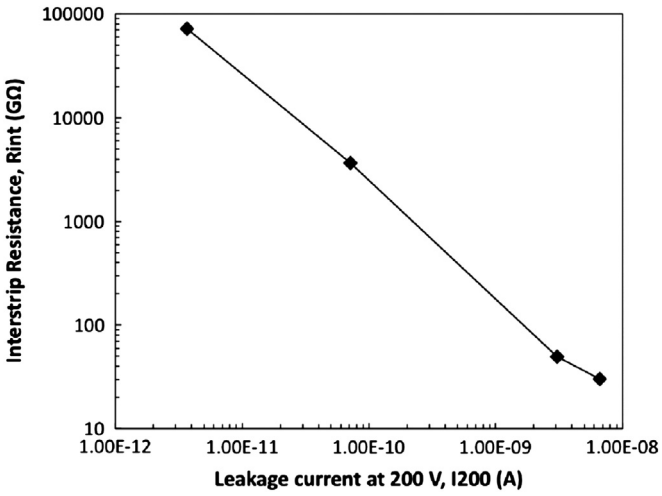

Fig. 7. TCAD simulated interstrip resistance as a function of leakage current.

The variation in the leakage current as a function of the parameters A_n and A_p is shown in Fig. 5. The leakage currents varies by 3 orders of magnitude when A_n and A_p are decreased from 1.0 to 1×10^{-8}. The current saturates at A_n and A_p below ~1×10^{-8}. The simulated leakage current as a function of bias voltage is shown in Fig. 6. Both non-irradiated and irradiated TCAD conditions were simulated using the parameters in Table 2 and the interstrip resistance geometry in Table 1.

4.2. Interstrip resistance

The interstrip resistances R_{int} were simulated for both the non-irradiated and irradiated conditions. In addition, simulations were carried out for conditions with slightly less leakage current. The result is shown in Fig. 7. The interstrip resistance decreases by 2 orders of magnitude from the non-irradiated to irradiated conditions. No decrease in the interstrip resistance is observed if only the doping concentration or the interface charge is varied. The decrease in the interstrip resistance therefore results from an

increase in the leakage current due to the radiation damage of bulk.

4.3. Electric potential of the p-stop

The 2-dimensional distribution of electric potential for both non-irradiated and irradiated conditions is shown in Fig. 8. The two simulations have distinctive difference. The potential is more concentrated toward the n^+ implants for the non-irradiated conditions (Fig. 8(a)) and more uniform between the n^+ implants for the irradiated conditions (Fig. 8(b)). The difference is caused by the amount of interface charge Q_{fix}, $1\times10^{10}\,cm^{-2}$ in the non-irradiated and $1\times10^{12}\,cm^{-2}$ in the irradiated conditions. In the irradiated condition, an electron inversion layer is seen at the Si–SiO_2 interface everywhere except in the vicinity of the p-stop. This resistive inversion layer extends the electric potential between the n^+ implants. The electric potential between the implants is shown in Fig. 9. The result for the irradiated condition but with negative interface charge of $Q_{fix}=-1\times10^{12}\,cm^{-2}$ is also shown. The results suggest that the decrease in the electric potential of the p-stop comes from the increase in the interface charge that is positive.

4.4. PTP onset voltage

In 2-dimensions, the PTP structure is very similar to the basic geometry. In the PTP structure, the distance between the n^+-implants of 20 μm was used. The bias rail structure was set in the right-hand n^+-implant. The metal over the implant was connected directly to the implant (DC metal). The field plate was made by extending the DC metal toward the left-hand n^+-implant over the surface SiO_2. No bias resistor was integrated in parallel to the PTP gap. The PTP behavior was simulated by varying the electric potential V_{test} of the left-hand implant from 0 V to −200 V, while maintaining the backplane bias voltage at −200 V.

TCAD simulations were carried out with and without the field plate. These are labeled as full-gate and no-gate, respectively. The three parameters used to model the radiation damage were individually set using the following parameter values: For low (NB) and high (DB) silicon bulk damage N_{eff} was set to $4.7\times10^{12}\,cm^{-3}$ and $1.5\times10^{13}\,cm^{-3}$, respectively. For low (LT) and high (HT) interface change Q_{fix} was set to $1\times10^{10}\,cm^{-2}$ and $1\times10^{12}\,cm^{-2}$, respectively. For low (LC) and high (HC) leakage

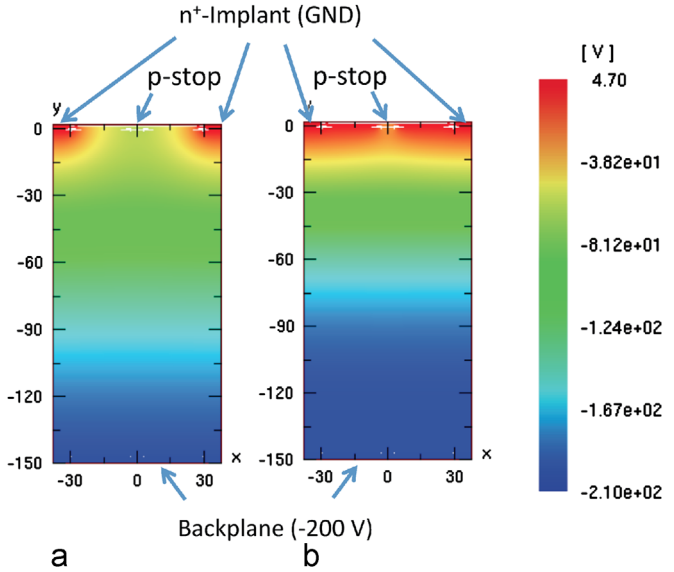

Fig. 8. TCAD simulated electric potential distributions for (a) non-irradiated and (b) irradiated conditions.

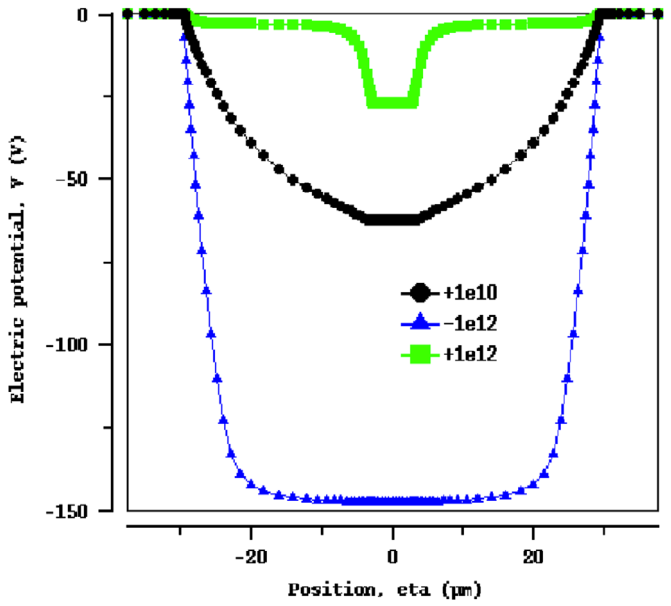

Fig. 9. TCAD simulated electric potential of the p-stop for non-irradiated ($Q_{fix}=+1\times10^{10}\,cm^{-2}$, circle) and irradiated ($Q_{fix}=+1\times10^{12}\,cm^{-2}$, square and $-1\times10^{12}\,cm^{-2}$, triangle) conditions.

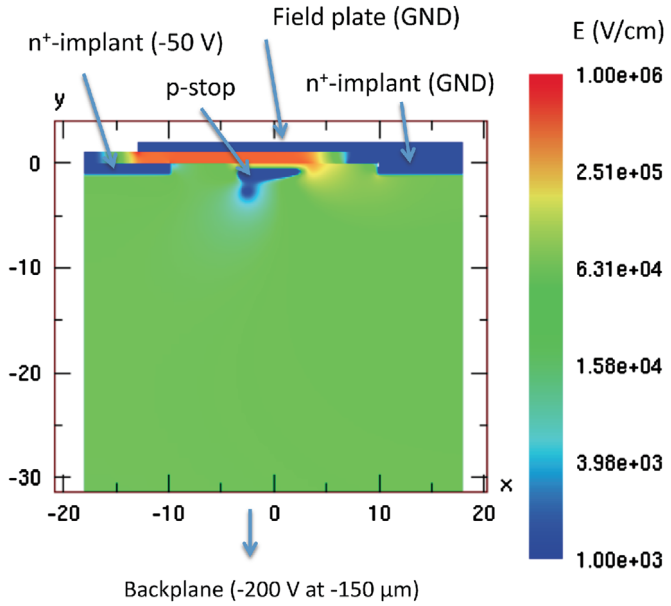

Fig. 10. TCAD simulated electric field distribution of the PTP structure with a full-gate field plate for irradiated condition at an onset voltage of −50 V.

current A_n and A_p were both set to 1.0 and 1×10^{-8}, respectively. The non-irradiated and irradiated ($1\times10^{15}\,n_{eq}/cm^2$) conditions were NB*LT*LC and DB*HT*HC, respectively. At low fluence the increase in interface charge is the dominant factor. The NB*HT*LC may correspond to the low fluence point, e.g., $5\times10^{12}\,n_{eq}/cm^2$.

An example of the 2-dimensional electric field distribution at V_{test} of −50 V for the full-gate and irradiated simulations is shown in Fig. 10. The PTP has just been turned on. The breakdown occurs at the highest electric field at the right-hand edge of the p-stop. The PTP behavior is shown in Fig. 11. The PTP onset voltage is defined as the voltage at the corner where the current starts to increase rapidly. For the no-gate and non-irradiated condition (NPTP) the onset voltage is around 70 V. For the full-gate and non-irradiated (NB*LT*LC) the onset decreases to around 50 V. Increasing the interface charge (NB*HT*LC) further reduces the onset to

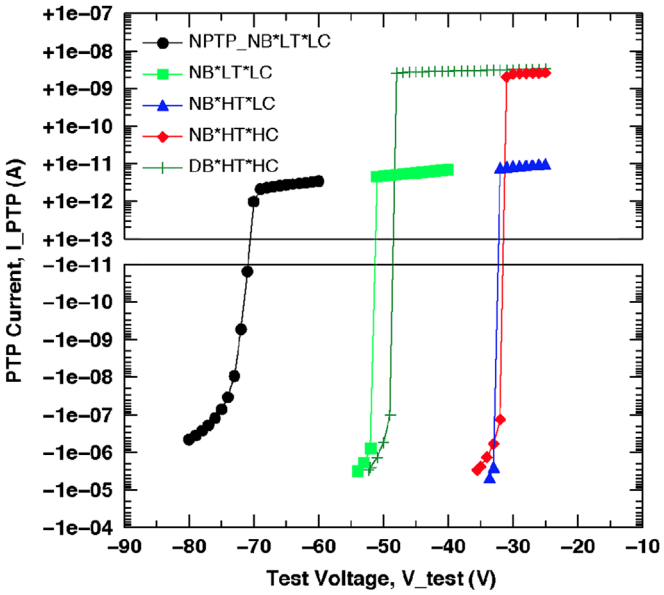

Fig. 11. TCAD simulated onset behavior of the PTP structures. (NPTP) non-irradiated without a field plate. (NB∗LT∗LC) non-irradiated with a full-gate field plate, (NB∗HT∗LC) non-irradiated full-gate with a high interface charge, (NB∗HT∗HC) irradiated full-gate with no bulk damage, and (DB∗HT∗HC) irradiated full-gate.

around 30 V. Increasing the leakage current (NB∗HT∗HC) has no effect on the onset voltage. Increasing the bulk damage (DB∗HT∗HC) increases the onset voltage to around 50 V. The simulated onset voltages are plotted in Fig. 4 as a function of fluence. The decrease and subsequent increase in the onset voltage as a function of increasing fluence result from a build-up of the interface charge followed by the increase in the acceptor states. The systematic offset of the onset voltages between the experimental measurements and the TCAD simulations are thought to be a result of the difference of the 3-dimensional devices and the 2-dimensional simulations.

5. Summary

We have developed radiation-tolerant n^+-in-p silicon sensors for use in high radiation environments. Novel n^+-in-p silicon strip and pixel sensors and test structures were fabricated, tested, and evaluated in order to understand the basic characteristics of the designs implemented. The resistance between the n^+ implants, the electric potential of the p-stop, and the PTP onset voltages were measured as a function of fluence. Radiation damage was approximated in the TCAD device simulations by increasing the acceptor states, increasing the interface charge, and increasing the leakage current. The increase in the leakage current was tuned using the Shockley–Reed–Hall model for the generation–recombination of electron–hole carriers. The TCAD simulations were used to understand the fluence dependencies of the devices. The decrease in the interstrip resistance is a consequence of an increase in the leakage current. The decrease in the electric potential of the p-stop results from a build-up in the positive interface charge. The decrease and subsequent increase in the PTP onset voltages result from the interface charge build-up and an increase in the acceptor states.

Acknowledgments

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