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Monolithic pixel detectors with 0.2 μm FD-SOI pixel process technology

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ABSTRACT

Truly monolithic pixel detectors were fabricated with 0.2 μm SOI pixel process technology by collaborating with LAPIS Semiconductor Co., Ltd. for particle tracking experiment, X-ray imaging and medical applications. CMOS circuits were fabricated on a thin SOI layer and connected to diodes formed in the silicon handle wafer through the buried oxide layer. We can choose the handle wafer and therefore high-resistivity silicon is also available. Double SOI (D-SOI) wafers fabricated from Czochralski (CZ)-SOI wafers were newly obtained and successfully processed in 2012. The top SOI layers are used as electric circuits and the middle SOI layers used as a shield layer against the back-gate effect and cross-talk between sensors and CMOS circuits, and as an electrode to compensate for the total ionizing dose (TID) effect. In 2012, we developed two SOI detectors, INTPIX5 and INTPIX3g. A spatial resolution study was done with INTPIX5 and it showed excellent performance. The TID effect study with D-SOI INTPIX3g detectors was done and we confirmed improvement of TID tolerance in D-SOI sensors.

1. Introduction

A monolithic silicon pixel detector made in one process is an ideal tool for X-ray and charged particle detection. A monolithic can be realized by utilizing SOI wafers. The development project of SOI monolithic pixel detectors started in 2005 as a Detector Technology Project (DTP) of the High Energy Accelerator Research Organization (KEK). The fabrication was made with 0.2 μm Fully Depleted (FD) SOI CMOS process at Lapis Semiconductor Co., Ltd. Since 2005, many prototype detectors using SOI technology have been developed [1–4]. The SOI detectors consist of two silicon layers and Buried OXide (BOX) between them. The SOI wafer is fabricated from two silicon wafers by using SmartCut™ by SOITEC. Since we can choose the initial silicon wafers, a low resistivity silicon is used for forming an SOI layer (an SOI-CMOS circuit layer), and a high resistivity silicon is used for the bulk silicon (the substrate) as a sensor. Czochralski (CZ) silicon wafers (n-type only) have been used to make the SOI wafers since the project started. However, the CZ-SOI wafer has a resistivity of 700 Ω cm and therefore high voltages of 300 V have to be applied to use a 300 μm−thick wafer in fully depleted condition. Float-Zone (FZ) wafers have recently been utilized for the SOI wafer fabrication, and eventually the FZ-SOI (n- and p-types) sensors were successfully developed. The recent improvement of the n-type FZ- (NFZ-) SOI detectors is described in this paper. Additionally, double SOI (D-SOI) wafers were successfully fabricated for the first time by using the Smart Cut™ method twice. The top silicon layer is used for the SOI-CMOS circuit and the middle silicon layer used as an electrode compensating for the total ionizing dose (TID) effect, also acting as a shield against the back-gate effect and cross-talk between the sensor and the electric circuit. The side STEM view of a D-SOI sensor is shown in Fig. 1. The first test results of a D-SOI detector are shown in this report.

2. Detector development

SOI monolithic detectors are developed in multi-project wafer (MPW) runs which KEK organized twice a year. In the FY2011 MPW run, two integration-type detectors, the INTPIX5 and the

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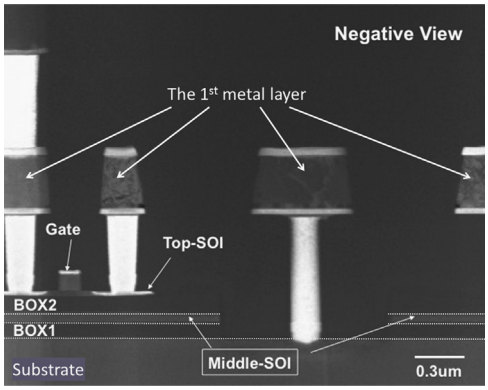

Fig. 1. The side STEM view of Double SOI sensor.

INTPIX3g, were developed. The specifications are shown in Table 1. The INTPIX5 is a large area, very fine pixel sensor for X-ray imaging, particle tracking and so on. The pixel circuit is shown in Fig. 2. This is a standard active pixel sensor (APS) circuit with a storage capacitor and a sensor gain switch. The CZ- and NFZ-INTPIX5 were made and irradiated with X-rays for spatial resolution study. The operation voltages of them were determined by measuring the leakage current. Fig. 3 shows *I–V* curves of CZ- and NFZ-INTPIX5 measured up to 400 V. For the CZ-INTPIX5, the back bias voltage (*Vdet*−*Vio*) was limited to only 100 V in other measurements because the leakage current was high: At this voltage, CZ-INTPIX5 was in a partial depletion state. On the other hand, the leakage current was very low up to 180 V for the NFZ-INTPIX5. Since the leakage current showed a rapid increase beyond 180 V (but it is not the breakdown), the back bias voltage was set to 170 V, at which the sensor was almost fully depleted. The INTPIX3g was made for study of n-type and p-type sensors, and D-SOI sensors. The INTPIX3g sensors with single SOI (S-SOI) and D-SOI wafers were studied for the radiation tolerance. Fig. 4 shows the pixel circuit of INTPIX3g. The reset switch can be selected in p-type and n-type sensors. A correlated double sampling (CDS) circuit is implemented in a pixel, and it can be turned off by using a *SKIP* switch. Other than INTPIX5, the buried n-well (BNW) process was applied between pixels to block current flows between pixels due to remaining middle SOI layers. In D-SOI, the breakdown voltage was about 50 V because of the middle SOI layer between high voltage and bias guard ring outside the pixel area (to be fixed in the next MPW run). Therefore, the back bias voltage was limited to 20 V for the sensors of both types. In the D-SOI INTPIX3g, the voltage of the middle SOI was limited to −2 V (because the voltage tolerance was unknown). In SOI-CMOS circuits, hole traps at the BOX cause parameter shift by the TID effect [5]. The negative voltages at the middle SOI might help to reduce the TID effect.

3. Spatial resolution study

The CZ- and NFZ-INTPIX5 sensors were irradiated with monochromatic X-ray at BL-14B in the KEK Photon Factory (KEK-PF). Fig. 5 shows the experimental setup. The CZ sensor was operated under partially depleted condition in which the applied voltage was 100 V and the NFZ sensor under almost fully depleted condition, 170 V. The X-ray energy was set to 16.1 keV and the absorption efficiency for those is about 26% for 150 μm CZ sensor and 60% for 500 μm NFZ sensor, respectively. The sensors were irradiated from the front and the back side to study the difference between a front-illuminated and a back-illuminated sensor. X-ray intensity was fixed to see the difference of image qualities in both

Table 1
Specifications of SOI sensors.

Chip name	INTPIX5	INTPIX3g
Chip size (mm × mm)	18.4 × 12.2	6.0 × 9.1
Pixel size (μm × μm)	12 × 12	18 × 18
# of pixels (H × V)	1408 × 896	256 × 256

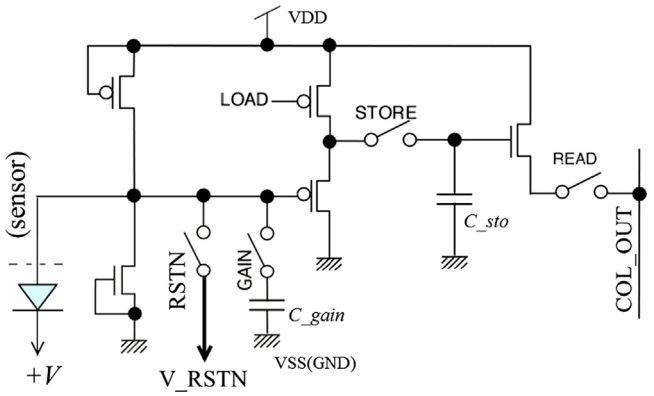

Fig. 2. Pixel circuit of INTPIX5.

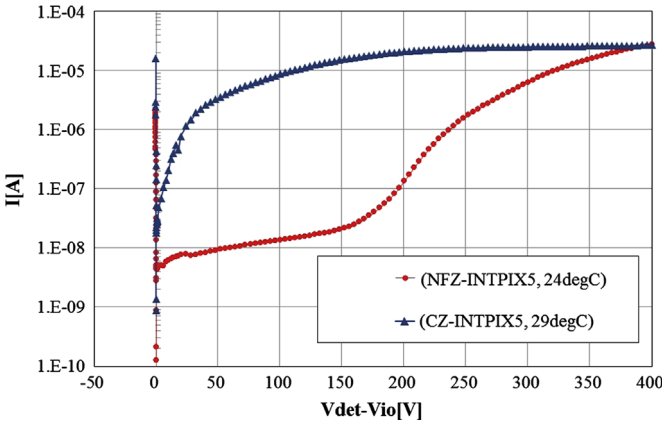

Fig. 3. *I–V* curves of CZ- and NFZ-INTPIX5.

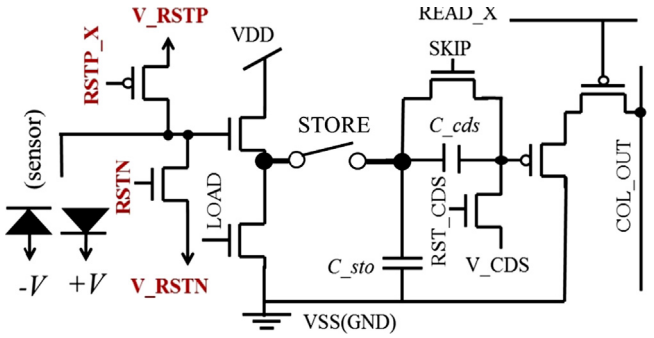

Fig. 4. Pixel circuit of INTPIX3g.

sensors. Spatial resolution was evaluated using X-ray test chart manufactured by NTT-AT Co., Ltd. The chart contains 16, 20, and 25 μm slits (in cycles, 31.25 LP/mm, 25 LP/mm, and 20 LP/mm, respectively). The material of the slit is 20 μm Au supported by 1 μm silicon nitride. At 20 μm−Au, X-ray transmission is less than 1%. Contrast transfer function (CTF) was calculated using the chart, which can be expressed as $CTF[\%] = (I_{MAX} - I_{GAP})/(I_{MAX} - I_{MIN})$, where I_{MAX} is the maximum output at a slit, I_{GAP} the minimum

output between slits, I_{MIN} the average output at the region covered with Au plate (not irradiated by X-ray). Figs. 6 and 7 show images of the chart measured in CZ- and NFZ-INTPIX5. The images were summed in 100 images and the integration time in an image was 200 μs. In CZ-INTPIX5, the statistics were poor because the depletion thickness was not large and therefore the absorption efficiency was low. Additionally there was a base shift due to X-ray absorption at the un-depleted region. In NFZ-INTPIX5, the statistics were better than that of CZ-INTPIX5 because the depletion thickness was larger. Because it was almost fully depleted, the base shift was very small, about 100 ADU. Fig. 8 shows the CTF distribution in CZ- and NFZ-INTPIX5. It was found that the CZ-INTPIX5 has better spatial resolution than the NFZ-INTPIX5. However, NFZ-INTPIX5 can also be used for high-resolution X-ray imaging since the CTF was more than 30% even at 31.25 LP/mm.

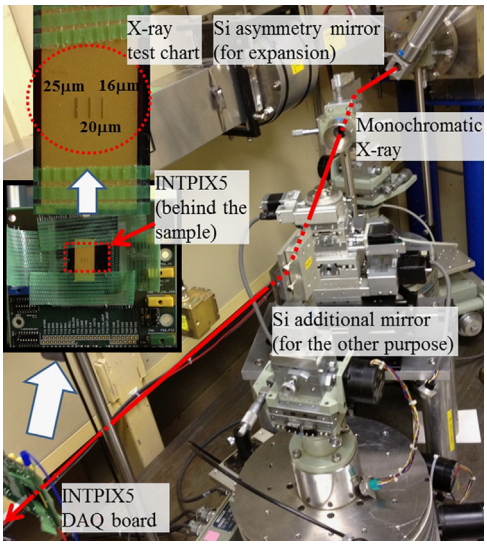

Fig. 5. Experimental setup at KEK-PF BL-14B.

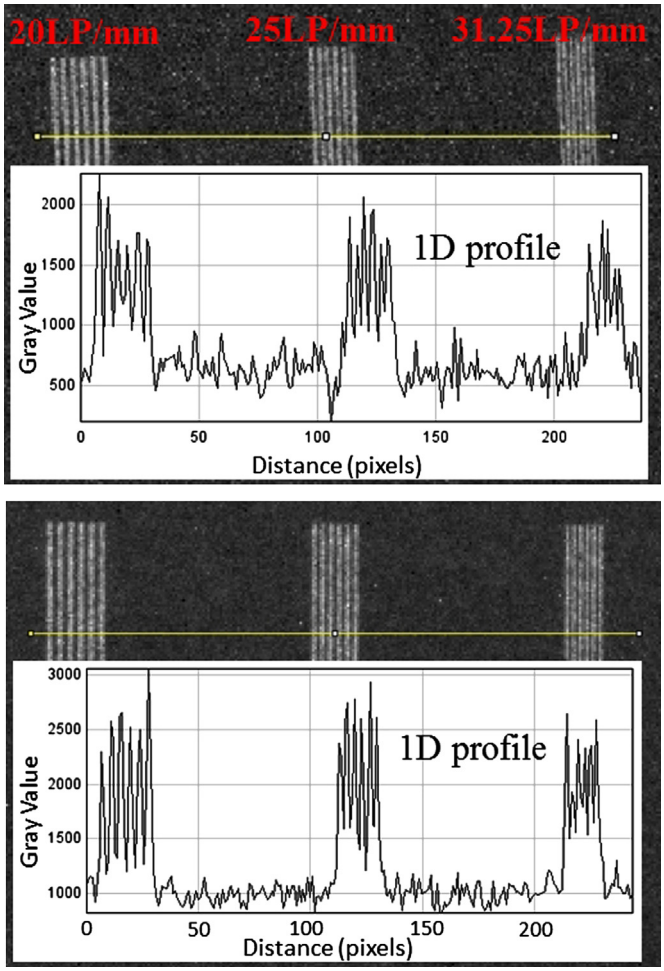

Fig. 6. Test chart images in CZ-INTPIX5. Top (bottom) images are for front (back) illumination.

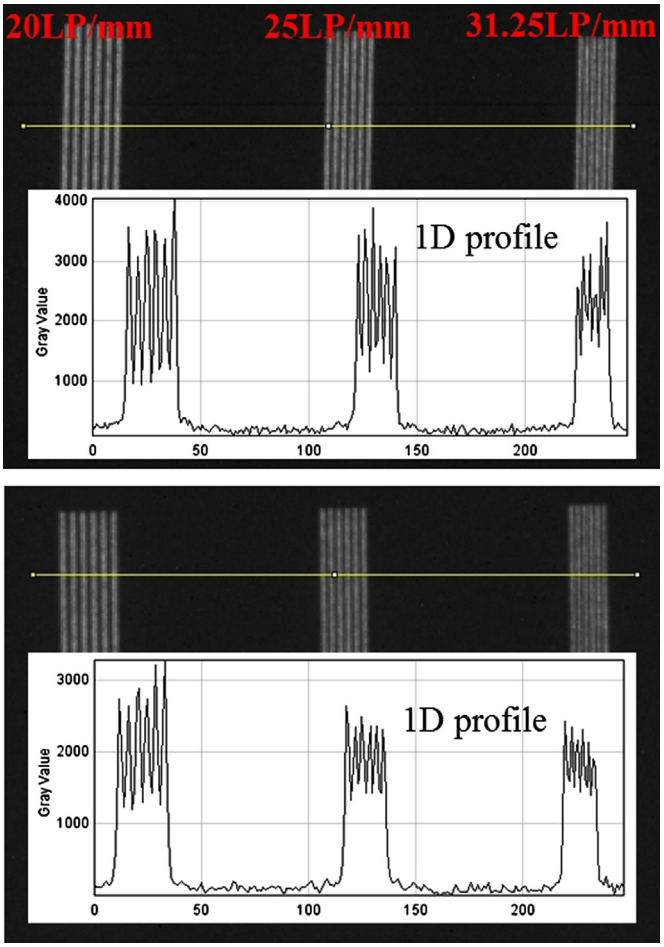

Fig. 7. Test chart images in NFZ-INTPIX5. Top (bottom) images are for front (back) illumination.

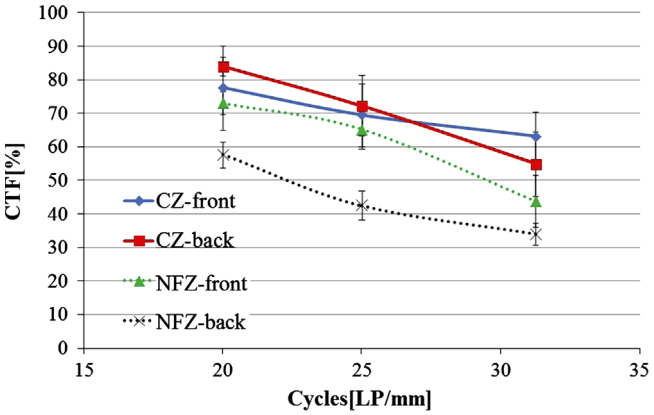

Fig. 8. CTF distribution in CZ- and NFZ-INTPIX5.

4. TID tolerance study

Using the S- and D-SOI INTPIX3g, the X-ray irradiation test was done using a Rigaku X-ray generator with copper (Cu) target. In advance, the X-ray spectra were measured at an output voltage of 30 kV, by an X-ray detector (Amptek XR-100CR, 6 mm^2 / 500 μm, 1.0 mil Be) with an X-ray slit with a size of 0.3 mm by 0.3 mm. The spectra showed K_α and K_β lines were dominant, and therefore the weighted average of those, 8.2 keV, was used for the estimation of the number of photons. The SOI sensors were put far from the X-ray target by 160 mm, and the size of an X-ray slit in front of the sensor was 1 mm by 1 mm. The X-ray intensity was measured by a large-area Silicon PIN photo diode (Hamamatsu C3584-08) at 30 kV and 60 mA. The radiation damage in the SOI sensor was normalized by the BOX absorption dose just below the SOI circuit layer. The S- and D-SOI chips were irradiated from the front side. In the S-SOI INTPIX3g, the absorption dose for the first irradiation was 23.2 krad, and the absorption dose for 10 s after the 2nd time was 11.6 krad. In the case of the D-SOI INTPIX3g, in the first 10 irradiations the dose was 12.6 krad in each and then the irradiation time was expanded to 60 s, and therefore the dose was 76.0 krad in each. There was about 1-minute intermission between the irradiations. The D-SOI INTPIX3g was irradiated to about 2.3 Mrad in total. Fig. 9 shows the result of the S-SOI INTPIX3g. After 60 krad, the signal started attenuation and eventually disappeared after 90 krad irradiation. Additionally, the base voltage was shifted. Fig. 10 shows X-ray spot images after 40 and 90 krad irradiations. The middle part was illuminated with X-rays and therefore the signal disappeared after 90 krad irradiation. At the edge of the slit, the radiation dose was not high and therefore some sensitive pixels remained around the spot. In the case of the D-SOI INTPIX3g, the signal did not disappear even after 2 Mrad as shown in Fig. 11. However, the base voltage was still shifted. Fig. 12 shows the base shift of the S- and D-SOI INTPIX3g as a function of the BOX absorption dose. In the S-SOI case, NMOS transistors were very sensitive to the accumulation of hole traps at the BOX and the transistors became on when the dose exceeded about 90 krad. In the D-SOI case, hole traps were attracted to the middle SOI when negative voltages were applied and therefore the TID tolerance increased. The test proved the effectiveness of the double SOI structure. In this test, the applied voltage of −2 V was unchanged. The radiation tolerance should be enhanced by applying larger voltage to the middle SOI. Additionally, the dynamic range should be restored to non-irradiation level. We are in progress of verifying the middle SOI, and a modified SOI chip is under fabrication in the 2nd MPW run in FY 2012.

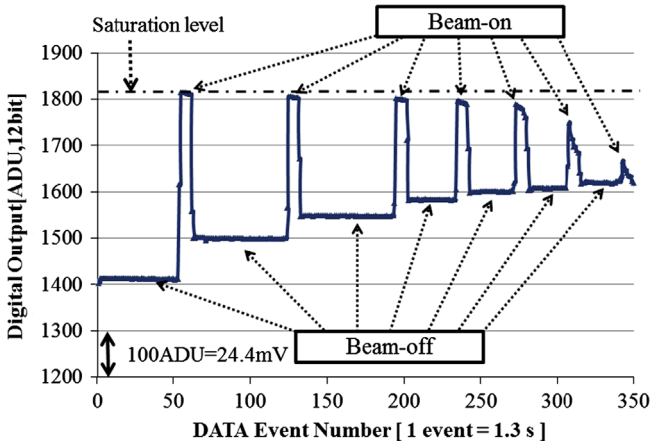

Fig. 9. Dose dependence of a pixel output in S-SOI.

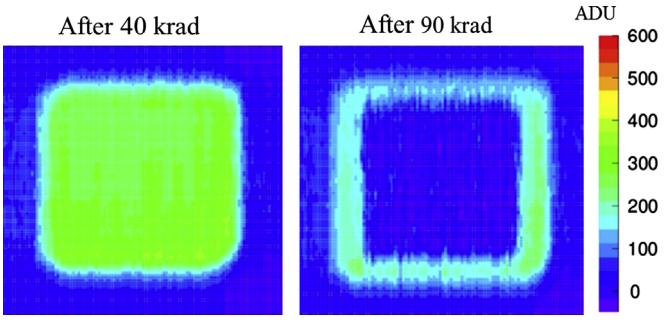

Fig. 10. X-ray spot images from S-SOI after irradiation.

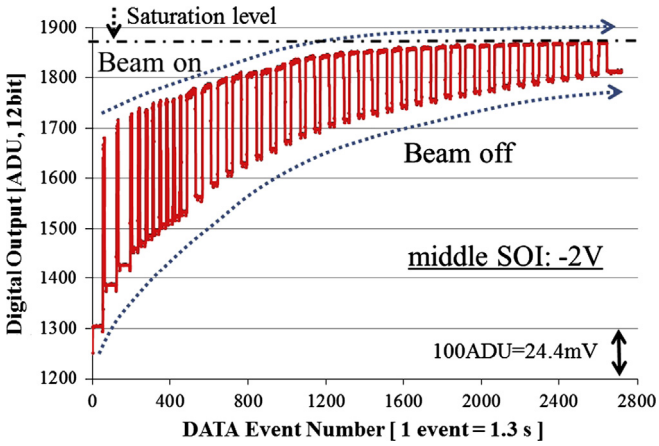

Fig. 11. Dose dependence of a pixel output in D-SOI.

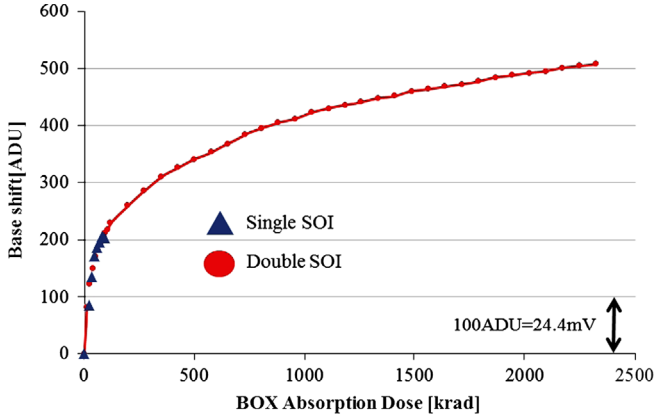

Fig. 12. Base shift by BOX absorption dose in S- and D-SOI.

5. Summary

We are developing monolithic pixel detectors using SOI technology. Two wafers, NFZ- and D-SOI, were utilized in 2012. INTPIX5 was fabricated using CZ- and NFZ- SOI wafers and it showed very good spatial resolution in both sensors. INTPIX3g was fabricated using S- and D-SOI wafers and the D-SOI structure revealed enhanced TID tolerance. We will continue these studies in 2013.

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