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Development of the Pixel OR SOI detector for high energy physics experiments

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ABSTRACT

A Silicon-On-Insulator (SOI) Technology is suitable for vertex detectors for high energy physics experiments since complex functions can be fabricated on the SOI wafer with a small amount of material thanks to the monolithic structure. We developed a new sensor processing scheme "PIXOR(PIXel OR)" for pixel detectors using a LAPIS 0.20 μm SOI process.

An analog signal from each pixelated sensor is divided into two dimensional directions, and 2*n* signal channels from a small *n* by *n* pixel matrix are ORed as *n* column and *n* row channels, then the signals are processed by a readout circuit in each small matrix. This PIXOR scheme reduces the number of readout channels and avoids a deterioration of intrinsic position resolution due to large circuit area, that was a common issue for monolithic detectors. This feature allows high resolution, low occupancy and on-sensor signal processing at the same time. We present the successful results of the PIXOR readout scheme using a first prototype.

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1. Introduction

In high energy physics experiments, a vertex detector plays an important role to identify b/c quarks by measuring impact parameters of tracks from short-lived heavy hadrons. Vertex detectors require

(1) High point resolution
(2) Low occupancy
(3) Low material budget
(4) Radiation tolerance
(5) Low power consumption

and generally semiconductor detectors are used since the characteristics are suitable for the requirements.

One of the candidates is a silicon-on-insulator pixel detector (SOIPIX) which utilizes a substrate layer as a radiation sensor [1]. The SOIPIX consists of three layers, a substrate sensor layer, an SiO_2-layer called buried oxide (BOX) layer, and a CMOS circuit layer (Fig. 1). The substrate and CMOS circuit layers are insulated by BOX layer. If a particle penetrates the SOIPIX, electron–hole pairs are created in the substrate layer. The signal charges drift to and are collected by through-silicon vias, which electrically connect the substrate and circuit layers, and then processed by the circuit. Thanks to this monolithic structure, problems in hybrid silicon detectors can be solved and the performance as vertex detectors is improved.

Since a standard sub-micron CMOS process is used for SOIPIX (1) high point resolution with fine pixel is achievable (detail will be discussed in Section 2). Fine pixel and faster signal processing allow (2) low occupancy even if the vertex detector is located at very close to interaction point. The monolithic SOIPIX is (3) low material compared with hybrid vertex detector which has bump bondings connecting sensor layer and circuit layer. Concerning (4) radiation tolerance, the probability of single-event-effect (SEE) is very small thanks to thin active-layer, however total-ionizing-dose (TID) effect still needs some improvement for applications in high radiation environment [2] (we have some possible solutions for TID effect). Finally, (5) low power consumption is achievable due to low leakage current and small parasitic capacitance.

The feature of pixel detectors which have readout chip on-sensor also allows the use of more intelligent signal processing in each pixel simultaneously. Moreover, a high signal-to-noise ratio, granted by the low sensor parasitic capacitance, may reduce its sensor thickness considering minimum ionizing detection.

The paper is organized as follows. In Section 2, we introduce the new signal processing scheme called "PIXOR". Then we explain

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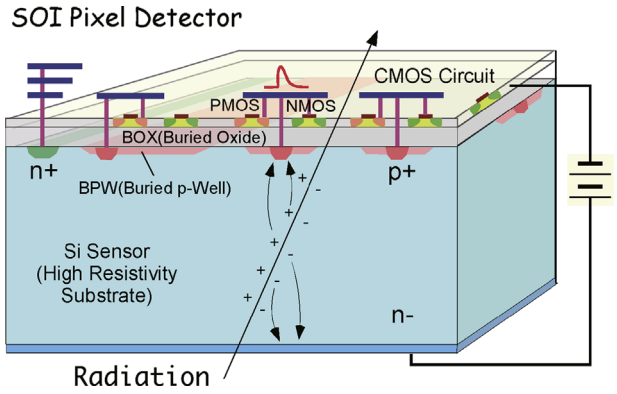

Fig. 1. Structure of the SOIPIX. The thickness of Si-sensor, BOX layer and CMOS circuit are 50–725 μm, 0.20 μm and 0.04 μm, respectively.

the first prototype of the PIXOR chip in Section 3, and report its evaluation results in Section 4. Finally we summarize the prototype PIXOR chip in Section 5.

2. PIXOR scheme

In general, to obtain 2-dimensional position of a penetrating particle, two kinds of sensor shape can be considered, strip and pixel. In very high radiation environments, pixel detectors should be used since the occupancy is much smaller than that of strip detectors. However, the position resolution for conventional pixel detectors is as not good as that of strip detectors. To avoid the problem, a new sensor processing scheme Pixel OR (PIXOR) was developed.

2.1. Limitation of pixel detectors with chip-on-sensor

In high energy physics experiments, data are usually taken when trigger signals are issued. Thus each detector should have a trigger receiver. For conventional chip-on-sensor pixel detectors, each pixel has its own readout circuit and trigger receiver. Since the readout timing is synchronized with the trigger, occupancy can be small enough. However, position resolution is limited by pixel size which is constrainted by circuit area on each pixel (Fig. 2). One of the merits of SOIPIX is that complex functionalities can be fabricated with a standard CMOS process. If complicated circuitry is included in each pixel, the pixel size becomes much larger and the position resolution becomes worse. There are pixel detectors with rectangular pixel shape to improve the resolution in the shorter side's direction but these sacrifice the position resolution in the longer side's direction [3–5].

2.2. New readout scheme – PIXOR

To solve the pixel size problem, the PIXOR readout scheme was developed. PIXOR is a signal handling scheme for pixelated sensor nodes and represents an intermediate structure between pixels and strips.

The PIXOR readout scheme (Fig. 3) is based on a unit of an $n \times n$ pixel matrix, called Super Pixel. A signal from one pixel in a Super Pixel is divided into two directions, X and Y. For each column, the X signals of the n pixels in that column are analogue ORed together. Likewise for each row, the Y signals of the n pixels in that row are ORed together . The result is n ORed column signals and n ORed row signals. The ORed signal is processed by a readout circuit and sent to a data acquisition system. This readout scheme reduces the number of readout channels from n^2 to $2n$, and there is space available to include a complex readout circuit. Moreover,

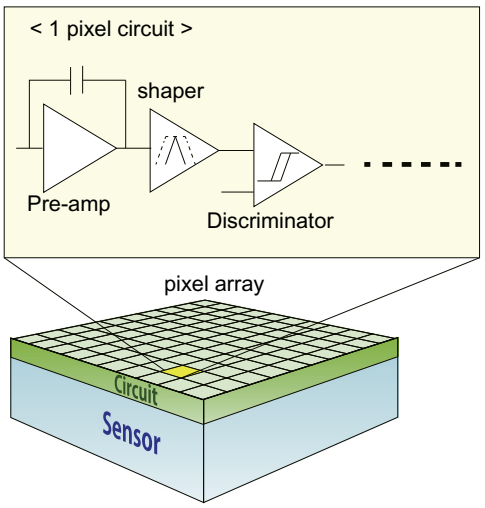

Fig. 2. Schematic view of chip-on-sensor. Each pixel has each readout circuit.

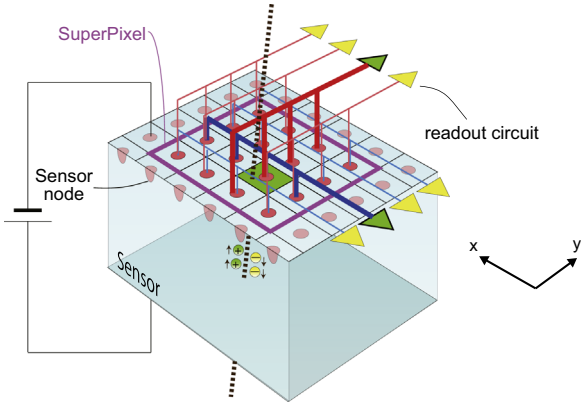

Fig. 3. Conceptual view of PIXOR (4×4 Super Pixel case). A charged particle penetrates the green pixel. The signal is divided into X(blue)/Y(red) directions. In this figure, readout circuit is not shown. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

we can change the effective circuit area by not enlarging its pixel size, but optimizing the number of ORed pixels. If the Super Pixel is small enough, the probability to have two hits is tiny compared with strip detector and ghost hits can be negligible. In conclusion, a PIXOR could solve the circuit area problem and achieve a high point resolution and a low occupancy.

3. First prototype – PIXOR1

We developed the first prototype PIXOR1 to confirm the PIXOR scheme within the SOIPIX Collaboration [6]. The PIXOR1 is fabricated by LAPIS Semiconductor Co. Ltd. 0.20 μm CMOS fully depleted (FD-) SOI process, and its sensor is 260 μm thick [7].

3.1. Circuit

The primary goal of the PIXOR1 evaluation is to confirm the basic concept of PIXOR readout scheme. For this purpose, we developed PIXOR1 chip just having the pixel OR part on the sensor, and analog and digital circuits are off-sensor (Fig. 4).To avoid electrical connection between readout channels, two diodes are used in the OR line. The analog part consists of a charge amplifier, a shaper and a discriminator with a 4-bit DAC. The gain and peaking time of the amplifier and shaper are 100 μV/e and 100 ns.

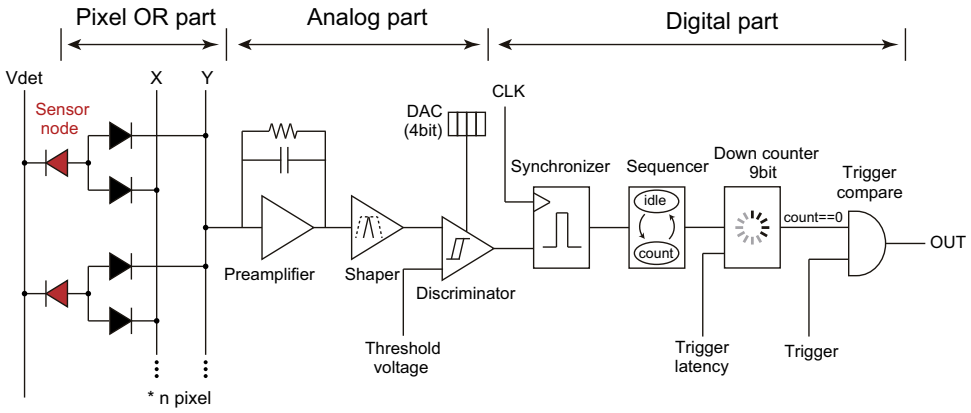

Fig. 4. PIXOR1 circuit for single channel. Analog and digital part are not mounted on sensor region (off-sensor).

A common threshold voltage can be applied to the discriminator for all channels and fine threshold tuning can be controlled by the 4-bit DAC in each channel. Here, we adopt the binary readout method to handle the hit data to avoid the use of any analog buffers to store the signal charge during the trigger latency.

The digital part manages binary data holding and timing comparison of a hit and trigger. Generally, in high energy experiments, a trigger decision typically takes several micro seconds, and after that the trigger signal is sent to each sub-detector. Hence, the hit information should be stored during the trigger latency. The digital part of the PIXOR1 has a 9-bit down counter to hold the binary data in each channel. A signal coming from analog part is synchronized to the digital clock (with synchronizer), then the use of down counter is checked by the sequencer, count down starts from the latency time which corresponds to a initial value of the counter (by the 9-bit down counter). When the time of the counter becomes zero, hit data timing is compared with the external trigger signal by trigger compare. If the timing is consistent, hit data is sent to a central data acquisitions system. Once trigger comparison is done, the sequencer discards the hit information and waits for the next signal. For higher occupancy environments, we will mount additional counters which allow a higher number of hits to be recorded.

3.2. Test element group

To check the analog and discriminator signals separately, two simple test circuits (called Test Element Group: TEG) were included on the PIXOR1 chip; one outputs a signal from a shaper (shaper output TEG in Fig. 5), the other outputs a signal from a discriminator (binary output TEG in Fig. 5). Thanks to the PIXOR scheme, the pixel pitches can be reduced to 25 μm and 40 μm in each direction with 16-pixel OR.

The shaper output TEG is used to confirm that the two divided signals have same shape and amplitude. In this region, there are 7 Super Pixels with 4-pixel-OR PIXOR readout scheme having 16 pixels and 8 readout channels. We can monitor the two shaper outputs from *X* and *Y* directions simultaneously.

The binary output TEG aims to check the data processing with a trigger signal. A signal from a pixel sensor is processed by pixel OR, analog and digital circuits and binary hit information can be obtained with a trigger signal. This area consists of the 22 Super Pixels with 16-pixel-OR PIXOR readout scheme having 256 pixels and 32 readout channels, where all readout circuits can be included on the Super Pixel. Fig. 6 shows a layout of a Super Pixel for binary output TEG.

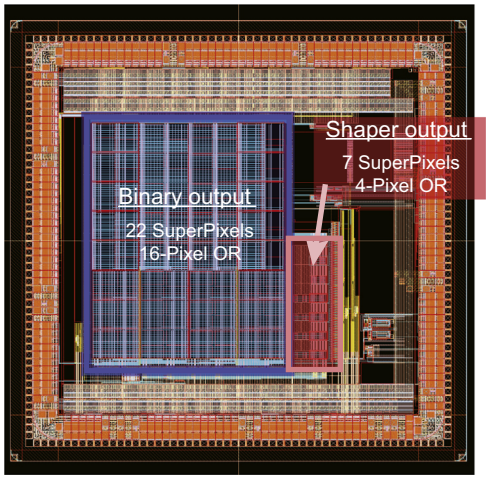

Fig. 5. Layout of the PIXOR1. The chip size is 6 mm × 6 mm.

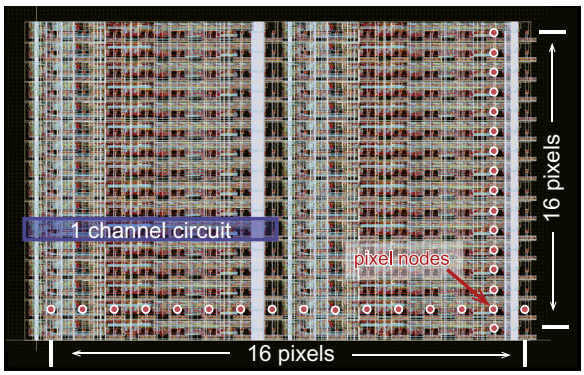

Fig. 6. Layout of a Super Pixel (16-pixel OR) which is the readout circuit on-sensor. In this paper, we report the result which is readout circuit off-sensor.

4. PIXOR1 result

We report results of basic evaluations, the shaper output is checked with an X-ray source and a validation of the trigger processing digital circuit is performed.

4.1. Shaper output

We measured the shaper output with ^{109}Cd X-ray source which radiates 88 keV photons making about 6000 electron–hole pairs in the silicon sensor which corresponds to a number of the pairs

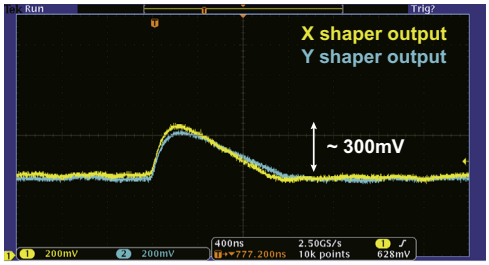

Fig. 7. Shaper output with a ^{109}Cd X-ray source.

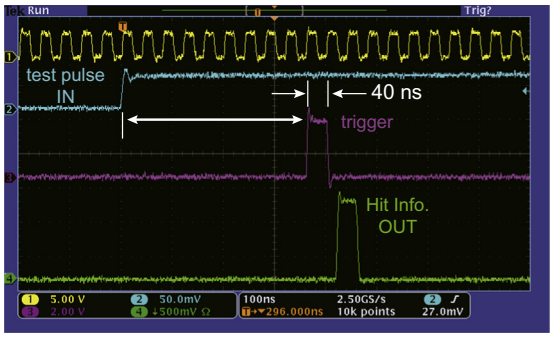

Fig. 8. Evaluation of trigger processing circuit. From top to bottom, clock (yellow), test pulse (cyan), trigger (magenta) and binary hit information (green). (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

generated by a minimum ionizing particle penetrating about a 75 μm silicon layer.

Fig. 7 shows shaper outputs for *X*and *Y*directions taken with Tektronix DPO-3034. Clear signals with 6000 input electrons are seen and the signal charges are equally divided into the two directions. This result confirms one of the important functions for PIXOR readout scheme.

4.2. Digital circuit

We have evaluated the overall circuit with a test-pulse to check the synchronization of the hit timing and trigger timing by digital circuit. Fig. 8 shows clock, input test pulse signal, trigger signal and output binary hit information. The digital circuit could store the signal hit information during the trigger latency and send a binary hit information as expected.

5. Summary

A limitation of point resolution due to large circuit size is a common issue for hybrid and monolithic pixel detectors. The Pixel OR (PIXOR) scheme is designed to solve the problem. To reduce the circuit area, the number of readout channels is reduced from n^2 to $2n$ by taking analog OR of several pixel nodes in both *X*and *Y*dimensions in each $n \times n$ pixel matrix. We fabricated the PIXOR1 chip as a first prototype and evaluated it. As a result, we confirmed that signals are cleanly divided into two dimensions and the trigger processing circuit works well as expected. Since the basic PIXOR scheme has been confirmed, further work will include measurement of cluster size with an X-ray source and the beam test to study the position resolution. More complex circuitry can be fabricated with the next chip, PIXOR2.

Acknowledgments

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References

[1] Y. Arai, et al., Nuclear Instruments and Methods in Physics Research Section A 636 (2011) S31.
[2] K. Hara, et al., IEEE Transactions on Nuclear Science NS-56 (5) (2009) 2896.
[3] G. Aad, et al., Journal of Instrumentation 3 (2008) P07007.
[4] H.C. Kastli, et al., Nuclear Instruments and Methods in Physics Research Section A 565 (2006) 188.
[5] W. Snoeys, et al., Nuclear Instruments and Methods in Physics Research Section A 465 (2001) 176.
[6] SOIPIX Collaboration. ⟨http://rd.kek.jp/project/soi/⟩.
[7] LAPIS Semiconductor. ⟨http://www.lapis-semi.com/⟩.