



## Investigation of radiation hardness improvement by applying back-gate bias for FD-SOI MOSFETs

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### ABSTRACT

Radiation hardness improvement of fully depleted silicon on insulator (FD-SOI) metal-oxide-silicon field effect transistors (MOSFETs) has been investigated in terms of back-gate bias recovering to compensate generated positive charge in buried oxide (BOX) by X-ray irradiation. In general, the radiation tolerance of FD-SOI MOSFETs is low in total ionizing dose (TID) due to the generated positive charge in BOX. However, biasing the back-gate to negative can compensate the charge. In the method, the electrode of back-gate should cover both N and P channel different gate length MOSFETs to minimize area penalty. To reduce the gate length dependent characteristic change by the irradiation, high dose lightly doped drain (LDD) is newly introduced. The back-gate bias windows within 100 mV in the threshold voltage and 15% in the drain current change up to 112 kGy(Si) X-ray irradiation has been confirmed for the N and P channel MOSFETs of wide gate length range from 0.2 to 10  $\mu\text{m}$ .

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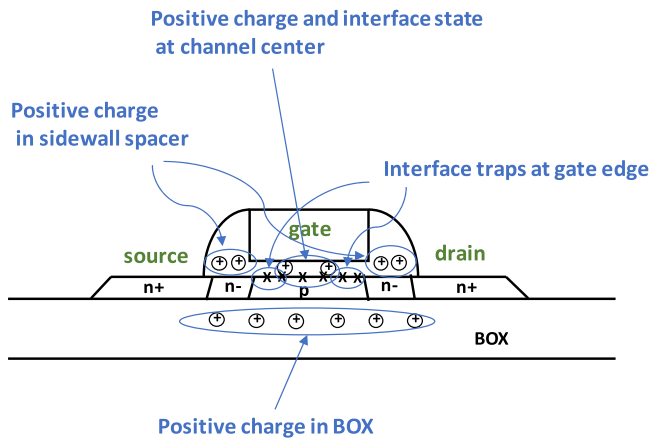
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### 1. Introduction

A monolithic pixel imager using silicon on insulator (SOI) technology has been considered to be a suitable detector for scientific experiments such as X-ray imaging, X-ray energy spectrum analysis, and charged particle tracking [1]. The advantages of SOI pixel imager are small pixel size owing to sub-micron via between the sensor and the circuitry and stacking of the circuitry on the sensor, high gain owing to small parasitic capacitance of the sense node, and low cost and high reliability owing

to the commercial semiconductor device process [2]. From radiation hardness point of view, the capture cross section of single event upset (SEU) is smaller than bulk complementary metal-oxide-semiconductor (CMOS) because of the transistor's perfect isolation by oxide and no thyristor structure in SOI [3]. However, it is well known that SOI has weakness in total ionizing dose (TID). The major X-ray irradiation inducing damages of the metal-oxide-silicon field effect transistor (MOSFET) are caused by the generated positive charge in oxide and the generated traps at interface between oxide and silicon [4]. When X-ray irradiated

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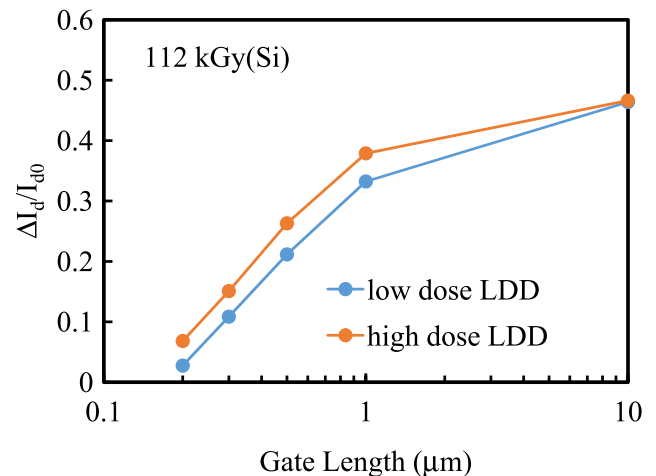
**Fig. 1.** Schematic cross section of FD-SOI MOSFET after X-ray irradiation for N channel MOSFET. In the case of P channel MOSFET, the generated positive charge and interface traps are the same but n+, n-, and p must be replaced by p+, p-, and n, respectively.

to SOI-MOSFET, electron–hole pairs are generated in gate oxide, buried oxide (BOX), and sidewall spacer. Some of the generated electrons and holes are recombined and the rest of electrons and holes drift by electric field in the oxide. Because the mobility of hole in oxide is lower than that of electron, some of the generated holes are trapped in the oxide. Thus, positive charge generated in the oxide by X-ray irradiation. The holes which drift to Si-SiO<sub>2</sub> interface create interface traps. From the structure of SOI-MOSFET, the positive charges are generated in gate oxide, BOX, and sidewall spacer. The traps are also generated at the interface between body silicon and gate oxide as shown in Fig. 1. The generated positive charge in sidewall spacer and interface traps at gate edge make gate length dependent characteristic change called as radiation induced gate length modulation (RIGLEM) [5,6]. On the other hand, the generated positive charge in gate oxide or the generated positive charge in BOX and the interface traps at gate center are considered to be no or less gate length dependence. The gate length independent characteristic change can be compensated by applying the back-gate bias through buried well in handle wafer in the case of single SOI or middle SOI in the case of double SOI [7]. Thus, to work the back-gate bias recovering efficiently, RIGLEM must be improved. In addition, it should be better to use the common back-gate bias electrodes for N and P channel transistors with various gate length to minimize the area penalty because of relatively rough design rule of the buried well or middle SOI patterns and due to keeping N and P channel active merge technique [8].

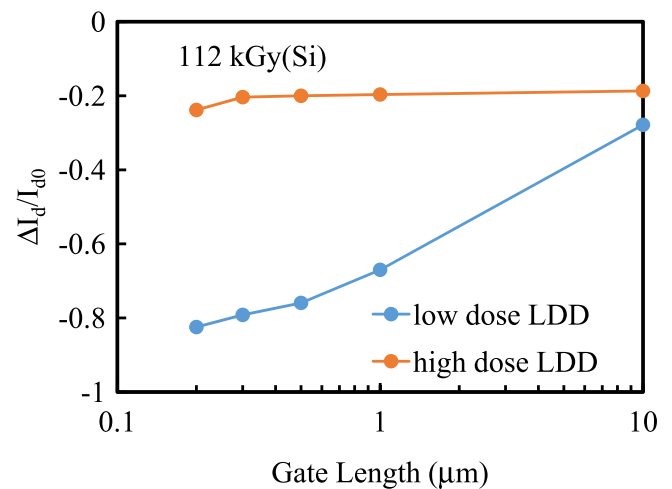
In this paper, RIGLEM improvement by high dose lightly doped drain (LDD) and characteristics recovering by applying proper back-gate bias are shown. The back-gate bias windows to keep given allowable ranges of threshold voltage and drain current change are also investigated when the back-gate electrode of the N and P channel MOSFETs with wide range of gate length is assumed to be in the same back-gate electrode plane.

## 2. Experimental

Test structures consisted of fully depleted SOI (FD-SOI) MOSFETs were fabricated by using a 0.2 μm FD-SOI CMOS process prepared by Lapis semiconductor [9]. To reduce the effect of positive charge generated by X-ray irradiation in the isolation oxide which is called as radiation induced narrow channel effect (RINCE) [10], impurity doping to the sidewall of SOI active was employed. Salicided active and gate poly silicon were also employed to reduce parasitic resistance and make contact reliable [11]. Conventional LDD structure with a 100 nm sidewall spacer was used. In the LDD process, two implant conditions



**Fig. 2.** Drain current change after 112 kGy(Si) irradiation as a function of gate length for N channel MOSFETs. The blue line indicates low dose LDD and the orange line high dose LDD. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)



**Fig. 3.** Drain current change after 112 kGy(Si) irradiation as a function of gate length for P channel MOSFETs. The blue line indicates low dose LDD and the orange line high dose LDD [13]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

which were relatively low or high dose were examined. BOX, final SOI, and gate oxide thickness are 200 nm, 40 nm, and 4.5 nm, respectively.

Floating body N and P channel MOSFETs with constant gate width of 10 μm and gate length of 0.2, 0.3, 0.5, 1.0, and 10 μm were examined. Evaluating MOSFET parameters are threshold voltages ( $V_t$ ) and linear region drain current ( $I_d$ ) measured from  $I_d$ - $V_g$  characteristics with  $|V_d| = 0.1$  V and varying the back-gate bias,  $V_{\text{back-gate}}$ , applied to the buried well from -18 to +2 V at room temperature. The threshold voltages are extracted from the  $I_d$ - $V_g$  curves at the maximum transconductance point. The linear region drain currents,  $I_d$ , were measured at  $|V_d| = 0.1$  V and  $|V_g| = 1.8$  V. The drain current change is defined as  $\Delta I_d/I_{d0} = (I_d - I_{d0})/I_{d0}$  where  $I_{d0}$  is linear region drain current of the pre-irradiation MOSFET.

To perform X-ray irradiation, a newly developed wafer level X-ray irradiation system was used [12]. The system has X-ray generator of a molybdenum rotary target with an acceleration voltage of 40 kV and a 0.5 mm thick aluminum filter to eliminate X-rays below 10 keV. X-ray dose rate was set to 3 Gy(Si)/s. During irradiation, all terminals of MOSFETs were connected to the ground. Even though the

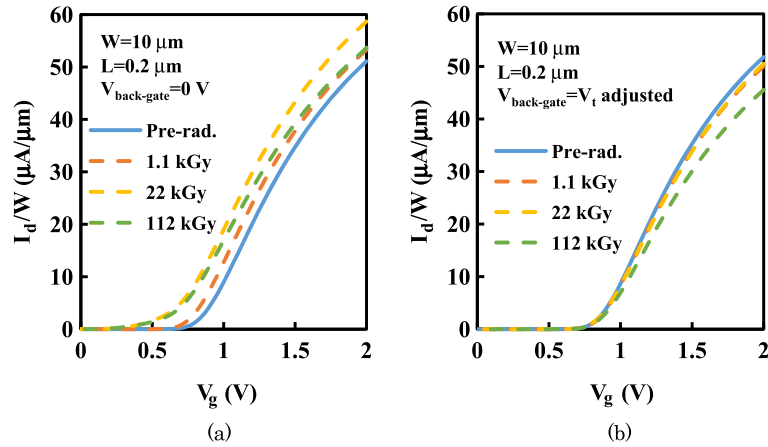


Fig. 4.  $I_d$ - $V_g$  characteristics of pre and irradiated N channel MOSFET with (a)  $V_{back-gate} = 0$  V and (b) back-gate bias to align  $V_t$  to pre irradiated one.

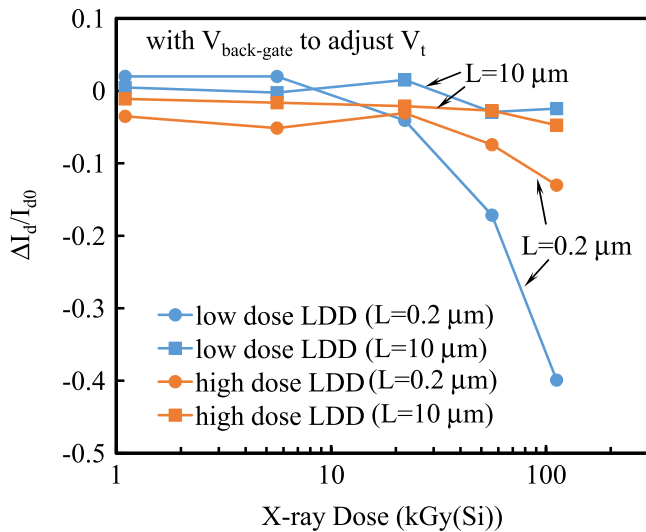


Fig. 5. N channel MOSFET drain current change with  $V_{back-gate}$  to adjust  $V_t$  as a function of X-ray dose for short ( $0.2 \mu\text{m}$ ) and long ( $10 \mu\text{m}$ ) channel devices. The blue lines indicate low dose LDD and the orange lines high dose LDD. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

terminals should be biased under the operation condition when the actual operation is considered, data of all terminal grounded was chosen for the simple analysis.

### 3. Results and discussion

#### 3.1. RIGLEM improvement by higher dose LDD

In the case of N channel MOSFETs, increase of the drain current is mainly caused by the generated positive charge in BOX which has no or less gate length dependence. On the other hand, the decrease of drain current is mainly caused by the generated interface traps at the gate edge from analysis of charge pumping method which will be reported in the future. Therefore, to reduce the gate length dependence, the high dose LDD is one of counter measures because the dopants of LDD diffuse laterally and cover the gate edge region as an n- diffusion layer. The N channel MOSFET's drain current change after 112 kGy(Si) X-ray irradiation as a function of gate length are shown for the low and high dose LDD in Fig. 2. The gate length dependence of drain current change is slightly improved by the high dose LDD. When the back-gate bias recovering is used, the improvement is obvious as described in the next section. The P channel MOSFET's drain current change after 112 kGy(Si) X-ray irradiation as a function of gate length are shown for low and high dose LDD in Fig. 3. In the case of P channel MOSFETs, the drain current decreases monotonically with X-ray dose due to the generated positive charge in BOX. The gate length dependence of drain current change for the low LDD dose is caused by the generated positive charge in sidewall spacer [5]. By using the high dose LDD, the

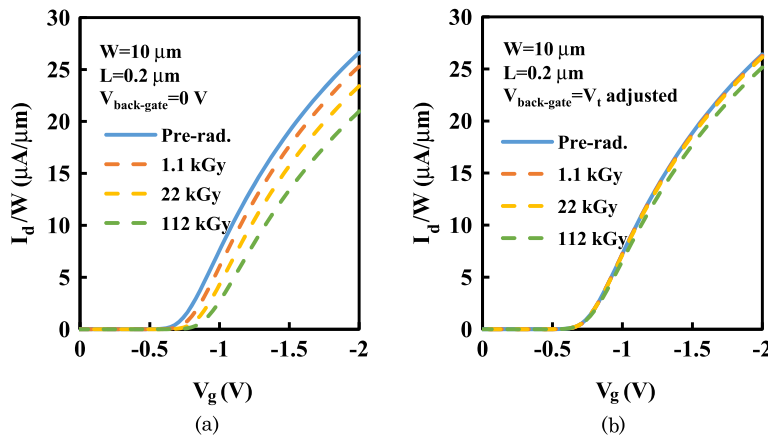


Fig. 6.  $I_d$ - $V_g$  characteristics of pre and irradiated P channel MOSFET with (a)  $V_{back-gate} = 0$  V and (b) back-gate bias to align  $V_t$  to pre irradiated one.

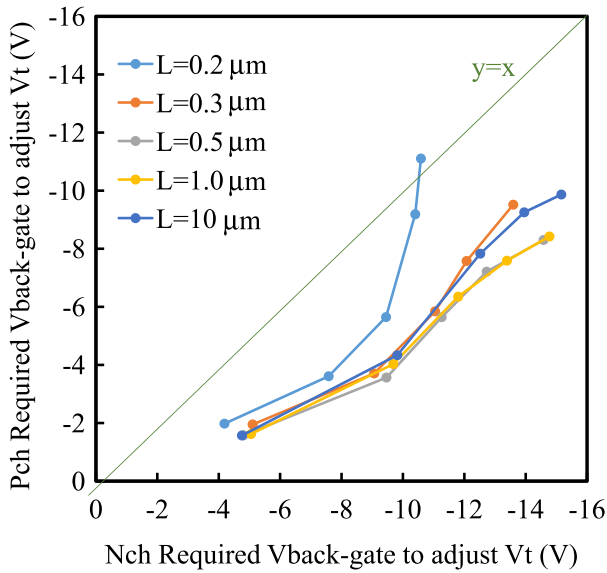


Fig. 7. Correlation between required  $V_{back-gate}$  to adjust  $V_t$  for N channel and that for P channel MOSFETs.

gate length dependent drain current change is improved as shown in Fig. 3.

### 3.2. Characteristic recovering by back-gate bias

The gate length dependence of the drain current change is improved by using the high dose LDD for both N and P channel MOSFETs. With the high dose LDD MOSFETs, characteristic recovering by back-gate bias is investigated after X-ray irradiation up to 112 kGy(Si). In this recovering, the back-gate bias is set to adjust the threshold voltage to that of pre-irradiation. The N channel 0.2  $\mu\text{m}$  MOSFETs'  $I_d-V_g$  characteristics when the back-gate bias is the ground or set to adjust the threshold voltage are shown in Fig. 4(a) or (b), respectively. When the back-gate bias is the ground, the drain current increases after X-ray irradiation because of the threshold voltage decrease due to the generated positive charge in BOX. On the other hand, the drain current decreases with X-ray dose when the threshold voltage is adjusted by the back-gate bias because of the mobility reduction by the generated interface traps. If the generated charge by X-ray irradiation is uniformly distributed in the plane of oxide, the charge is easily compensated by field effect of the back-gate bias. On the other hand, the mobility reduction by the generated interface traps is hardly compensated by the field effect of the back-gate bias. It is also noted that the high dose LDD improves the drain current

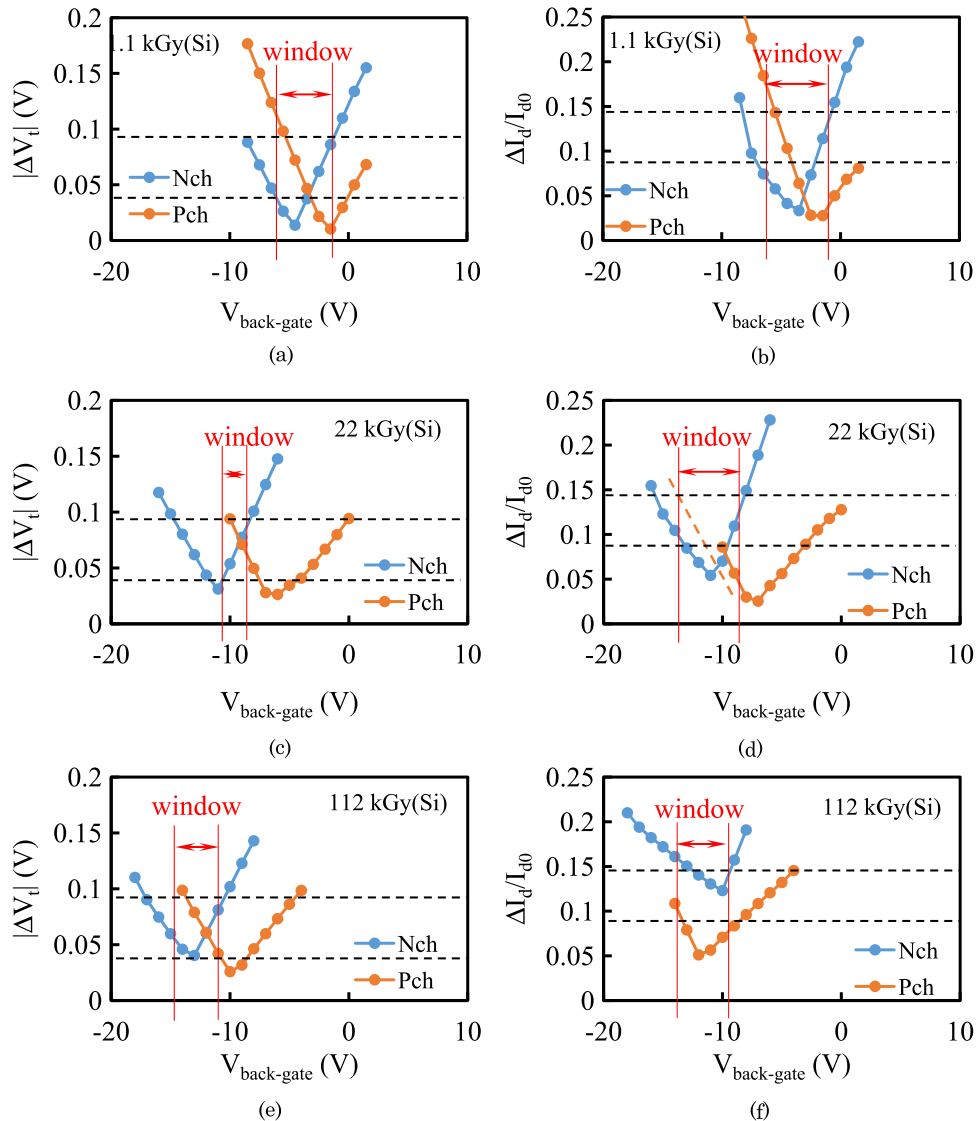


Fig. 8. The maximum threshold voltage change (a), (c), (e) and drain current change (b), (d), (f) within the gate length range from 0.2 to 10  $\mu\text{m}$  as a function of  $V_{back-gate}$  after 1.1 kGy(Si) (a), (b), 22 kGy(Si) (c), (d), and 112 kGy(Si) (e), (f) X-ray irradiation.

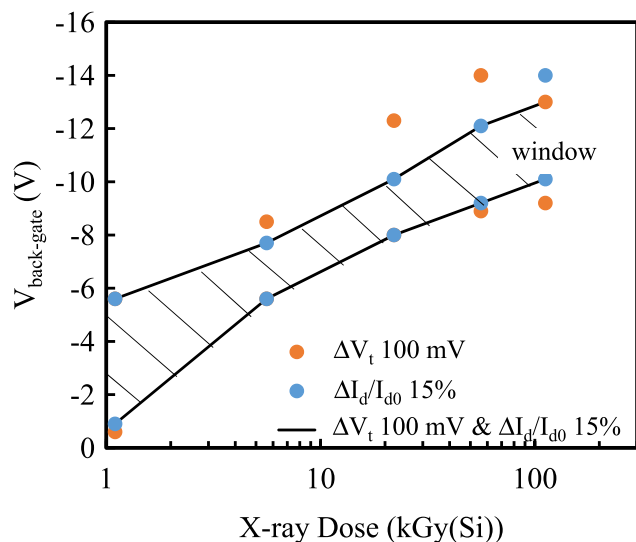


Fig. 9. Back-gate bias windows to allow 100 mV threshold voltage change and 15% drain current change as a function of X-ray dose.

change with the back-gate bias to adjust the threshold voltage especially shorter gate length as shown in Fig. 5. The  $L = 0.2 \mu\text{m}$  MOSFET drain current change of high dose LDD is only around 15% after 112 kGy(Si) irradiation while the drain current change of the low dose LDD is around 40%. The P channel  $0.2 \mu\text{m}$  MOSFETs'  $I_d-V_g$  characteristics when the back-gate bias is the ground or set to adjust the threshold voltage are shown in Fig. 6(a) or (b), respectively. When the threshold voltage is adjusted by the back-gate bias, the drain currents are almost identical up to 112 kGy(Si) irradiation even though the gate length is  $0.2 \mu\text{m}$ . It is confirmed that applying the back-gate bias is efficient to recover the characteristics after X-ray irradiation for both N and P channel MOSFETs. The correlation between the required back-gate biases to adjust the threshold voltages for N channel and those for P channel are also shown in Fig. 7 as a parameter of the gate length. The required back-gate biases are approximately on the same trend except for  $L = 0.2 \mu\text{m}$  case due to RIGLEM of the N channel MOSFETs. The biases of P channel are always lower than those of N channel which may be caused by work function difference between body silicon and buried well. In the case of P channel, the generated holes tend to migrate to the buried well.

### 3.3. Back-gate bias windows

The applying negative back-gate bias is confirmed to be an effective method to recover characteristics after X-ray irradiation. However, the required back-gate voltage to adjust the threshold voltage must be different between N and P channel MOSFETs. Even though the back-gate voltages are different, the back-gate electrode for N and P channel MOSFETs should be in the same plane in order to minimize area penalty and keeping N and P channel active merge technique. Thus, the back-gate bias windows to recover the characteristics within a given allowable range of the threshold voltage or drain current change have to be investigated. To define the back-gate bias windows,

the maximum threshold voltage or drain current changes from pre-irradiation at  $V_{\text{back-gate}} = 0 \text{ V}$  within the gate length range of  $0.2$  to  $10 \mu\text{m}$  with varying the back-gate bias after X-ray irradiation are taken for the N and P channel MOSFETs. The results are shown in Fig. 8 in the case of 1.1, 22, and 112 kGy(Si) irradiation. As shown in the figure, there is no back-gate bias windows up to 112 kGy(Si) irradiation when the allowable range is 50 mV in the threshold voltage change or 10% in the drain current change. When the allowable range is set to 100 mV in the threshold voltage change or 15% in the drain current change, the existing of back-gate bias windows are confirmed as shown in Fig. 9.

## 4. Conclusion

The FD-SOI MOSFET radiation hardness improvement has been investigated in terms of applying the back-gate bias to compensate the generated positive charge in BOX by X-ray irradiation. The buried well in handle wafer for the single SOI or the middle SOI for the double SOI can be used as the back-gate electrodes. To minimize the area penalty by introducing the back-gate electrode, the common back-gate electrodes is considered for the N and P channel MOSFETs with different gate length from  $0.2$  to  $10 \mu\text{m}$ . The high dose LDD can help to recover the characteristics of different gate length MOSFETs because RIGLEM is reduced for the N channel and almost eliminated for the P channel MOSFETs. It is also confirmed that the back-gate bias windows to recover the characteristics up to 112 kGy(Si) X-ray irradiation when the 100 mV in the threshold voltage and 15% in the drain current changes are assumed to be the allowable range for the device operation. This method may be one of solution candidates for radiation hardness improvement of TID weak FD-SOI MOSFETs.

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