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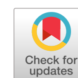
R&D status of SOI-based pixel detector with 3D stacking readout ☆



Toru Tsuboyama [a,*], Shun Ono [a], Miho Yamada [a], Yasuo Arai [a], Manabu Togawa [a], Ikuo Kurachi [a], Yoichi Ikegami [a], Kazuhiko Hara [b], Akimasa Ishikawa [c], Masayuki Ikebe [d], Makoto Motoyoshi [e]

[a] *KEK, High Energy Accelerator Research Organization, Tsukuba, Ibaraki 305-0801, Japan*
[b] *University of Tsukuba, Tsukuba, Ibaraki 305-8571, Japan*
[c] *Tohoku University, Aoba-ku, Sendai, Miyagi 980-8578, Japan*
[d] *Hokkaido University, Sapporo 060-0814, Japan*
[e] *Tohoku Microtec, Aoba-ku, Sendai, Miyagi 980-8579, Japan*

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ABSTRACT

SOFIST4 is an SOI pixel sensor designed for the International Linear Collider (ILC) vertex detector. In order to satisfy the requirements of the ILC vertex detector, the chip consists of three-stage hit-charge and hit-time memories in each 20 μm × 20 μm pixel with 3D integration technology. The SOFIST4 chip was submitted for an MPW run in 2017, and 3D integration will be performed in 2018. In this article, the design of the SOFIST4 chip is first described. Then the 3D integration and 3D CAD technology are explained.

1. Introduction

The luminosity of particle accelerators is being increased rapidly in order to examine the standard model and explore new particle physics. The pixel detectors, which will be installed close to the collision point, should be operated at high hit rates from physics events as well as beam backgrounds. To measure the particle tracks precisely, we need to reduce the pixel size. In addition, a high time resolution is necessary to select the hit signal from the off timing backgrounds. To implement such complex functions in the pixel sensor, we have started R&D of a 3D integration pixel sensor, where readout IC chips are stacked on the sensor, and a high-density signal connection is made between the chips.

An effort toward a 3D integrated pixel sensor has been reported by the VIP collaboration [1]. The group stacked two readout ICs and integrated them onto a sensor wafer. The X-ray images were successfully obtained using the sensor.

2. SOFIST pixel sensor

In the International Linear Collider (ILC) [2], approximately 1300 beam bunches undergo collisions with 554-nsec intervals for 1 ms, followed by a non-collision interval of 200 ms, as shown in Fig. 1.

The SOFIST silicon-on-insulator (SOI) pixel sensor [3] is designed to satisfy the requirements for the bunch structure. We decided to integrate several memories for the charge and timing of hits in each pixel and sample data during the 1300 collisions. The SOFIST1 and SOFIST2 prototype sensors have hit-charge memories and hit-time memories, respectively. SOFIST1 exhibited a 1.4 μm spatial resolution with a 20 μm × 20 μm pixel size [3]. SOFIST2 showed approximately 2 μsec timing resolution (preliminary).

2.1. SOFIST4

In 2017, we submitted the SOFIST4 prototype chip. To integrate the full pixel functions in the small pixel area of 20 μm × 20 μm, we introduced SOI 3D integration technology. The pixel circuits are distributed on the lower and the upper chips as shown in Fig. 2. The sense node, charge-sensitive amplifier (CSA), and comparator are integrated in the lower chip, and the shift register and the three-stage hit-charge and hit-time memories are implemented in the upper chip. There are four bump connections per pixel, as shown in Fig. 3. Two bumps transfer the analog signal and comparator output from the lower chip to the upper chip. The other two bumps connect the ground and the power supply to stabilize the power supply. The SOFIST4 chip incorporates the double SOI (DSOI) radiation-hard technology [4] so that it will work in the harsh radiation conditions in high luminosity accelerators. The specifications of the SOFIST4 chip are summarized in Table 1.

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* Corresponding author.
E-mail address: toru.tsuboyama@kek.jp (T. Tsuboyama).

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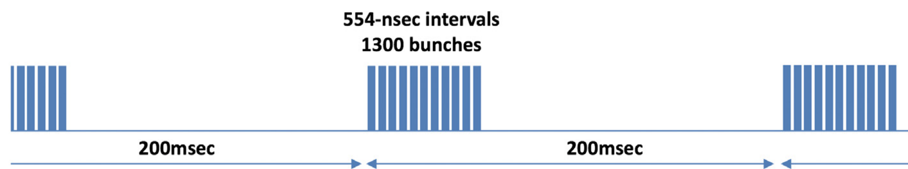

Fig. 1. The beam collision structure of the ILC.

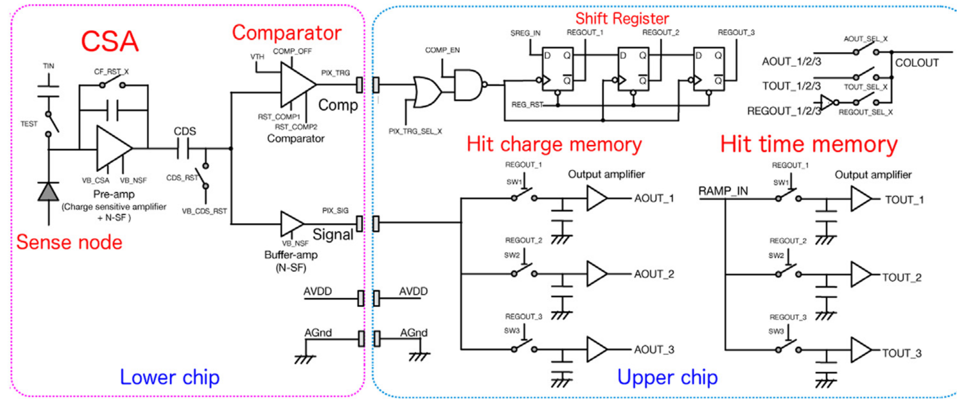

Fig. 2. Pixel circuit of SOFIST4.

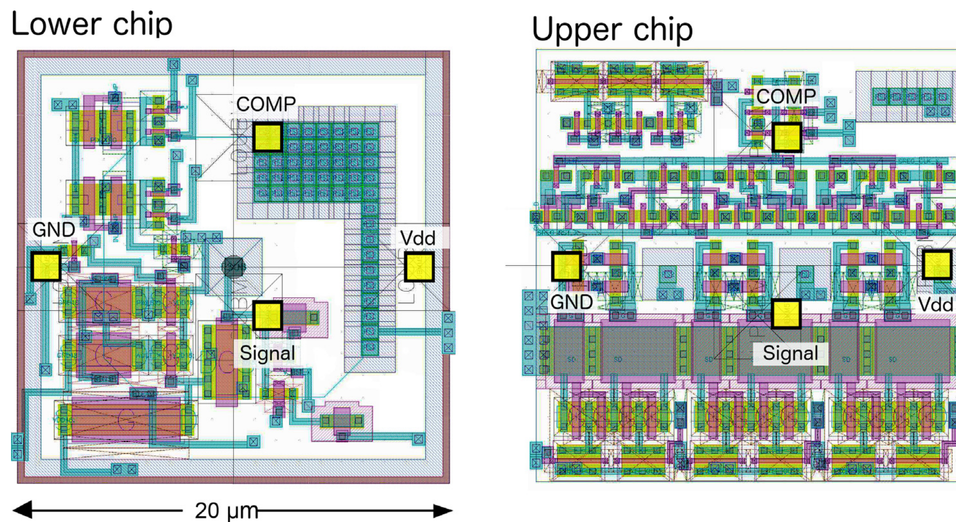

Fig. 3. Pixel layouts of the SOFIST4 lower chip and upper chip. The four pads for the bump connection are shown with bold lines.

2.2. SOFIST4 operation

The CSA and comparator are reset before each beam collision. If the comparator detects the hit signal after a collision, it triggers the shift register. The shift register outputs REGOUT_1 to 3 are connected to hit-charge and hit-time memories 1 to 3, respectively. A ramping voltage, which is used to record the hit time, is supplied to RAMP_IN. The memories hold the hit-charge and ramping voltage when REGOUT_1 to 3 are asserted. Thus, each pixel can hold information on up to three hits in the 1300 collisions. The voltage in the hit-charge and hit-time memories are read out at 200 ms intervals and transferred to the data acquisition system.

Table 1
Specifications of the SOFIST4 chip.

Pixel size	20 μm × 20 μm
Number of bumps/pixel	4
Array size	104 × 104
Bump density	10k connection/mm^2
Active area	2.08 mm × 2.08 mm
Chip size	4.45 mm × 4.45 mm
Wafer	DSOI (FZ-p)
Wafer thickness	50 μm

3. 3D integration with the gold nanoparticle bumps

To achieve high-density bump bonding, a new bumping method is introduced. Conventionally, such high-density connections are made using indium bumps. However, the indium bump method requires high pressure in order to realize a reliable connection. As the pressure is a limited in order to reduce the stress to the CMOS circuit, it was not possible to achieve a high connection yield.

To improve the quality of 3D integration, a method of using cone bumps made of gold nanoparticles was developed [5]. Fig. 4 shows a schematic of the bump deposition apparatus. Gold nanoparticles are produced in the generation chamber and transferred to the deposition

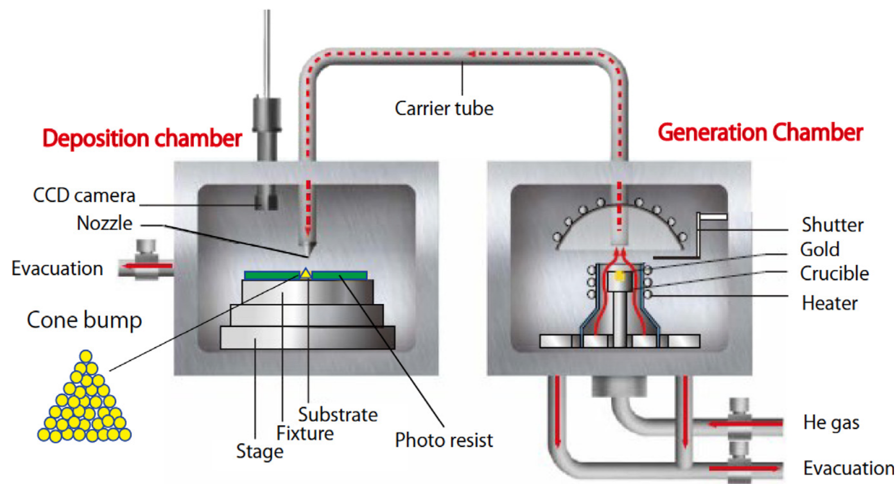

Fig. 4. Schematic of the gold nanoparticle bump development chamber.

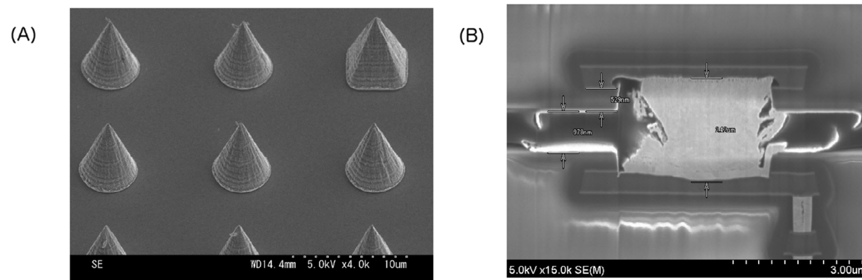

Fig. 5. (A) Typical shapes of the gold bumps. (B) Cut out view of a gold bump after the bonding process.

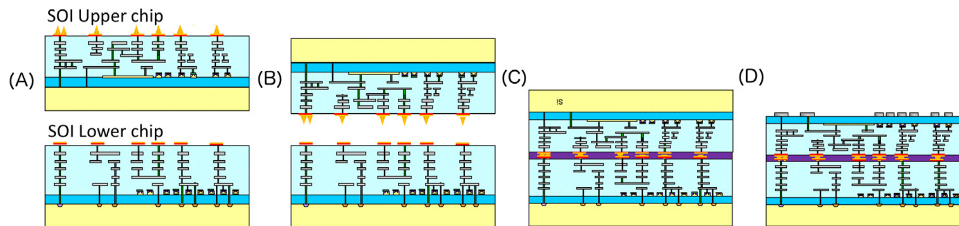

Fig. 6. Procedure for SOI 3D stacking.

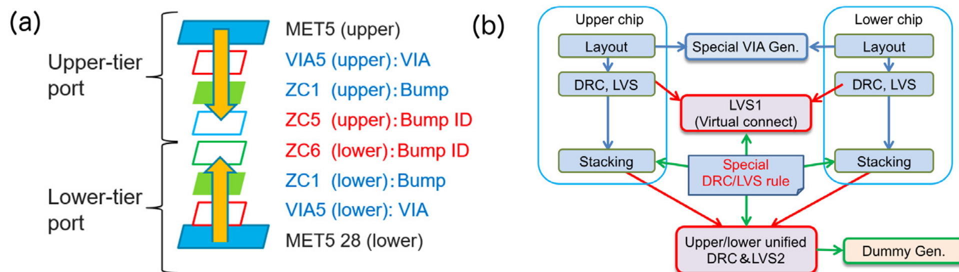

Fig. 7. (a) Virtual layers for the DRC and LVS produced in the 3D CAD. (b) Procedure for the DRC and LVS for 3D stacking.

chamber. The nanoparticles are sprayed through a photoresist on the wafer. They naturally develop into cone-shaped bumps, as shown in Fig. 5(a). The typical size of each bump is 2.5 μm in diameter and 2.5 μm in height. The minimum spacing between bumps is 5 μm. As the bumps are piles of gold nanoparticles, they can be crushed by low pressure, as shown in Fig. 5(b); consequently, the variation of the bump heights can be absorbed, and the stress to the silicon wafer is reduced. Because there is no oxide layer, a high connection yield can be achieved. The connection resistance is typically 0.3 Ω per connection [6].

Fig. 6 shows the procedure for 3D integration. (A) Gold bumps are developed on the upper chip. (B) The upper and lower chips are then placed face to face and aligned. (C) The two chips are pressed so that the cone bumps on the upper chip touch the pads on the lower chip. (D) Finally the silicon part of the upper chip is ground out and the wire bonding pads are developed. Through silicon vias are not necessary in

the SOI 3D integration, because the electrical connections between the top and bottom surfaces can be made naturally.

4. CAD design tools

To design the 3D integration ICs, there have been efforts to extend the existing 2D CAD tools [5]. However, design rule check (DRC) and layout versus schematic (LVS) are indispensable for verifying the design geometrically and logically. For the design of the SOFIST4 chip, a new method is developed [7]. When a user places micro-bump cells like vias, several virtual layers are automatically generated in the upper and lower chips. The virtual layers unify the two chips geometrically, as shown in Fig. 7(a). For LVS, the virtual layer forms circuit nodes between the upper and lower circuits, and the combined circuit verification becomes possible. To proceed with efficient verification, the upper and lower chips should be checked independently. Then the two chips are combined with the virtual layers, and combined verification is be applied, as shown in Fig. 7(b). Dummy bumps, which are necessary for equalizing the stress on the wafer, are generated automatically.

To implement 3D DRC and LVS in the existing LSI CAD tool, only the rule files were modified, and we did not have to develop special tools. In this 3D extension, however, the capabilities of the combined parasitic extractions [8] are still to be implemented.

5. Summary and prospects

The SOFIST4 chip was submitted for an MPW run in June 2017. The wafer will be delivered in February 2018, and the 3D integration will be finished in late 2018, after which evaluation will start. Once the technology is established, a more intelligent pixel sensor, for example, several pixel sensor layers that are unified, will be tested to reconstruct tracks inside the pixel detector. The dense connections between chips could lead to highly parallel data processing.

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