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Development of a radiation tolerant fine pitch planar pixel detector by HPK/KEK

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ABSTRACT

In the recent development of pixel detectors for the inner part of the ATLAS detector upgrade of the High Luminosity LHC, a thin, typically 150 μm, planar pixel detector has been developed. To reduce hit occupancy, the pixel size is smaller compared to the currently operating pixel detector in ATLAS and the 2 pitch options, 50 μm × 50 μm and 25 μm × 100 μm, are readout by the same 50 μm × 50 μm pitch readout ASIC. To evaluate the performance of the fine pitch pixel detector, two methods are tested, a) emulated using the current ASIC (FE-I4) using non-uniform size of pixel, where two 50 μm×250 μm pixels are spitted to 50 μm×50 μm and 50 μm×450 μm, (b) used new ASIC (FE65p2) with full 50 μm×50 μm pitch. The FE65p2 is the prototype ASIC produced by TSMC using 65 nm CMOS process, with an expected lower noise than FE-I4. In this paper, basic devices performance and testbeam results before and after irradiation are presented.

1. Introduction

The physics experimental program Large Hadron Collider (LHC) [1] has been successfully operated for the last seven years, from October 2010–November 2017. The observation of the Higgs boson [2,3] and measurements of its properties [4,5] by ATLAS [6] and CMS [7] were an important milestone for the field of high energy particle physics. For the observation of Higgs coupling through the study of rare decay channels, as well as the Higgs self coupling, further precision of measurements of Higgs sector couplings and electroweak produced Beyond the Standard Model Phenomena are the next target of hadron collider experiments. One of the most powerful planned experiments to probe these topics is the High Luminosity Large Hadron Collider (HL-LHC) [8] which is planned to start in 2026. A plan for upgrading the ATLAS detector at HL-LHC is currently on going. This paper shows the thin, typically 150 μm, and fine pitch pixel (50 μm × 50 μm and 25 μm × 100 μm) silicon sensor developed for the outer part of the planar pixel detector in the ATLAS experiment upgrade for the HL-LHC.

2. ATLAS upgrade tracking detectors

2.1. Pixel detector

The ATLAS Inner Tracking (ITK) detector upgrade project plans to replace all existing ATLAS tracking detectors [9] which consists of silicon pixel detectors, micro-strip detectors and Transition Radiation Trackers to the new silicon detectors with pixel [10] and strip [11] sub-system. The outer part of pixel detector will be built out of Planar type detectors [12,13]. The read out ASIC for the pixel hybrid detectors have been designed by CERN RD53 collaboration [14]. The ASIC is electrically connected to the sensor with bump bonding technology. In this process, ASIC and Sensor are flip chipped after SnAg solder bumps are deposited to the pad on ASIC and under bump metalization (UBM) to the pad on sensor. One pad corresponds to the single electrode and pads are placed two dimensional matrix with 50 μm × 50 μm pitch. According to the structure, the planar pixel sensor with the same matrix pitch pads is designed.

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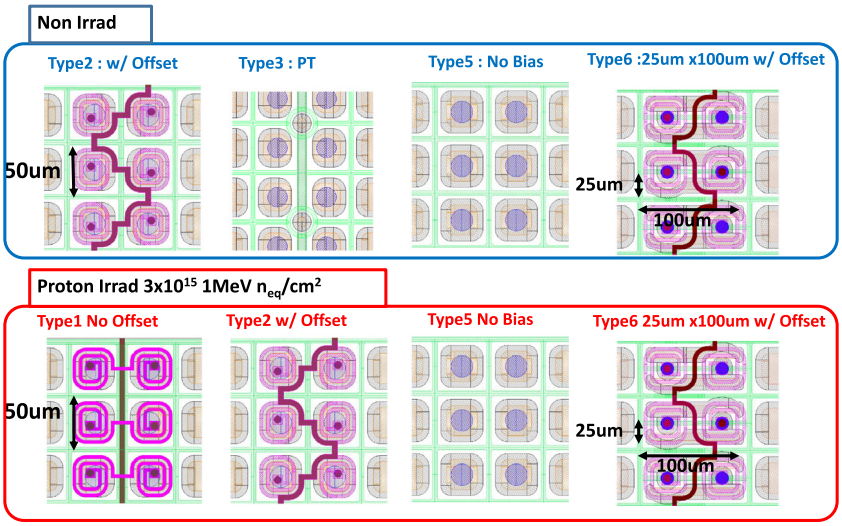


Fig. 1. Various Sensor types of the biasing structure sensors compatible with the FE-I4 ASIC. The top four types were tested before irradiation and the bottom four types have been tested after irradiation. Light and dark magenta show poly-silicon bias resistors and bias rails respectively, the black line with a shadow is the top Aluminum, the orange area located inside of the top Aluminum shows the n^+ implant, and the green line corresponds to the p-stop structure. Typical resistivity value for the bias resistor for each pixel to the bias rail is 600 kΩ. For non-irradiated samples, poly-silicon bias structure, punch-through bias structure and no bias structure types with 50 μm × 50 μm and poly-silicon bias strucutre with 25 μm × 100 μm are compared. For irradiated sample, poly-silicon bias structure with and without offset from pixel boundary, no bias structure with 50 μm × 50 μm and poly-silicon bias strucutre with 25 μm × 100 μm are compared. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Table 1
Comparison of the specifications for the FE-I4 and FE65p2 ASICs. Two thresholds value noted stable threshold and typical threshold showed as the threshold in ASIC specification and the threshold used for the testbeam measurement respectively.

ASIC	FE-I4	FE65p2
ASIC dimension	17 mm × 20 mm	3 mm × 4 mm
CMOS process	130 nm	65 nm
Pixel size	50 μm × 250 μm	50 μm × 50 μm
Pixel matrix	336 × 80	64 × 64
Stable threshold	1500 e^-	500 e^-
(Typical threshold)	2000–3000 e^-	700 e^-

2.2. Planar pixel detector by KEK/HPK

The n^+-in-p type pixel sensors which have Boron-doped electrodes in the Phosphorus-doped bulk have been developed by KEK, with Hamamatsu Photonics K.K. for production of the devices [15–18]. The FE-I4 ASIC [19] which is used for the Insertable B-layer (IBL) detector [20] in ATLAS are used for the development, however the pixel size is five times larger (50 μm × 250 μm) than the pixel size which is used for ITK pixel detector. In this paper, measurements of the first fine pixel size (50 μm × 50 μm) devices are presented.

3. Fine pitch pixel detector design

The fine pixel size (50 μm × 50 μm) measurement could be achieved by using two methods, a) using the FE-I4 ASIC but two 50 μm × 250 μm pixels are divided to 50 μm × 50 μm and 50 μm × 450 μm, b) using the new FE65p2 ASIC [10]. The specification difference for the FE-I4 and FE65p2 are summarized in Table 1. The critical efficiency loss is observed at the pixel boundary region due to the charge sharing effect and bias structure [18] and the effect is more visible for the finer pixel detector simply because the relative amount of pixel boundary areas increases. To this end, the efficiency measurement of the fine pitch pixel detector has been performed. The efficiency measurement results presented in Section 5 are performed for the sensor with thickness of 150 μm as per the planned design of the outer barrel region of the upgraded detector.

3.1. FE-I4 ASIC small pitch adapted sensors

As shown in Fig. 1, various types of the biasing structure sensors are designed as optimized poly-silicon bias resistor (FE-I4 type 2) and no bias structure (FE-I4 type 5) with a 50 μm × 50 μm pixel size. A similar optimized poly-silicon bias resistor with 25 μm × 100 μm (FE-I4 type 6) is also tested. These three types are compared before and after proton irradiation at the fluence of 3×10^{15} 1 MeV n_{eq}/cm^2. Instead of the poly-silicon bias resistors, punch-through structure [16] (FE-I4 type 3) has also been compared for the case of before irradiation. The poly-silicon bias resistor type but with the bias rail located at the pixel boundary (FE-I4 type 1) is also tested for the comparison of measurements on irradiated samples.

3.2. FE65p2 ASIC small pitch native modules

FE65p2 ASIC compatible sensors are produced and compared for various bias structures as shown in Fig. 2. The FE65p2 type 2 and FE65p2 type 5 described above are compared before and after irradiation. In addition to this, FE65p2 type 1 and FE65p2 type 6 structures are tested after irradiation. A sample with no biasing structure and 25 μm × 100 μm pixel size (FE65p2 type 8) is also compared after irradiation.

4. Irradiation and testbeam

To qualify the radiation tolerance of the pixel detector, proton irradiation at Cyclotron and Radioisotope Center (CYRIC) facility operating at Tohoku University and subsequent measurements at a testbeam at CERN Super Proton Synchrotron (SPS) has been carried out.

4.1. Irradiation at CYRIC Tohoku University

A proton irradiation facility, Cyclotron and Radioisotope Center (CYRIC) at Tohoku University, is used to irradiate the pixel modules. The high intensity proton beam with a momentum of 70 MeV/c and typically 300 nA beam current is used for the irradiation. The temperature is maintained at −15 °C by a cold nitrogen gas flow. The irradiation is uniform in the module (consists of sensor and ASIC) plane and in depth. The detailed setup and fluence control are described in Ref. [18].

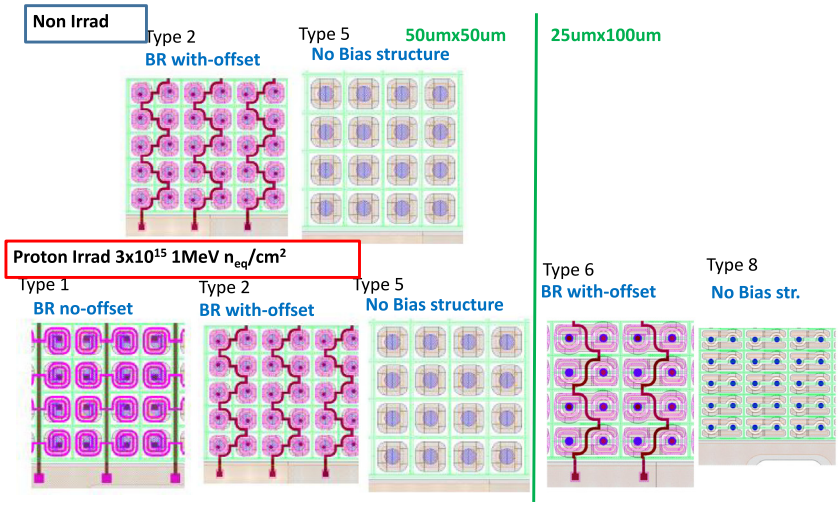


Fig. 2. Various sensor types of the biasing structure sensors compatible with the FE65p2 ASIC. The top two types are tested before irradiation, and the bottom five types are tested after irradiation. Colors are the same as in Fig. 1. For non-irradiated samples, poly-silicon bias structure and no bias structure types with 50 μm × 50 μm are compared. For irradiated samples, poly-silicon bias structure with and without offset from pixel boundary, no bias structure with 50 μm × 50 μm, and poly-silicon bias structure and no bias structure types with 25 μm × 100 μm are compared. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Table 2
The overall and center efficiency of irradiated FE-I4 samples for each types. Fluence for all sensors are 3×10^{15} 1 MeV n_{eq}/cm^2. The uncertainties are statistical only.

	FE-I4 type 1	FE = I4 type 2	FE = I4 type 5	FE = I4 type 6
Overall efficiency	89.34 ± 0.05%	93.87 ± 0.04%	97.12 ± 0.03%	96.93 ± 0.02%
Center efficiency	99.04 ± 0.08%	99.19 ± 0.07%	99.33 ± 0.07%	99.23 ± 0.02%

4.2. Testbeam at CERN

The testbeam facility at the Super Proton Synchrotron (SPS) at CERN with a 120 GeV pion beam was used. In order to measure the efficiency of pixel detectors a precise pointing resolution of the particle passing through is needed. For the EUDET telescope with Mimosa-26 sensors [21–23] are placed in the beam line, and the device under test (DUT) is installed in between. At typical pointing resolution for this setup is 4.5 μm. Operation of FE-I4 chip kept comparator threshold to 2400 e^- and 3000 e^- for non-irradiated and irradiated samples, respectively. For comparison, a 2200 e^- comparator threshold could be achieved for a few data taking runs for irradiated samples. As a default connection, the bias structure is set to be electrically floating but virtually grounded to an ASIC amplifier of the ASIC via bump bonding connection. For comparison, the bias structure is set to ground for a few data taking runs for irradiated samples. In case of the bias structure is set to ground, lower efficiency is expected due to the ground potential except electrode on the surface makes to hinder the charge correction. In the cases with the FE65p2 chip, the comparator threshold is set to 700 e^- for both non-irradiated and irradiated samples.

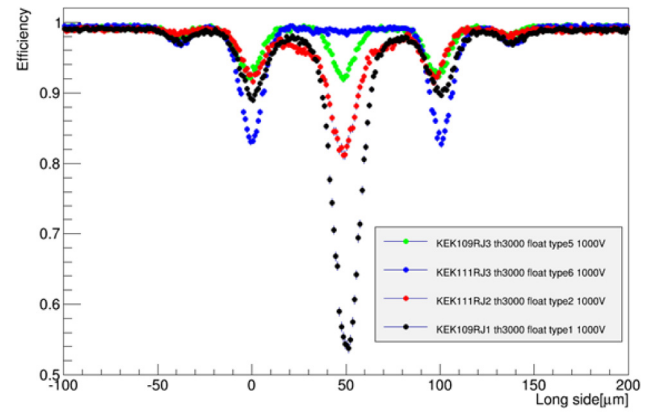
5. Results

5.1. FE-I4 ASIC small pitch adapted sensors

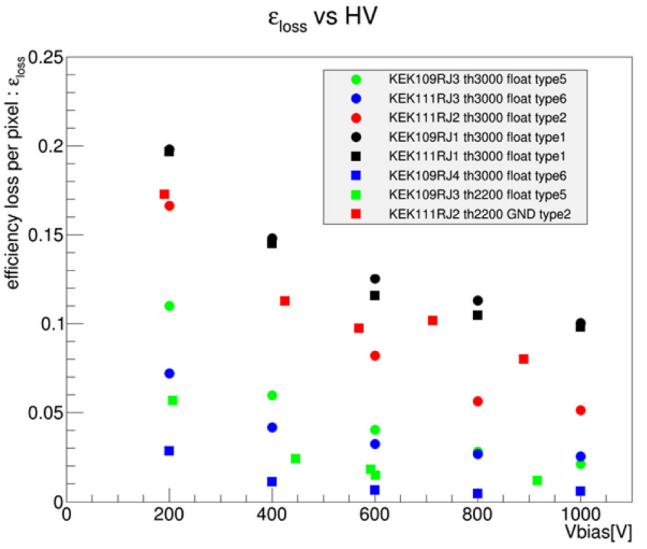
Overall efficiency for various types of bias structures are evaluated using all tracks pointing to the good pixels which are not masked nor noisy. Efficiency using all the tracks pointing to the pixel center defined as 3 sigma of pointing resolution away from pixel boundary is evaluated as center efficiency. All efficiencies for non-irradiated samples are over 99%, except the overall efficiency for FE-I4 type 3 structure which is 94.8%, due to the punch through structure. The overall and center efficiency for irradiated samples are shown in Table 2. All center efficiency for various types are over 99%. The 2.2% efficiency loss is evaluated to be due to the charge sharing effect by comparing overall and center efficiency for FE-I4 type 5 which does not have any biasing structure. An additional 3.5% efficiency loss due to the FE-I4 type 2 bias strucutre is evaluated by comparing overall efficiency between FE-I4 type 2 and FE-I4 type 5. In the FE-I4 type 6 case with pixel size of 25 μm × 100 μm, the efficiency loss is 2.3% including both the charge sharing and bias structure effect. This is simply because the bias structure is not passing close to the pixel corner, where the produced charge is supposed to share to four pixels, unlike the 50 μm × 50 μm pixel size case. To check the reason of the efficiency loss, positions this dependence of the efficiency is shown in Fig. 3(a). At 0, 50 and 100 μm position corresponds to the pixel boundary, while the bias resistor is located at 50 μm. The FE-I4 type 5 (green dots) efficiency drops equally for all three pixel boundaries due to the charge sharing, while FE-I4 type 2 (red dots) shows a larger efficiency drop at the 50 μm location due to the bias structure. The FE-I4 type 6 (blue dots) have a smaller efficiency drop at the 50 μm position since no corner exists for the 25 μm × 100 μm case. For type 1 (black dots), about a three times larger efficiency drop is observed at the bias structure than for FE-I4 type 2. The efficiency drop as a function of detector bias is shown in Fig. 3(b). Certainly the lower comparator threshold runs show a smaller efficiency loss when compared with a threshold of 2200 e^- (green square) and a threshold of 3000 e^- (green circle). The grounding bias structure (red square) shows worse performance than floating bias structure (red circle) due to the ground potential except electrode on the surface makes to hinder the charge correction.

5.2. FE65p2 ASIC small pitch native modules

All the efficiency losses using the FE-I4 ASIC are expected to improve due to the lower comparator threshold, 700 e^- when using the FE65p2 module. Although the overall efficiencies measured with the FE65p2 are lower than FE-I4 due to the ASIC problem which appeared due to the timing issue of chip operation, relative efficiency in the position dependence has to be kept to the same. Since center efficiency is expected to be over 99%, the measured efficiency is normalized to 100% at the center region of the pixel defined as 3 sigma of pointing resolution away from the pixel boundary. Figs. 4(a) and 4(b) show position dependence of the measured efficiency obtained by FE65p2 modules for 25 μm × 100 μm and 50 μm × 50 μm pixel size, respectively. Since no significant efficiency loss at the pixel boundary is observed with a bias voltage over 600 V, the upper limit of the efficiency loss for

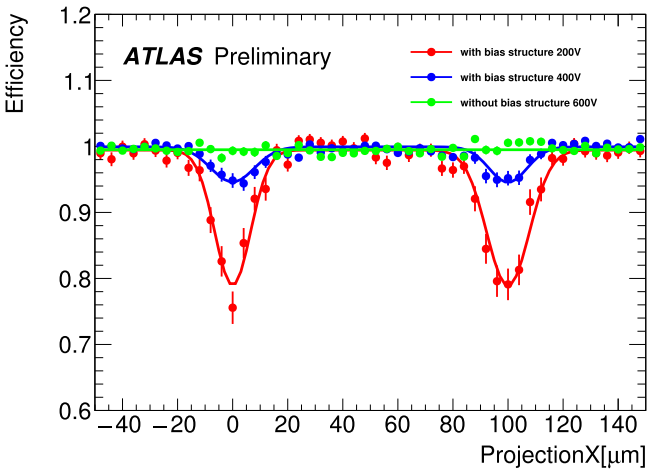


(a) Position dependence.

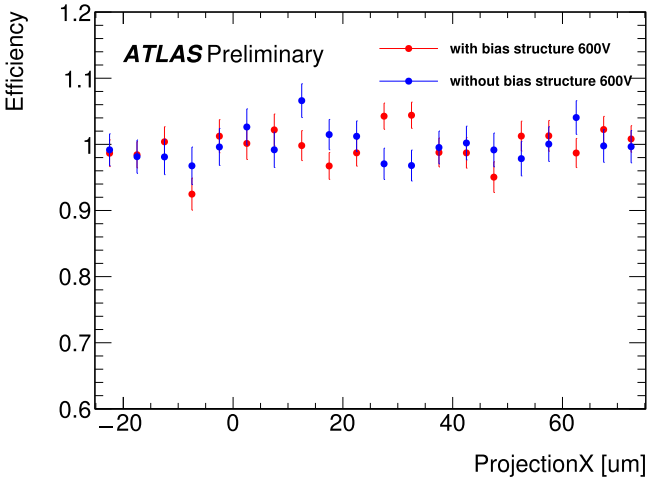


(b) Bias voltage dependence.

Fig. 3. (a) Position dependence of the efficiency for the sensors compatible with the FE-I4 ASIC. At 0, 50 and 100 μm position correspond to the pixel boundary while bias resistor exists at 50 μm as shown in Fig. 1 each color corresponds to the bias type as shown in the legend. (b) Bias voltage dependence of the efficiency loss. each color corresponds to the biasing type and comparator threshold value and floating/grounding bias structure are validated.. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)



(a) 25 μm × 100 μm



(b) 50 μm × 50 μm

Fig. 4. The relative efficiency to the efficiency of center region as a function of relative position to the pixel boundary for the sensors compatible with the FE65p2 ASIC. a) is for 25 μm × 100 μm while the red and blue lines correspond to the sensor with bias structure and detector bias 200 V and 400 V. The green line corresponds to the sensor without bias structure and 600 V. b) is for 50 μm × 50 μm while red and blue correspond to with and without bias structure respectively.. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

25 μm × 100 μm and 50 μm × 50 μm pixel size with bias strucutre are evaluated as 0.5% and 1%, respectively relative to the efficiency at the center of pixel region.

6. Conclusion

In the development of the ATLAS pixel detector upgrade, optimization of the sensor structure has been presented. The efficiency measurements of fine pitch pixel detectors with 50 μm × 50 μm and 25 μm × 100 μm pixel size, have been performed before and after proton irradiation (3×10^{15} 1 MeV n_{eq}/cm^2). The efficiency loss at the pixel boundary region largely depends on the biasing structure of the sensor and comparator threshold of the readout ASIC. In the case of 3000 e^- threshold with the optimized biasing structure (FE-I4 type 2), 2.2% efficiency loss by charge sharing effect and 3.5% efficiency loss by bias structure effect was observed. The lower comparator threshold value, 2200 e^-, shows clear improvement of the efficiency. The prototype ASIC which is expected to have a close threshold value, 700e^-, to the ASIC for the final ATLAS pixel upgrade detector, results in a smaller efficiency loss than the FE-I4 ASIC. No significant efficiency drop at the pixel boundary was observed with the comparator threshold 700e^- by the FE65p2 ASIC after irradiation. Results conclude that the fine pitch pixel sensor, 50 μm × 50 μm or 25 μm × 100 μm pixel size, produced by HPK/KEK with the low noise ASIC (set the comparator threshold 700e^-) should fully satisfy the requirement of the ATLAS pixel detector upgrade.

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