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Noise evaluation of silicon strip super-module with ABCN250 readout chips for the ATLAS detector upgrade at the High Luminosity LHC

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ABSTRACT

Toward High Luminosity LHC (HL-LHC), the whole ATLAS inner tracker will be replaced, including the semiconductor tracker (SCT) which is the silicon micro strip detector for tracking charged particles. In the development of the SCT, integration of the detector is the important issue. One of the concepts of integration is the “super-module” in which individual modules are assembled to produce the SCT ladder.

A super-module prototype has been developed to demonstrate its functionality. One of the concerns in integrating the super-modules is the electrical coupling between each module, because it may increase intrinsic noise of the system. To investigate the electrical performance of the prototype, the new Data Acquisition (DAQ) system has been developed by using SEABAS. The electric performance of the super-module prototype, especially the input noise and random noise hit rate, was investigated by using SEABAS system.

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1. Introduction

The Large Hadron Collider (LHC) at CERN is the world's highest energy particle accelerator. In order to significantly increase the integrated luminosity during one additional decade, the High Luminosity LHC (HL-LHC) project is already planned. At the HL-LHC, the instantaneous luminosity will be improved by at least a factor of five (up to $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$). ATLAS is one of the general purpose detectors of the LHC, and it will be upgraded for its operation at the HL-LHC. For the upgrade, the current inner

tracking detectors of ATLAS will be replaced by an all silicon-based tracker [1].

The SemiConductor Tracker (SCT) is one of the sub-systems of the ATLAS inner tracker and consists of silicon micro-strip detector modules [2]. The SCT will be upgraded for the HL-LHC. To evaluate the performance, prototypes of each elements have been developed.

One of the integration concepts for the upgraded strip detector is the “super-module”. In the super-module concept, a SCT ladder consists of individual double-sided silicon micro-strip modules aligned on the support frames. Each double-sided strip module is a top–bottom symmetric object composed of two silicon micro-strip sensors glued back-to-back to a central Thermo-Pyrolitical-Graphite (TPG) baseboard and hybrids with readout ASICs bridged on the top

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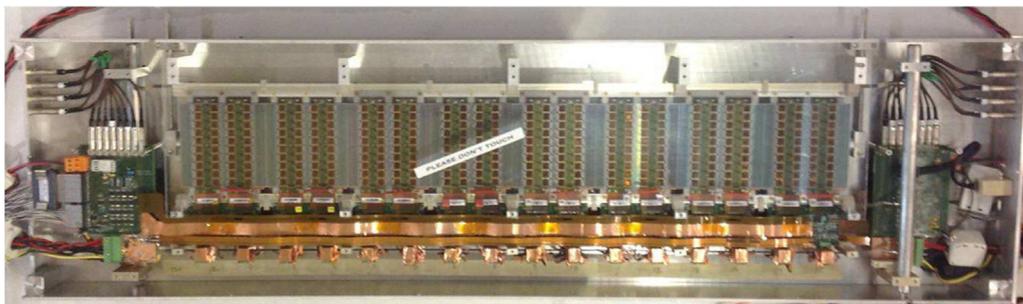


Fig. 1. Super-module prototype populated with eight double-sided strip modules.

of the sensors. Since each module is electrically and thermally decoupled, the detector can be stable in the operation.

A super-module prototype has been developed to demonstrate its electrical functionality (Fig. 1) [3]. One of the concerns for the integration is to try to avoid any electrical coupling between modules, as this may increase the intrinsic noise of the system. To investigate the electrical performance of the prototype, a new data acquisition system has been developed by using a multi-purpose DAQ board called SEABAS [4]. In this paper, the electrical performance of the super-module prototype as measured with the SEABAS system is described.

2. The system setup

2.1. The super-module prototype

The super-module prototype (see Fig. 1) consists of 8 double-sided silicon micro-strip modules, 16 BCC boards, 2 Super-Module Boards, 32 DC–DC power converters, 2 sets of three types of bus tapes and cooling pipes. These electrical components are mounted on an aluminum support structure.

ATLAS07 [5] is the new radiation-tolerant strip sensor used for the super-module prototype. ATLAS07 is produced in 6-in. wafers by Hamamatsu Photonics. The sensor has a n-on-p structure and its dimension is about $10 \times 10 \text{ cm}^2$. The sensor contains four rows of 1280 strips each with a single strip dimension of $2.38 \text{ cm} \times 74.5 \mu\text{m}$. The super-module prototype shown in Fig. 1 has more than 80,000 strip channels in total.

The signals from a sensor are processed by the ATLAS Binary Chip Next 250 (ABCN250) [6] readout ASICs produced in 250 nm CMOS technology. An ABCN250 chip has 128 readout channels, and the chips are mounted in two columns of ten on the hybrid (Fig. 2). The ABCN250 amplifies the signals from a sensor and outputs a binary hit information at 40 or 80 MHz clock frequency.

The Buffer Control Chip (BCC) distributes operation signals from the data acquisition system to two columns of ten ABCN250s and multiplexes their output signals at 80 or 160 MHz. Two BCCs are mounted on a BCC board which is an interface board between two hybrids and the bus service tapes.

The low-voltage required to power the ABCN250s is provided by SM01C DC–DC converters [7]. Each converter supplies a fixed

output voltage of 2.5 V by dropping the input voltage of 12 V provided externally through the low-voltage bus.

Three different types of bus tapes have been produced at CERN and used in the super-module prototype. A data bus distributes the common LVDS signals to control both BCCs and ABCN250s, and it receives each multiplexed data stream coming from up to 16 BCCs. A high-voltage bus supplies the bias voltage to each sensor individually and a low-voltage bus is used for powering the DC–DC converters. Two sets of three different bus tapes are used for the top and bottom sides of the super-module prototype [3].

A Super-Module Board (SMB) interfaces the off-detector high- and low-voltage power lines and external control signals to the bus tapes. One SMB is used for one side of the super-module. Two Analog-to-Digital Converters (ADCs) are mounted on the SMB to measure the temperature of each hybrid via its corresponding surface-mounted thermistor.

The High-Voltage (HV) is supplied by iseg EHS8210n-F eight-channel HV-supply card loaded in ECH224 crate. The high- and low-voltage power-supplies are operated through a custom-made National Instruments-LabVIEW [8] based control system.

2.2. The SEABAS system

A new Data Acquisition (DAQ) system has been developed in order to evaluate the performance of the super-module prototype by using a SoI Evaluation BoArd with Sitcp (SEABAS). SEABAS has been developed as a multi-purpose DAQ board (Fig. 3). SEABAS has two FPGAs (Virtex-4 XC4LVX25-10FF668) for user-FPGA and SiTCP [9]. The users can implement any logic into the user-FPGA to operate devices under test and process their output data. SiTCP is used for communication between the user-FPGA and a computer.

SiTCP is a technology to realize TCP/IP and UDP communication only with hardware logic in a FPGA without using any processor. This allows Ethernet communication with low power consumption. The maximum data transfer rate of TCP/IP with SiTCP in our system is 100 Mbps by using 25 MHz operation clock and 1 Gbps with the

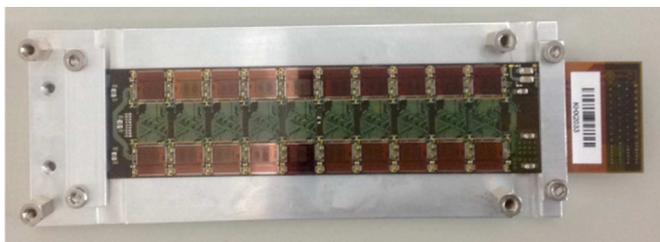


Fig. 2. Picture of a hybrid containing 20 ABCN250 readout chips.



Fig. 3. Picture of the SEABAS board.

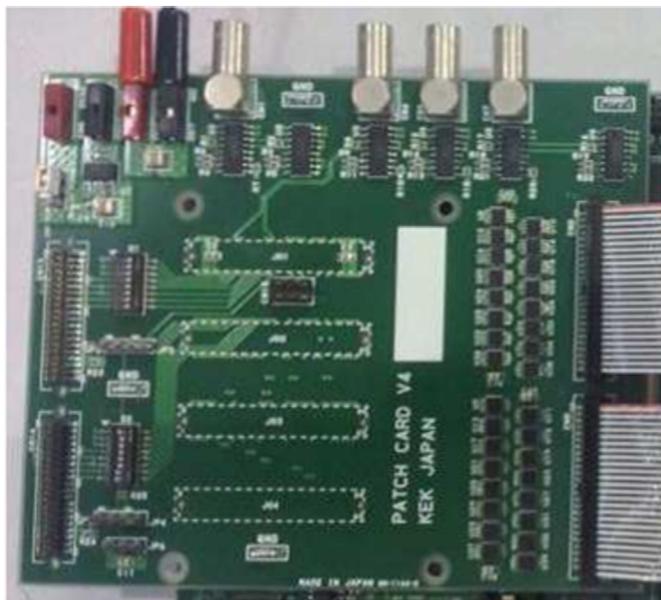


Fig. 4. Patch card for the super-module prototype.

latest version of the SiTCP. UDP communication is used for slow control due to its slow operation clock of 500 kHz.

The patch card (Fig. 4) was developed as the interface between the super-module prototype and SEABAS. Two data buses are jointed with two 64-pin connectors to send operation signals from SEABAS and data from hybrids both for top and bottom sides.

Our DAQ system is designed to make logic implemented in user-FPGA as simple as possible, keeping the data processing speed high enough. For that purpose, the encoding and decoding of commands and output data from the hybrids is done via software. The user-FPGA just generates operation signals for the front-end chips, receives data from them and stores them into a FIFO memory. The data in the FIFO memory are sent to SiTCP with the specific protocol and transferred to the computer via Ethernet. This simple design of the firmware in user-FPGA allows to use the same firmware to test different chips, requiring us to change only design of the software in a computer.

3. The evaluation of the system

3.1. The scan and the optimization

The parameters of the chip configuration need to be optimized to operate the chips correctly. For that reason, the functionalities

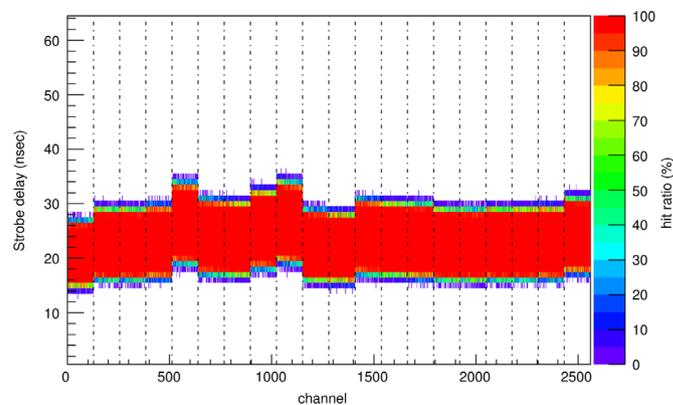


Fig. 6. Results of strobe delay scan for hybrid 0.

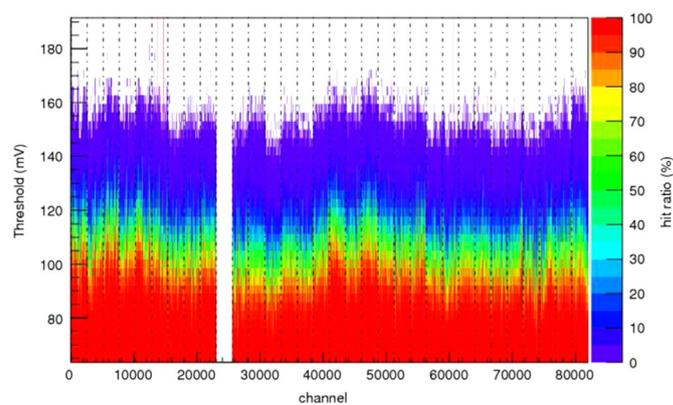


Fig. 7. Results of threshold scan before trim scan.

to scan the chip parameters are implemented into our readout system.

The first optimization is for the readout timing. It is optimized by setting two parameters, i.e., latency and strobe delay. The readout chip stores hits into a pipeline which has 255 clock length. Once a trigger is injected into the chip, the hits in the pipeline corresponding to a certain time period before injecting the trigger (latency) are output. In the latency scan, the number of hits in each strip channel is checked as a function of the latency as shown in Fig. 5. In Fig. 5, latency of 112 is the optimal timing for readout.

After the latency scan, the timing of the injection pulse with respect to the clock phase is adjusted by using strobe delay. Fig. 6 shows the hit efficiency as a function of strobe delay for each strip channels. The rising edge (T_{up}) and falling edge (T_{fall}) of the region with 100% efficiency are used to find the optimal value of the strobe delay (T_{opt}), i.e., $T_{opt} = (T_{fall} - T_{up})/4 + T_{up}$.

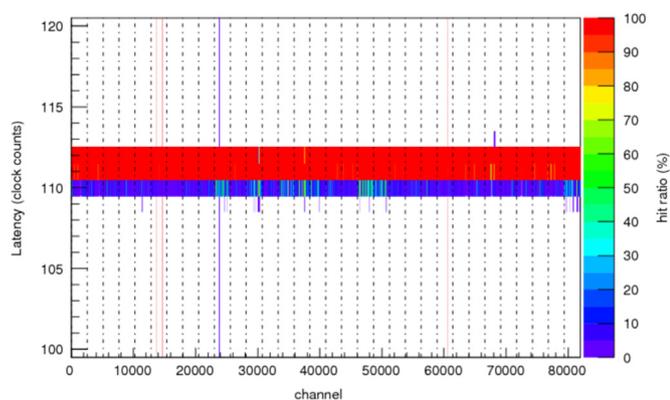


Fig. 5. Results of latency scan.

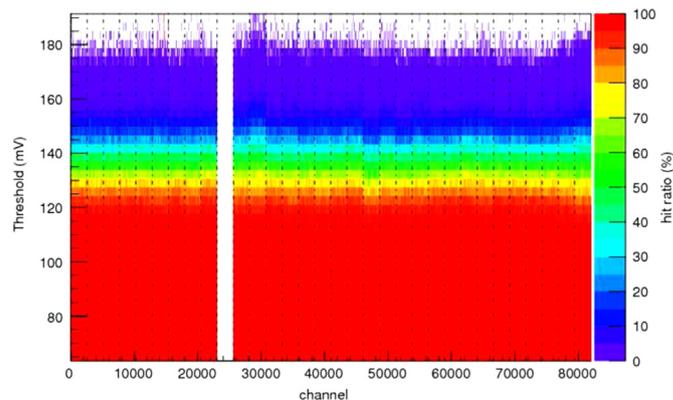


Fig. 8. Results of threshold scan after trim scan.

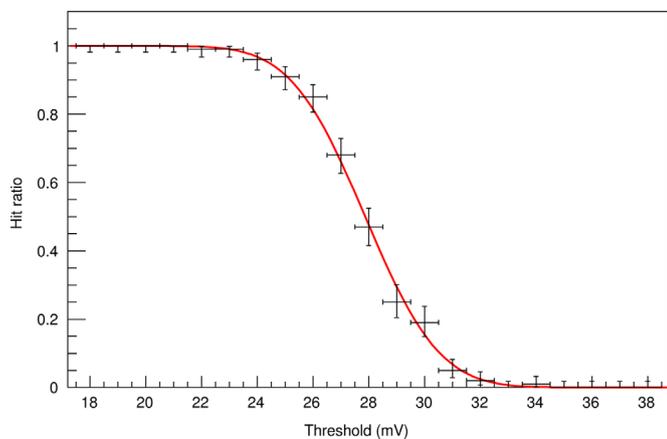


Fig. 9. S-curve for a typical strip channel.

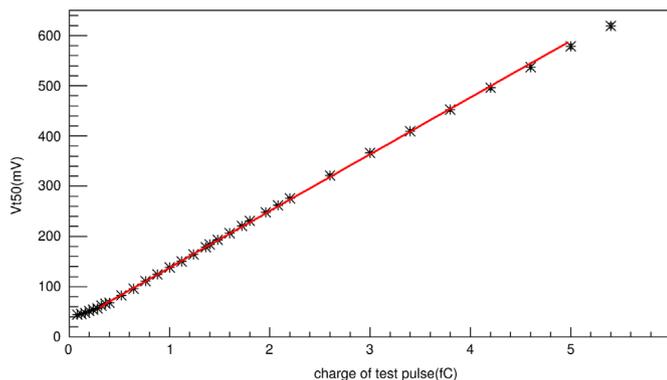


Fig. 10. Response curve for a typical strip channel.

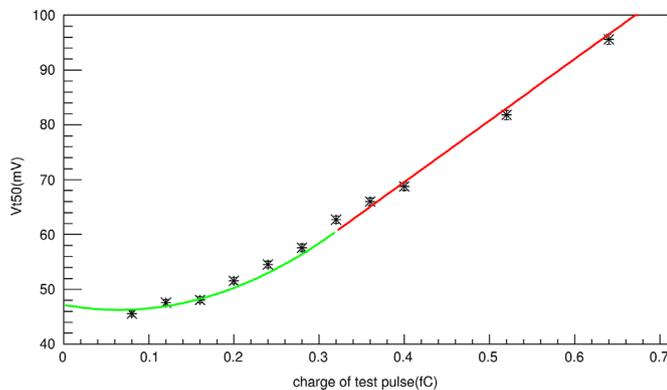


Fig. 11. Response curve in low threshold. Linearity is lost in lower threshold region. Quadratic function is used as fitting function for such region.

The last optimization is the trim scan. Before the trim scan, as shown in Fig. 7, the results of the threshold scan for each channel has a different threshold voltages to obtain 50% hit efficiency, which is called V_{t50} , because of different offset of threshold for each channel. The trim scan is determining an offset for each channel so that to achieve a uniform V_{t50} across all the chips. After the optimization, as shown in Fig. 8, the uniform V_{t50} are obtained.

3.2. The evaluation of the performance

In order to evaluate the electrical performance of the super-module prototype, the noise performances were estimated by the distribution of hit ratio as a function of the threshold for a given input charge for a given channel (so called S-curve, see Fig. 9). By fitting the S-curve as shown in Fig. 9 to a complementary error

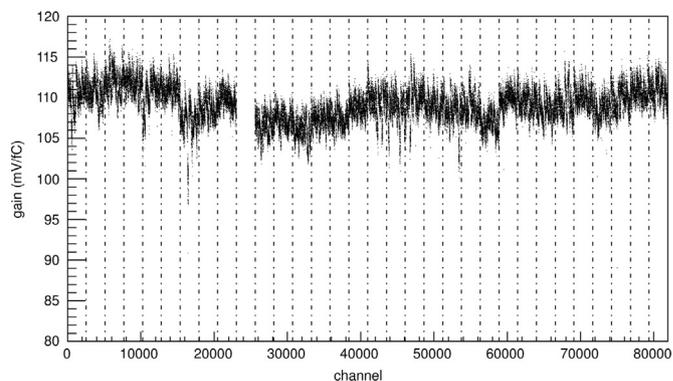


Fig. 12. Gain distribution for all the modules. The dotted lines indicate the boundary between the hybrids.

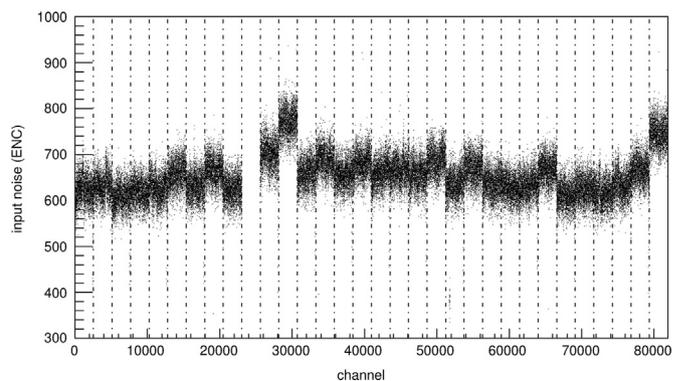


Fig. 13. Input noise distribution for all the modules. The dotted lines indicate the boundary between the hybrids.

function, the standard deviation of the fitting function represents the input noise. The standard deviation is in unit of voltage, but the scale of voltage is depend on individual differences of pre-amplifier for each channels. Therefore, the input noise is evaluated in unit of equivalent noise charge (ENC). To evaluate the input noise in unit of ENC, the gain is used. The gain is determined from the slope of the response curve of the threshold scan, as shown in Fig. 10. The response curve has a good linearity around the nominal operation threshold of 1 fC, however, loses its linearity in lower threshold region as shown in Fig. 11. The gain is, therefore, obtained from the fitting result around that linear region. The input noise is determined as standard deviation, which is obtained from the S-curve fitting with 1 fC test pulse, divided by the gain. The response curve is measured for all the modules except for hybrid 9 which had a problem in the powering with the DC-DC converters.

Fig. 12 shows distribution of the gain for all the modules. The average of the gain is 109 mV/fC. Fig. 13 shows distribution of the input noise for all the modules. In Fig. 13, hybrid 11 (from 28,160 channel to 30,719 channel) and hybrid 31 (from 79,360 channel to 89,119 channel) have large input noise which is assumed due to large noise created by the pulse generator in chip as discussed later.

Except for hybrid 11 and hybrid 31, the average noise was 644 electrons. Only 0.3% of channels had an input noise larger than the specification value of the chip (750 electrons) [10]. The strips with noise higher than 750 electrons localize at certain area, therefore, damage on the sensor is assumed to be the reason of the high noise.

The results shown in Fig. 13 were obtained by the measurement with all the modules at the same time (simultaneous measurements). To evaluate cross-talks between hybrids and chips, we

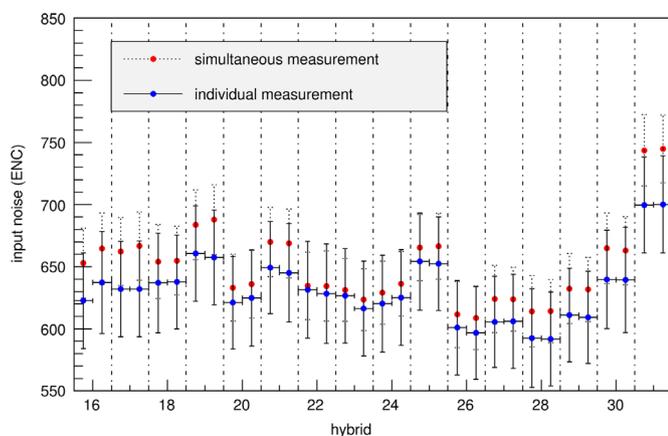


Fig. 14. The input noise obtained in individual and simultaneous measurements. Each point shows a noise value averaged over ten chips at each column in the hybrids at the bottom side. The dotted lines indicate the boundary between each hybrid.

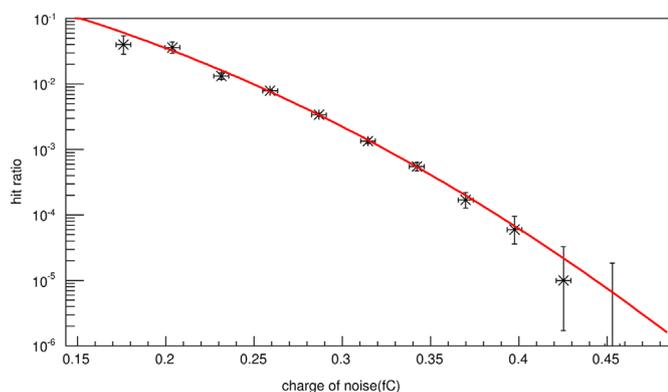


Fig. 15. Noise occupancy plot for a typical strip channel.

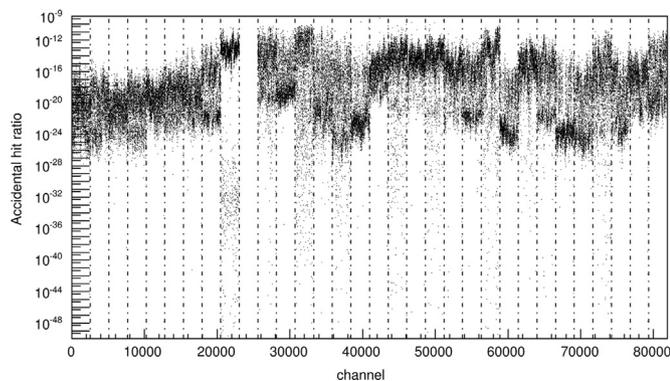


Fig. 16. Accidental hit ratio at 1 fC. The dotted lines indicate the boundary between the hybrids.

performed response curve measurements for each hybrid on the bottom side of the super-module one by one without enabling the other hybrids (individual measurements). In order to save measurement time, only three points were taken for the response curve in individual measurements. Fig. 14 shows the input noise obtained in individual and simultaneous measurements. Each point shows a noise value averaged over ten chips at each column in the hybrids at the bottom side. Larger input noise was obtained in simultaneous measurements on average. The differences of the averages between simultaneous and individual measurements were found to range between from 0.5% to 6.0%. The same channel in the power-supply is used to provide power for operating all DC-DC converters in one side, therefore, DC-DC converters in the

same side are electrically coupled. For that reason, the DC-DC converter can pick up electrical noise from the others in the same side which are operated simultaneously. That is assumed in the source of higher input noise in the simultaneous measurement than individual measurement.

As the last test, we performed a noise occupancy scan which is a threshold scan without any injected test charge to evaluate random hit ratio. Since the random hit ratio is assumed to be low, at most 10^6 triggers were sent at each threshold, then for each channel, a noise occupancy plot was obtained as shown in Fig. 15. Since the random hit is observed only in low threshold regions, each threshold value was converted to equivalent charge by using the response curve shown in Fig. 11. Each noise occupancy plot is fitted with $\exp(-\frac{(Q-Q_0)^2}{2\sigma^2})$, then random hit ratio at $Q=1$ fC was calculated.

Fig. 16 shows the random hit ratio at the threshold of 1 fC for all the modules. Hybrid 11 and hybrid 31 have the same level of the random hit ratio compared to the other hybrids, and it is inconsistent with higher input noise in these hybrids in response curve measurements shown in Fig. 13. The big difference of the input noise between each hybrid in response curve measurements is assumed to be caused by the noise generated by the pulse generator in the chip. The random hit ratio is evaluated by extrapolating fitting function to 1 fC in noise occupancy plot shown in Fig. 15, and the fitting error on the hit ratio is less than 30% for more than 96% of the channels, and the evaluated random hit ratio distributes much wider. For that reason, the fitting error is negligible. The random hit ratio is less than 10^{-13} for more than 90% of channels and 10^{-9} at the maximum.

4. Summary

The super-module concept is one of the integration concepts of the ATLAS SCT upgrade for the HL-LHC. A new simple DAQ system has been developed by using SEABAS to investigate electrical performance of the super-module prototype. The entire system was successfully controlled and readout by the SEABAS system. Furthermore, simultaneous and individual threshold scans and noise occupancy scans were performed.

Two hybrids have larger input noise than the other as observed in the response curve of the threshold scan presumably due to problem in DC-DC converters. Except for these two hybrids, the average of the input noise is found to be 644 electrons, with only 0.3% of the channels having larger noise than the specification value.

In reading out the modules individually, the noise decreased by up to 6.0%, compared with the results of the simultaneous readout. It is assumed that the differences came from DC-DC converters. More than 90% of channels had lower random hit ratio than 10^{-13} .

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