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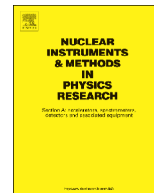

Characteristics of non-irradiated and irradiated double SOI integration type pixel sensor

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ABSTRACT

We are developing monolithic pixel sensors based on a 0.2 μm fully depleted silicon-on-insulator (FD-SOI) technology for high-energy physics experiment applications. With this SOI technology, the wafer resistivities for the electronics and sensor parts can be chosen separately. Therefore, a device with full depletion and fast charge collection is realized. The total ionizing dose (TID) effect is the major challenge for application in hard radiation environments. To compensate for TID damage, we introduced a double SOI structure that implements an additional middle silicon layer (SOI2 layer). Applying a negative voltage to the SOI2 layer should compensate for the effects induced by holes trapped in the buried oxide layers. We studied the recovery from TID damage induced by ^{60}Co γ and other characteristics of the integration-type double SOI sensor INTPIXh2. When the double SOI sensor was irradiated to 100 kGy, it showed a response to the infrared laser similar to that of a non-irradiated sensor when we applied a negative voltage to the SOI2 layer. Thus, we concluded that the double SOI sensor is very effective at sufficiently enhancing the radiation hardness for application in experiments with harsh radiation environments, such as at Belle II or ILC.

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1. Introduction

1.1. Silicon-on-insulator pixel sensor

Monolithic pixel sensors are very attractive for high-energy physics applications for various reasons. Primarily, the metal bump-bonding used in hybrid-type pixel sensors is eliminated; this enhances the device reliability while reducing the production cost. It also reduces the overall device thickness, which minimizes the multiple scattering of the charged particles, and helps reduce the noise level owing to smaller detector capacitances realized by minimizing the pixel size. Monolithic technology is essential to realizing pixel sensors with small pixel sizes, which is a key requirement in future experiments for better position resolution on the order of 1 μm.

We have been developing monolithic pixel sensors [1–3] based on 0.2 μm fully depleted silicon-on-insulator (SOI) technology for various applications such as medical and material sciences [4]. The sensors are processed by Lapis Semiconductor Co., Ltd. [5] on SOI wafers fabricated with SOITEC SmartCut™[6] technology. The schematics of the SOI pixel sensor are illustrated in Fig. 1. The SOI silicon layer and handle wafer are bonded via a buried oxide (BOX) layer; thus, the resistivities can be chosen based on requirements of individual applications. The pixel nodes are implanted via a 200-nm-thick BOX layer to the handle wafer, which acts as the sensor substrate. The figure shows additional silicon layer (middle silicon), which is a new feature of double SOI pixel sensor described in detail in the following section.

Various types of SOI wafers have been developed for single SOI, including both n- and p-type Czochralski (Cz) and float-zone (FZ) grown wafers, as sensor substrates. The sensor thickness ranges from 50 to 500 μm. The double SOI wafer is realized with a Cz substrate.

Complementary metal-oxide semiconductor field-effect transistors (CMOS FETs) are constructed in the SOI silicon layer of 40 nm thickness. The FETs are interconnected by aluminum lines in the five metal layers on top; metal–insulator–metal (MIM) capacitors are also available. The buried p-well (BPW) is a key technology for suppressing the back-gate effect [1], where the detector bias applied to the back affects the operation of electronic circuitry.

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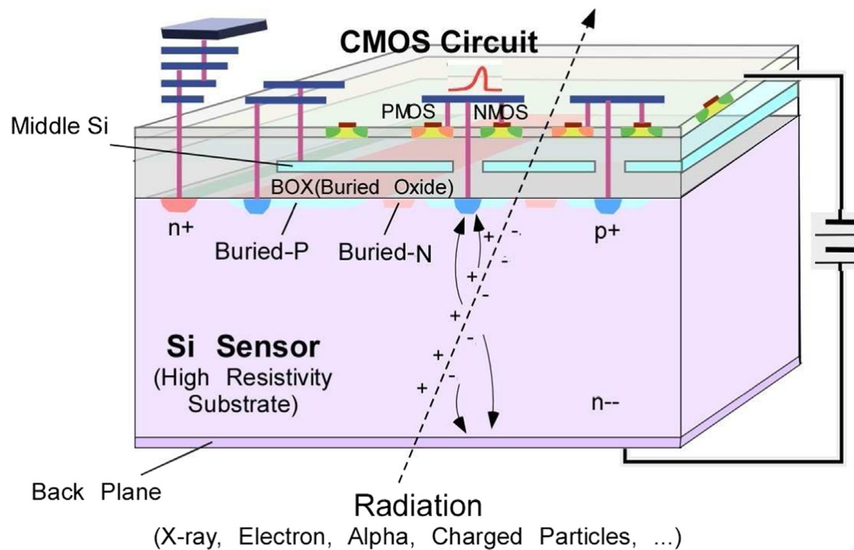

Fig. 1. Schematics of monolithic double SOI pixel sensor.

1.2. Double SOI device

The operation of CMOS devices is affected by the total ionization dose (TID) effect [7], which is primarily due to the accumulation of holes in the oxide layers. SOI-CMOS devices are fully enclosed in an insulator, which almost diminishes radiation damage such as single-event effects [8]. On the other hand, the TID damage is enhanced in the SOI-CMOS [9], which typically limits the operation of pixel devices up to a few kGy [10]. To use such devices for high-energy physics applications in hard radiation environments, the TID effect is a major issue to overcome. To compensate for the TID damage, we introduced an independent electrode underneath the BOX layer; the middle silicon layer (SOI2 layer). Such a double SOI wafer is fabricated by repeating the SOITEC SmartCut^{TM} procedure twice. A cross-sectional image of the first double SOI wafer and device is shown in Fig. 2. The middle silicon layer (p-type with 10 Ω cm resistivity) has a sheet resistance of 170 kΩ/sq with $CoSi_2$ silicide at the contact. By applying a negative voltage (V_{SOI2}) to the SOI2 layer, the effects due to radiation-induced holes trapped in oxide layers are cancelled [11–13]. The SOI2 layer should also suppress the back-gate effect and cross-talk between the circuitry (e.g. clock signals) and pixel nodes through the thin BOX layer [3].

1.3. INTPIXh2

INTPIXh2 is the first double SOI integration type SOI pixel sensor; it has pixels in 280 rows and 240 columns, where each pixel is 18 μm square in size. The overall chip size is 6 mm square, including peripheral circuitry such as for the address decoder and IO ports. We adopted the Cz n-type substrate with a resistivity of approximately 0.7 kΩ cm. The on-pixel circuitry is illustrated in Fig. 3, and the actual layout is shown in Fig. 4. The analog signal stored in the storage capacitor is switched out in series to the column line and digitized with an external 12-bit analog-to-digital converter (ADC).

Some of the characteristics of the double and single SOI types are compared. In the double type, the potential of the middle silicon layer underneath the pixels and the peripheral circuitry is controlled by a common V_{SOI2} voltage. TID damage was induced by ^{60}Co γ at a dose of 100 kGy. The sensors were irradiated at room temperature at a rate of 5 kGy/h with all of the terminals grounded during irradiation. Such a configuration does not represent realistic operation conditions. The effects of biasing during irradiation are under investigation using simplified FET TEGs (test element group) for a systematic and comprehensive understanding. Evaluation with a pixel device is to follow.

2. Leakage current

The leakage current was measured at room temperature as a function of the bias voltage. Fig. 5 shows example *I–V* curves for a 100 kGy irradiated sample in comparison with its curve at pre-irradiation. The V_{SOI2} voltage was varied in the post-irradiation measurements. The breakdown voltage of 12 samples was in a

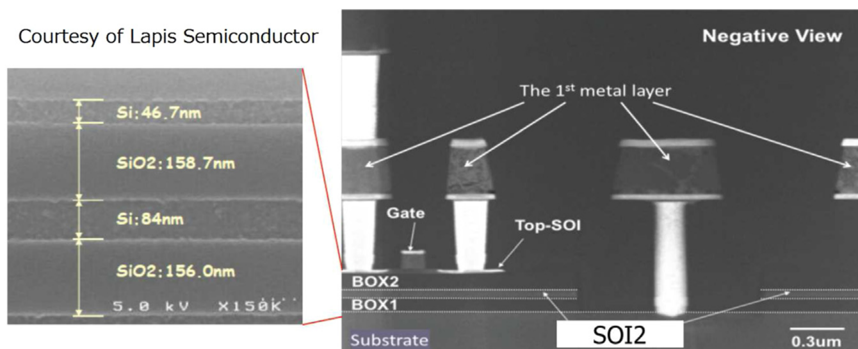

Fig. 2. Transmission electron micrography (TEM) images of the double SOI wafer and device (courtesy of Lapis Semiconductor).

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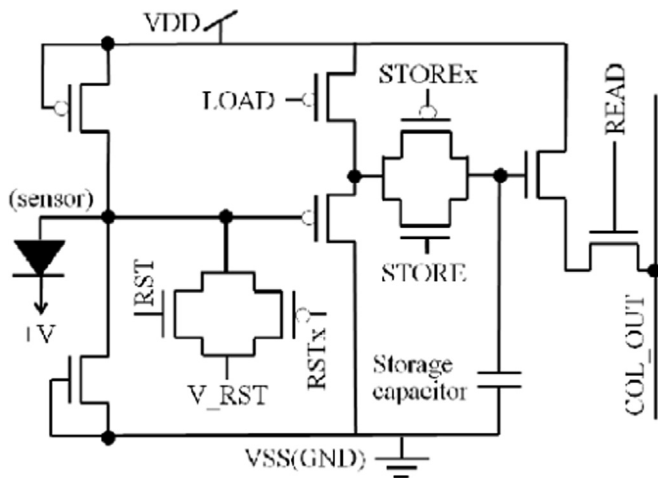

Fig. 3. On-pixel circuit of INTPIXh2 [11].

range from 300 to 400 V at pre-irradiation. The breakdown of the sample shown in the figure dropped to nearly 120 V after 100 kGy irradiation at V_{SOI2} −0 V (another 100 kGy irradiated sample showed 170 V breakdown), but recovers to 200 V by applying V_{SOI2} as small as −1 V; applying exceeding V_{SOI2} = −11 V degrades again the breakdown voltage. The degradation observed at V_{SOI2} = 0 V is dependent on the radiation dose, while the 200 V breakdown at non-zero V_{SOI2} stayed similar for the doses from 10 kGy to 100 kGy.

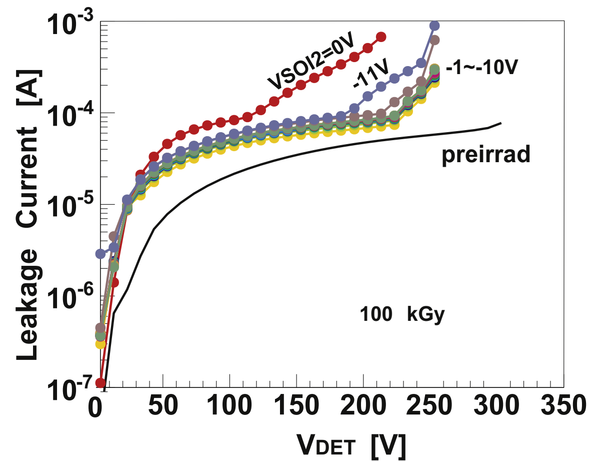

Fig. 5. Leakage current of the sensor irradiated to 100 kGy measured at different V_{SOI2} setting. The curves are compared with pre-irradiation curve. Measurements are at 20 °C.

The leakage current is a sum of contributions from the pixels and peripheral circuitry. The contribution from the pixels evaluated as the pedestal shift does not change by irradiation, suggesting that the leakage increase is dominantly caused in the peripheral.

As we discuss in Section 6, 200 V is not enough to fully deplete the device of 300 μm thickness. While we continue investigating the cause of the breakdown, 200 V is appropriate for the device thinned to 100 μm in an actual application.

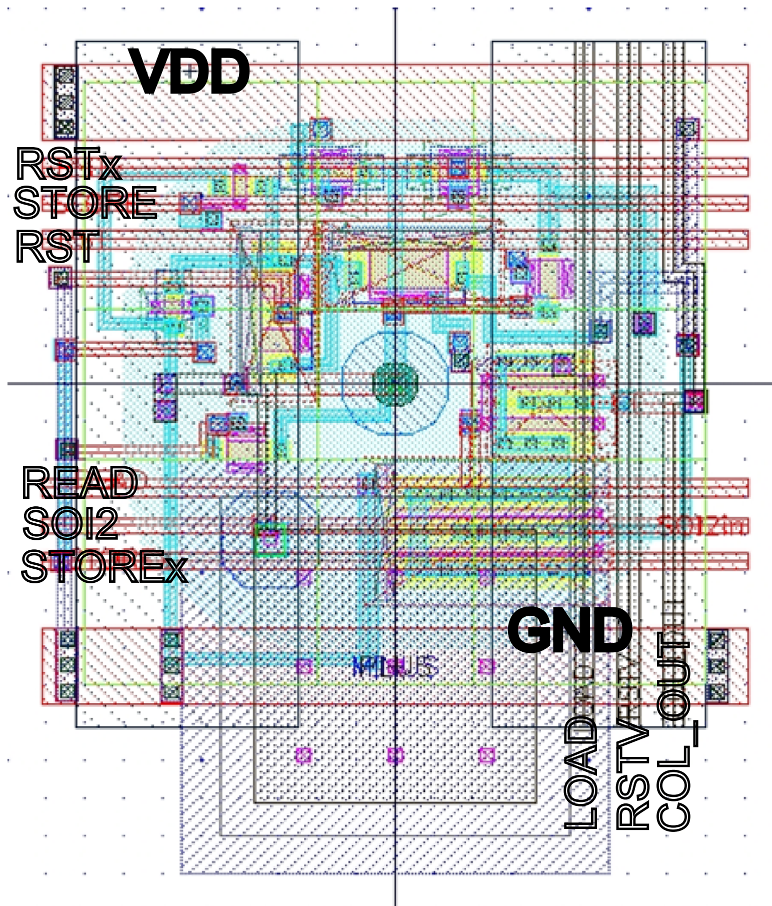

Fig. 4. Layout of the INTPIXh2 pixel components.

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3. Response to IR laser after 100 kGy irradiation

The response of a sensor of 300 μm thickness irradiated with 100 kGy was investigated by using an infrared (1024 nm wavelength) pulse laser. The response at a reverse voltage of 100 V was clearly confirmed at $V_{SOI2} = -10$ V while no response was observed at $V_{SOI2} = 0$ V (see Fig. 6). This demonstrates the effectiveness of the compensation using the double SOI feature.

We studied the functionality of the circuit by measuring the output linearity w.r.t. the reset voltage amplitude V_{RST} (see Fig. 4). Fig. 7 plots the results for the 100 kGy irradiated sensor (100 μm thick, 100 V applied reverse voltage). The vertical is in ADC unit obtained when the output voltage is integrated over 1 μs. The figure shows the recovery of the response through the application of the negative voltage V_{SOI2}. There was no response seen at $V_{SOI2} = 0$ V. The response curve of a non-irradiated sensor is also plotted for comparison. Radiation-induced shifts in operating conditions, mainly thresholds, of the FETs were not been completely recovered from. This is because the optimum V_{SOI2} to recover the threshold voltage depends on the FET type (n or p, body-tied or body-floating [12]) and complete compensation is not possible in this sensor design with a single common control. However, a responsive region was clearly recovered by V_{SOI2} with a slightly reduced dynamic range. Lowering V_{SOI2} further was not possible because no output was observed. A study with other devices suggested that this is caused by the threshold shifts of electrostatic discharge (ESD) diodes connected at the outputs which loose functionality at increased $|V_{SOI2}|$.

4. Signal time response

The signal time structure was evaluated by using the pulsed IR laser. The signal shape was measured by using a fast multi-pixel photon counter (MPPC) for a base width of 50 ns and including a jitter spread of 5 ns, as shown in Fig. 8. We measured the output charge from INTPIXh2 with a fixed integration time of 10 ns. By varying the delay time of integration start w.r.t. the IR laser trigger, we derived the signal time response of INTPIXh2. As shown in Fig. 9, the measured signal width was about 150 ns with a fast peaking time of 40 ns for the non-irradiated device. After 100 kGy, the time response slightly degraded to a 50 ns peaking time.

5. Cross talk

The cross-talk characteristics were measured by injecting collimated IR laser to one pixel and measuring the signals out of the

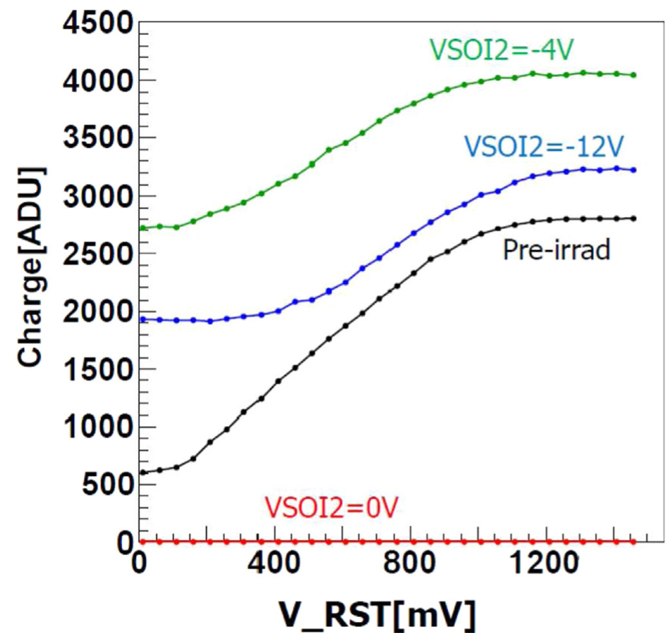

Fig. 7. Response to V_{RST} before and after 100 kGy irradiation with V_{SOI2} of 0 V, −4 V, and −12 V [12].

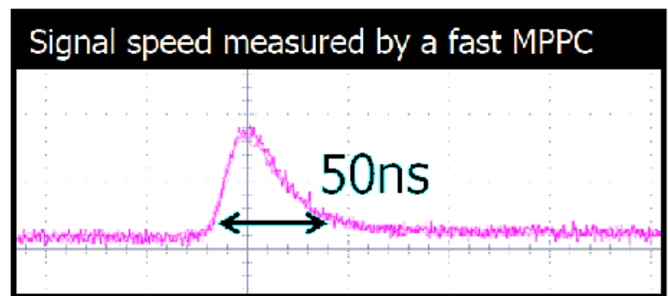

Fig. 8. Signal shape of IR-laser pulse measured with MPPC.

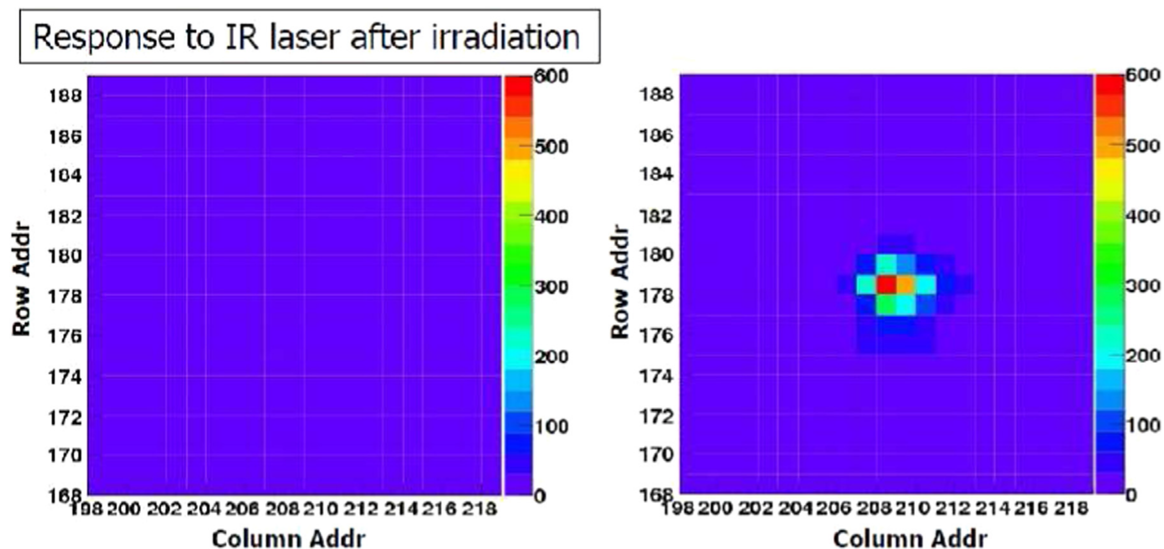

Fig. 6. Response to IR laser of a 100 kGy irradiated INTPIXh2: (left) $V_{SOI2} = 0.0$ V, (right) $V_{SOI2} = -10.0$ V [12].

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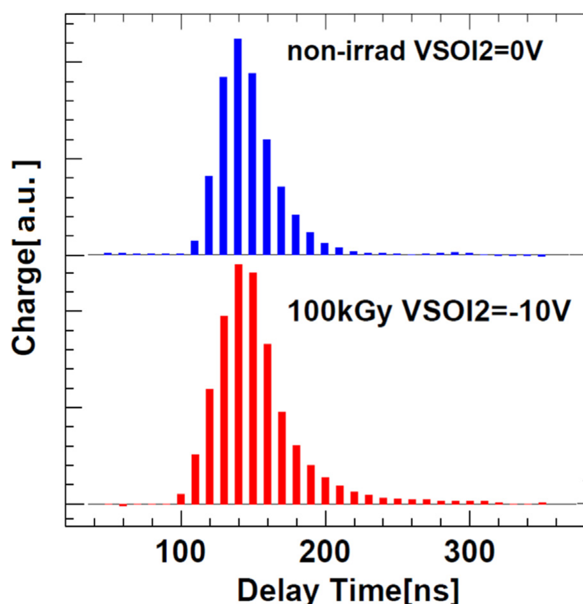

Fig. 9. Signal shape of (top) non-irradiated and (bottom) 100-kGy irradiated INTPIXh2.

surrounding pixels. A no metal region (window) was assured at the pixel center (see Fig. 4) to allow for light injection from the top. The laser spot size was adjusted to 4 μm square so that the laser was only injected to one pixel. We defined the cross talk as the ratio of the output signal from the pixel being evaluated to that from the pixel where the laser was injected. Fig. 10 shows the results for the 100 μm thick sensor before and after irradiation to 100 kGy for a signal integration time of 1 μs. The substantial cross talk at a low reverse bias voltage is suppressed with increasing the bias voltage before irradiation, as the inter-pixel region is fully depleted with the bias (see Fig. 11). The cross talk is small after irradiation at the same bias voltage. The potential of V_{SOI2} was set at -10 V in this measurement since a negative potential is required for observing the signal, see Section 3. The suppression of the cross talk by irradiation is explained because the electrical isolation between pixels is improved by irradiation through the accumulation of electrons between p-type pixel nodes for an n-type substrate. Those electrons attracted at the boundary prevent from creation of inversion layer which worsens the cross talk. The negative V_{SOI2} tends to remove the accumulated electrons and create an inversion layer but the applied potential is not sufficient to deteriorate the cross talk. In summary, the cross talk was determined to not be degraded by irradiation. Note that the middle silicon layer acts as an electrical shield [14] through the coupling to the sensor node, which reduces the amount of charge read out by the amplifier, as we discuss in Section 6.

6. Response to minimum-ionizing particles

The response to penetrating ^{90}Sr β-rays for a double SOI INTPIXh2 was measured with a single SOI INTPIXh2 for comparison. The available single-type INTPIXh2 was 500 μm thick with an n-type substrate and >2 kΩ cm resistivity, while the double was 300 μm thick with an n-type substrate and 0.7 kΩ cm resistivity. The β-ray source enclosed in a collimator was placed on top, and the penetrating β was triggered by a plastic scintillator. The data acquisition timing chart and the setup illustration are shown in Fig. 12. The signal integration time was set to 1 μs. The β-ray signal was reconstructed in a 7×7 pixel cluster about the seed pixel with the maximum response to an event. The reconstructed charge distribution is shown in Fig. 13 for the single SOI sensor which was biased at 250 V. At 200 V and above, the reconstructed charge peak is saturated and the sensor is fully depleted at 250 V. Fig. 14 shows the charge distribution for the double SOI sensor biased at 200 V. The depletion depth is calculated to 210 μm for the wafer resistivity. The measurement conditions and other parameters are summarized in Table 1. The sensor gain (μV/e$^-$) was obtained by observing the X-ray peaks of radioactive sources. The sensor gain of the double SOI was roughly one half of that of the single SOI. This is explained by the coupling between the BPW and SOI2 layer in the double SOI sensor. The coupling increased the detector capacitance and picked up a fraction of the signal by the SOI2 layer. The peak value of the single sensor 781 ADU (Fig. 13) was determined by a fit of a Landau and Gaussian convolution function. The value is consistent with the calculation using the sensor thickness of 500 μm and the parameters as listed in the table. The double-type sensor showed a mip peak at 158 ADU (Fig. 14). For a 210 μm depletion thickness, the value is slightly off but within the expectation if

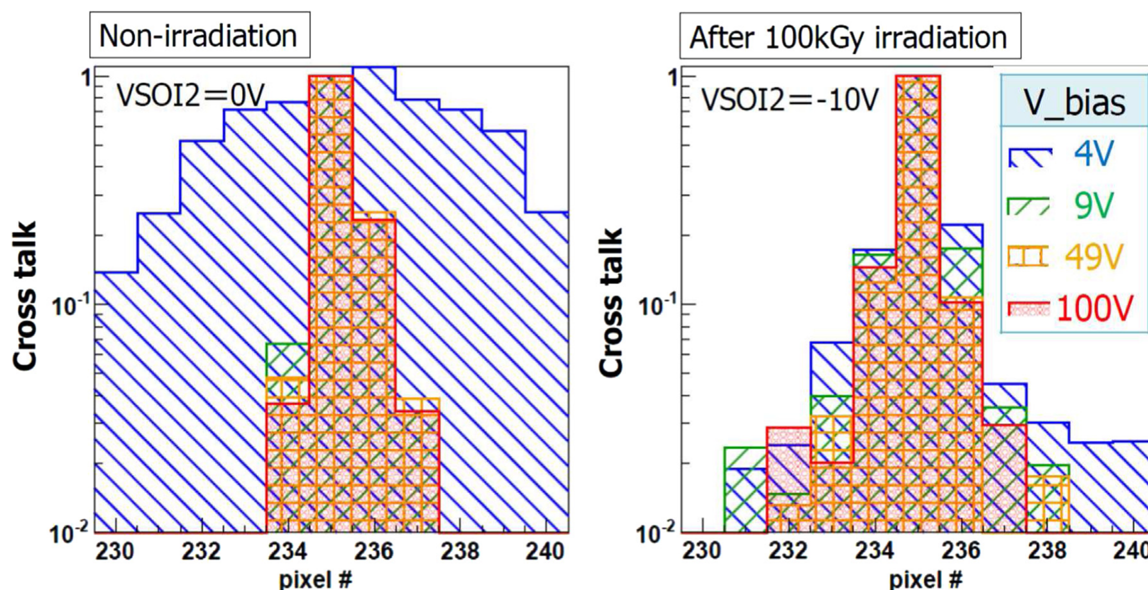

Fig. 10. Cross talk of INTPIXh2 before and after 100 kGy irradiation. The collimated laser was spotted at pixel-235, and relative pulse heights in neighboring pixels were plotted for typical bias voltages.

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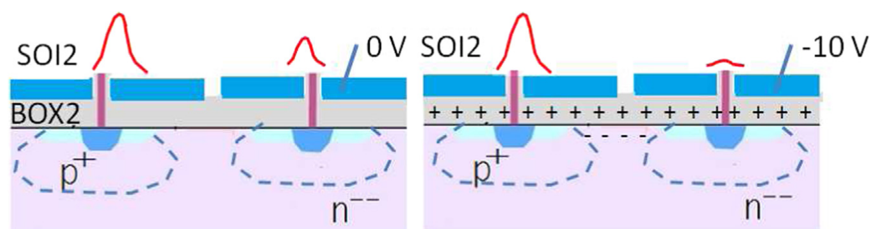

Fig. 11. Illustration of cross talk (left) before and (right) after irradiation. The V_{SOI2} voltage was 0 V before and −10 V after. The broken curve represents the depleted region at a low bias voltage.

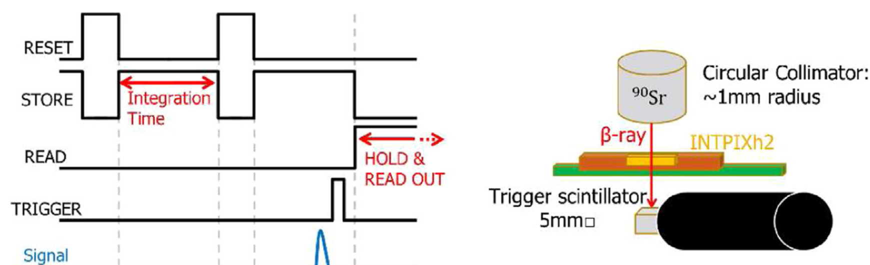

Fig. 12. (left) Data acquisition timing chart doe the mip measurement. On receiving a trigger, the following reset is disabled, and the readout sequence is activated. (right) Geometric illustration of the setup.

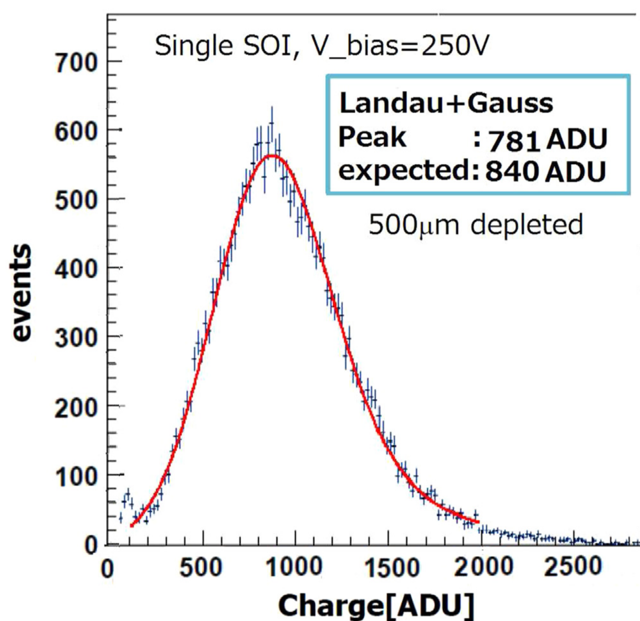

Fig. 13. Cluster charge distribution obtained in single INTPIXh2.

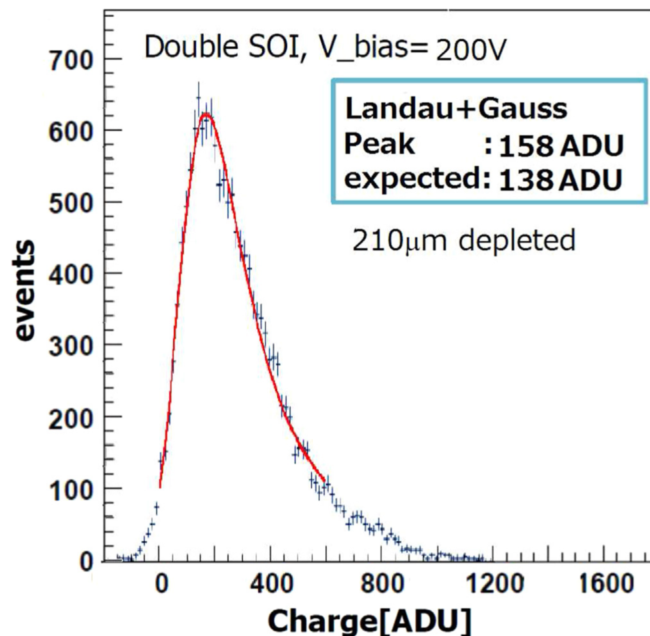

Fig. 14. Cluster charge distribution obtained with double SOI INTPIXh2.

we take into account of the uncertainty in the substrate resistivity and in other parameters.

7. Discussions and summary

We introduced a double SOI structure to compensate for the TID damage and characterized the performance of the integration-type pixel sensor INTPIXh2. The results obtained for the non-irradiated and 100 kGy irradiated sensors showed that the response of the irradiated sensor can be recovered by applying a negative voltage to the SOI2 layer. The double SOI structure enhanced the radiation resistivity up to 100 kGy. Therefore the double SOI sensor is already sufficiently radiation hard for use in high-energy experiments in hard radiation environment such as at Belle II or ILC.

Table 1
Parameters used in β-ray measurement. The depletion thickness of the double sensor is a calculated value for the substrate resistivity and applied bias voltage. The ADC conversion factors are the slope measured in the reset response (see Fig. 7).

Item	Single SOI	Double SOI
Physical thickness (μm)	500	300
Sub. resistivity (kΩ cm)	>2	0.7
Bias (V)	250	200
Depletion thickness (μm)	500	210
Gain (μV/e$^-$)	6.0	2.4
ADC conversion (ADC/mV)	3.5	3.4
Expected ADC/mip (ADU)	840	138

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Above this dose, however, the sensor became inoperative. The main reason is suspected to be the different radiation-induced threshold shifts among various types of FETs and the degradation of the transconductance, especially in PMOS FETs [12]. A recent study [15] succeeded in improving the radiation tolerance of PMOS FETs by adjusting the lightly doped drain (LDD) profile. Also individual V_{SOI2} adjustments in pixel, decoder and IO regions provide a wider operational range [16]. The radiation tolerance of such devices is currently being evaluated.

8. Acknowledgments

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