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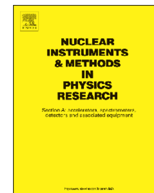

Development of n^+-in-p planar pixel sensors for extremely high radiation environments, designed to retain high efficiency after irradiation

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ABSTRACT

We have developed n^+-in-p pixel sensors to obtain highly radiation tolerant sensors for extremely high radiation environments such as those found at the high-luminosity LHC. We have designed novel pixel structures to eliminate the sources of efficiency loss under the bias rails after irradiation by removing the bias rail out of the boundary region and routing the bias resistors inside the area of the pixel electrodes. After irradiation by protons with the fluence of approximately $3 \times 10^{15}\ n_{eq}/cm^2$, the pixel structure with the polysilicon bias resistor and the bias rails removed far away from the boundary shows an efficiency loss of <0.5% per pixel at the boundary region, which is as efficient as the pixel structure without a biasing structure. The pixel structure with the bias rails at the boundary and the widened p-stop's underneath the bias rail also exhibits an improved loss of approximately 1% per pixel at the boundary region. We have elucidated the physical mechanisms behind the efficiency loss under the bias rail with TCAD simulations. The efficiency loss is due to the interplay of the bias rail acting as a charge collecting electrode with the region of low electric field in the silicon near the surface at the boundary. The region acts as a "shield" for the electrode. After irradiation, the strong applied electric field nearly eliminates the region. The TCAD simulations have shown that wide p-stop and large $Si–SiO_2$ interface charge (inversion layer, specifically) act to shield the weighting potential. The pixel sensor of the old design irradiated by γ-rays at 2.4 MGy is confirmed to exhibit only a slight efficiency loss at the boundary.

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1. Introduction

We have developed radiation-tolerant, planar-process, position-sensitive, silicon sensors in p-type 6-inch silicon wafers for applications in extremely high radiation environments [1–3] where radiation damage is generated by charged and neutral particles passing through the silicon sensors. Since the silicon bulk stays as p-type after irradiation, the p-type sensor requires lithographic processing only in the p–n junction side, simplifying the fabrication and leading to low device cost. Reading the signals out from the n-side enables the operation of the sensor without completely depleting the bulk and makes the sensor highly radiation tolerant. The planar silicon fabrication process is well established in the industry and is a cost-effective solution for large volume device production.

Extremely high radiation environments are found in the large hadron collider (LHC) [4]. The LHC accelerator complex is planned to be upgraded to High Luminosity LHC (HL-LHC) [5] to reach a

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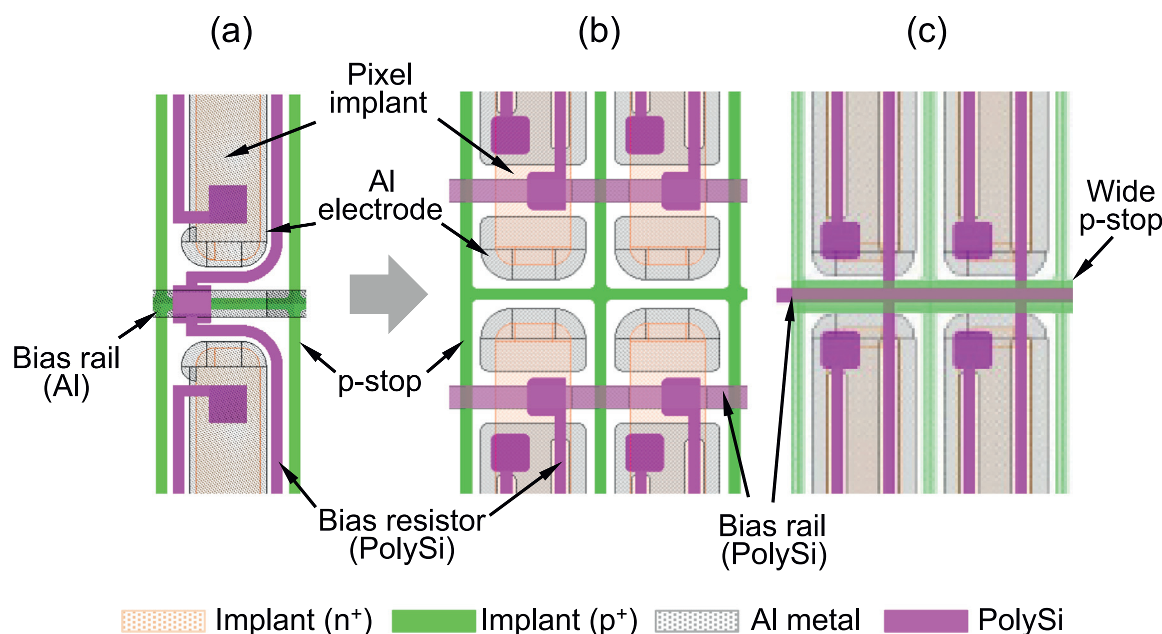

Fig. 1. Pixel structures: (a) old structure in wafer layout #2, (b) Type 10 and (c) Type 13 in wafer layout #4 .

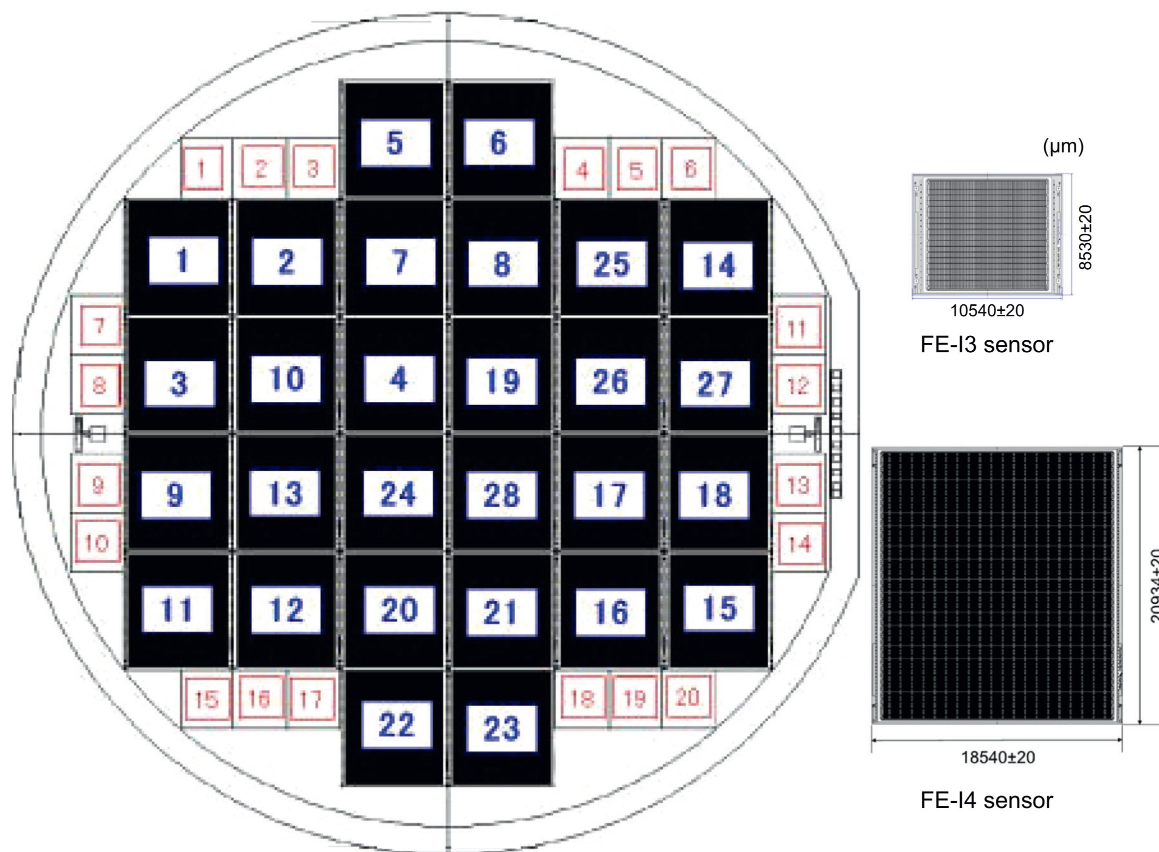

Fig. 2. Wafer layout #4 in 6-inch wafer, with 28 of ATLAS FE-I4 singles and 20 of FE-I3 singles of pixel sensors. Each FE-I4 and FE-I3 pixel sensor is 18.54×20.93 and 10.54×8.53 mm^2 in chip size, with a 336×80 and 160×18 matrix of 50×250 and 50×400 μm^2 pixels, respectively, with unique pixel structure per sensor.

higher collision rate (5×10^{34} cm^{-2}s^{-1} with "luminosity leveling") and consequently obtain an increase of one order in magnitude in the number of accumulated events (3000 fb^{-1}). The upgrade is scheduled during the LHC shutdown during the years 2024–2026. Our study primarily aims to develop a planar pixel sensor for the ATLAS detector, which is a general-purpose detector at a collision point in the LHC ring [6], that will be upgraded for the HL-LHC [7]. Considering a safety factor of 2, the sensor must cope with a radiation specified: the accumulated flow of particles ("fluence") of approximately 2×10^{16} 1 MeV-neutrons equivalent (n_{eq})/cm^2 and 3×10^{15} n_{eq}/cm^2 at a radius of 4 cm for the inner pixel layers and at 15 cm for the outer pixel layers, respectively [8].

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Table 1
Specifications of wafer layout #4 of n$^+$-in-p pixel sensors.

Silicon wafer diameter	6 inch (150 mm)
Wafer type	p-type, float zone (FZ)
Crystal orientation	⟨100⟩
Resistivity	3–7 kΩ cm
Thickness	320 μm
Thinned	150 μm
Number FE-I4 sensors	28
Number FE-I3 sensors	20

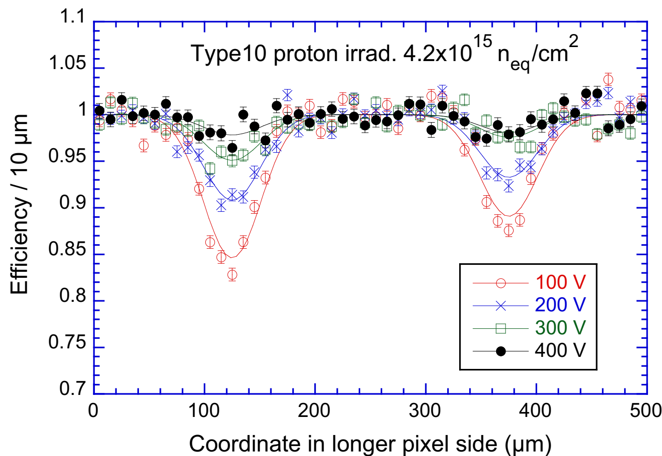

Fig. 3. Efficiency mapping over two pixel regions projected on the long pixel side. Pixel boundaries of the bias rail side and the no bias rail side are at 125 and 375 μm, respectively.

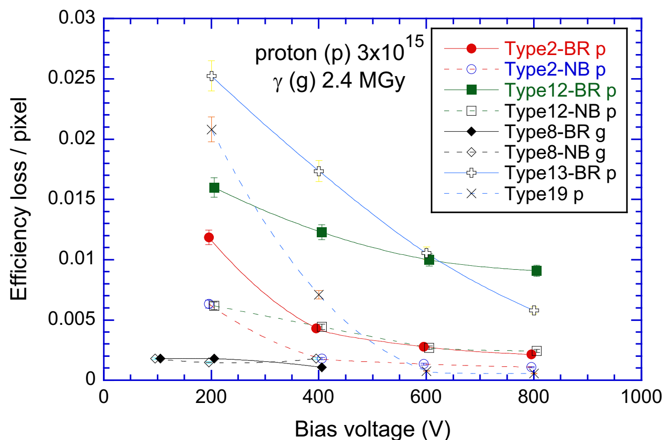

Fig. 4. Efficiency loss per pixel as a function of bias voltage in the bias rail (BR, filled) and the no bias bail (NB, open) regions, of Types 2 (Large offset, circle) and 12 (Small offset, square) pixel structures after proton irradiation of 3×10^{15} n$_{eq}$/cm^2, Type 8 (Old, diamond) after γ irradiation of 2.4 MGy. Those data of Types 13 (Wide p-stop, vertical cross) and 19 (No bias, cross) after proton irradiation [16] are reproduced together.

2. KEK/HPK n$^+$-in-p pixel sensors

2.1. Pixel structure – "Old" design (wafer layout #2)

We have previously produced n$^+$-in-p pixel sensors[1] in 6-inch wafers (hereafter referred to as "wafer layout #2") [2]. The sensors were bump bonded to the ATLAS pixel readout ASIC, FE-I4 [9], irradiated at a fluence of 2×10^{15} n$_{eq}$/cm^2 with 23 MeV protons at

[1] The superscript, +, indicates that the density of the material is higher than that of the silicon bulk.

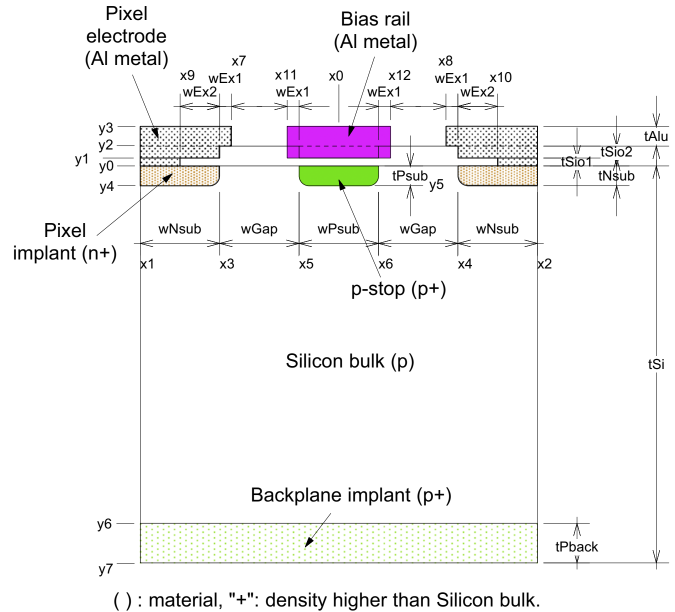

Fig. 5. TCAD 2D geometry of the pixel boundary region with the bias rail.

Table 2
Parameters before and after irradiation in TCAD simulations.

Parameter	Non-irrad.	Irrad.
Fluence (n$_{eq}$/cm^2)	0	3×10^{15}
Effective space charge concentration (p-type), N_{eff} (cm^{-3})	2.6×10^{12}	2.5×10^{13}
Full depletion voltage, V_{dep} (V)	44	430
Applied bias voltage, V_{op} (V)	100	430
Leakage current, I_{leak} (a.u.)	1	~10^3
Surface density of interface charge, Q_f (cm^{-2})	1×10^{10}	1×10^{12}

(a.u: arbitrary unit)

Table 3
Geometry parameters used in TCAD simulations.

Parameter	Value
Silicon thickness (*tSi*)	150 μm
Bulk type	p-type
Pixel: implant type	n-type
Dopant concentration	1×10^{19} cm^{-3}
Implant width, depth (*wNsub*, *tNsub*)	50, 1 μm
Metal electrode	Al, DC-coupled
Overhang (*wEx*1)	2 μm
p-stop: implant type	p-type
Dopant concentration	1×10^{16} cm^{-3}
Implant width (*wPsub*), narrow/wide	4 / 8 μm
Implant depth (*tPsub*=*tNsub*)	1 μm
Gap to Pixel implant (*wGap*), wide/narrow	9.5/6.5 μm
Bias rail: metal, thickness	Al, 1.8 μm
Overhang, wide/narrow (*wEx*1, −2 × *wEx*1)	2/−4 μm
Insulator thickness (*tSio*1)	0.2 μm
Backplane implant, thickness (*tPback*)	p-type, 3 μm
Dopant concentration	1×10^{18} cm^{-3}

KIT [10], and tested by beam tests before and after the irradiation [11]. Several issues were identified on the basis of the results of these experiments.

The pixel structure of interest in the wafer layout #2 is shown in Fig. 1(a) (hereafter referred to as "Old" structure). Although the individual pixels are to be DC coupled to the readout ASIC, we have designed a connection of bias potential to the individual pixels to

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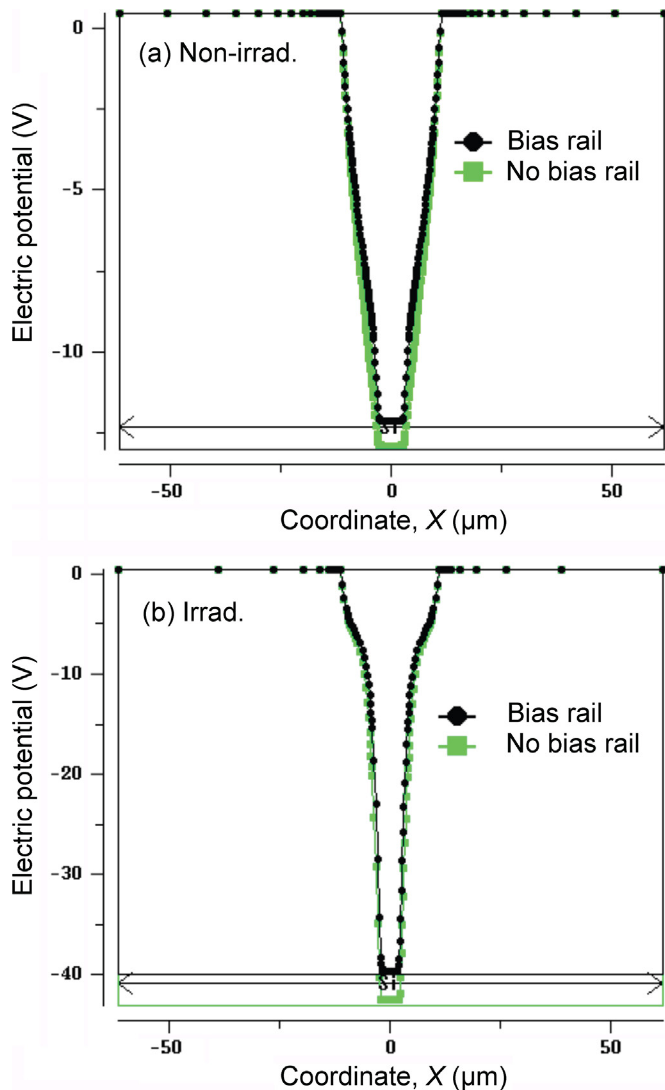

Fig. 6. Electric potential near the surface under the bias rail, with bias rail (black circle) and without bias rail (light-color square): (a) before irradiation (Non-irrad.) and (b) after irradiation (Irrad.).

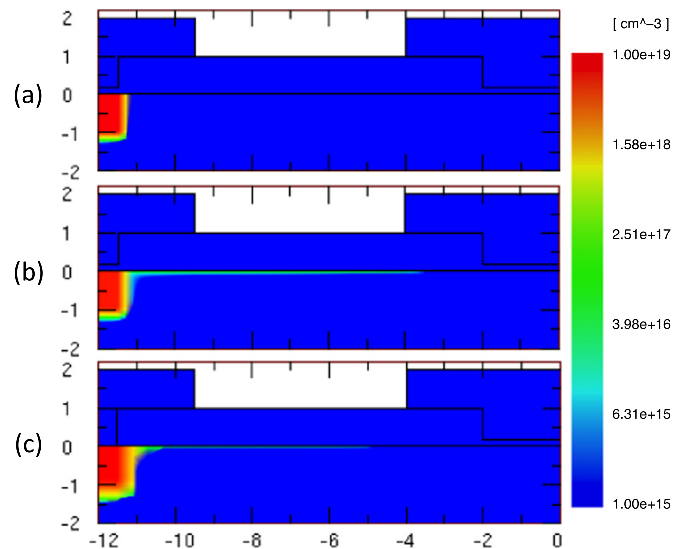

Fig. 7. Electron density in the surface of silicon simulated with TCAD: (a) before irradiation, $Q_f = 1 \times 10^{10}$ cm^{-2}, bias voltage −100 V, (b) the same as (a) but $Q_f = 1 \times 10^{12}$ cm^{-2}, and (c) after irradiation, $Q_f = 1 \times 10^{12}$cm^{-2}, bias voltage −430 V. The color scale is in the unit of volume density (cm^{-3}). (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

test the sensor without bump bonding to the ASIC. We use a bias resistor made of polysilicon material to connect the individual pixels to a bias rail common to a row of pixel pairs. The bias rail was made of polysilicon in the design. Addition of a biasing network is a complication in the pixel structure but the quality control of the sensors would save time and cost at later assembly stages.

In the old design, the bias rail runs in the middle of the boundary of a pair of pixels, which is shown horizontally in the figure, and the bias resistors are routed to the pixel implants by encircling outside the pixels. The bias rail runs over the narrow trace of p^+ implant in the surface of silicon, called “p-stop”. The p-stop is required to separate the n^+ pixel implants. The bias rail and the p-stop are separated spatially and electrically by the SiO_2 surface passivation. The width of the p-stop was chosen to be narrow according to the analysis of the designs [12]. The width of the bias rail is wider than that of the p-stop to reduce the electric field at the edge of the p-stop.

Efficiency loss was observed for this layout. The loss of efficiency was most pronounced under the bias rails, and was smaller but still noticeable under the bias resistors, compared to the loss at the pixel boundaries in the opposite side where no bias rail exists. In the absence of irradiation, the loss was negligible.

2.2. Optimization of pixel structures – novel design (wafer layout #4)

We have then designed novel pixel structures to optimize the pixel structures to mitigate the problems found for sensors with wafer layout #2. The structures of special interest are shown in Fig. 1, (b) Type 10 and (c) Type 13 in wafer layout #4. The physical mechanisms behind the efficiency loss, especially the difference between before and after irradiation, have been investigated and are presented in Section 4. Phenomenologically, we hypothesized that removal of the bias rails out of the boundary region and the placement of the bias rails and bias resistor traces in the area of and over the pixel implantation to shield them from the silicon underneath will mitigate the efficiency loss. In Type10 (hereafter referred to as “Large offset”), the common bias rail for a pair of rows of pixels is split into individual bias rails per a row of pixels, the bias rails are removed far away from the boundary, and the bias rails and the bias resistors are routed in the area of and over the pixel implantation. In Type13 (hereafter referred to as “Wide p-stop”), the common bias rails are kept at the boundaries, but their width is smaller and the width of the p-stop is wider, which is based on the hypothesis that the p-stop may function as a shield for the bias rail.

The novel pixel structures are laid out in wafer layout #4 as shown in Fig. 2 in two types of sensors: FE-I4 (18.54 × 20.93 mm^2) with a matrix of 336 × 80 of 50 × 250 μm^2 pixels [9] and FE-I3 (10.54 × 8.53 mm^2) with 160 × 18 of 50 × 400 μm^2 pixels [13]. The detailed description of the novel pixel designs is given in Appendix A along with relevant tables and figures. No additional cost is associated with the novel pixel structures in fabrication as the PolySi process has already been included.

Typical parameters of the wafer layout #4 are summarized in Table 1. The thickness of the raw wafers is 320 μm. After the fabrication of the front side, the thin sensors are fabricated by thinning the rear of the wafer to a thickness of 150 μm, followed by an additional process for the rear.

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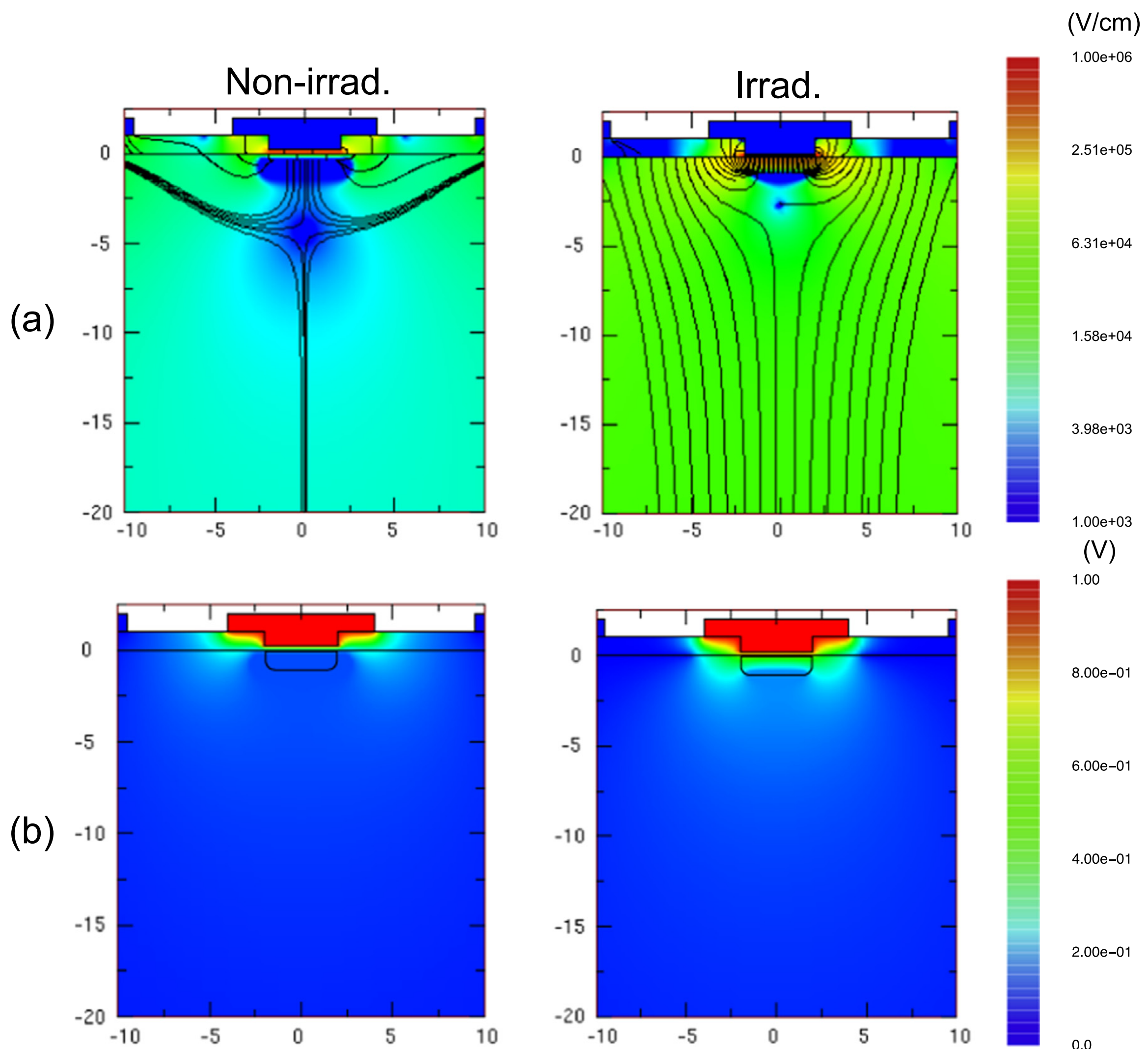

Fig. 8. 2D maps of the fields in the vicinity of bias rail, before and after irradiation in the left and right column, and in the rows of (a) electric field E overlaid with flow lines and (b) weighting potential of the bias rail V_{qA}, respectively.

3. Results with test beams

Pixel sensors with the novel pixel structures were irradiated at a fluence of 3 to 5×10^{15} n_{eq}/cm^2 with 70 MeV protons at CYRIC [14]. The samples were irradiated in an irradiation box attached to an X–Y stage to scan the beam uniformly over the samples. The samples were cooled to $-15\,°C$ during the irradiation with the cold nitrogen gas from a liquid nitrogen dewar, and after irradiation stored cold in a freezer. A pixel sensor of the old design was irradiated with γ rays at a dose of 2.4 MGy at TARRI [15]. These irradiated samples were then tested using test beams at DESY with 4 GeV electrons and/or CERN with 120 GeV π's [16,17]. Based on the energy of the beam particles, together with the distance between the telescope planes and the device under test (DUT), the pointing resolution of the beam particles at the DUT plane was approximately 30 and 8 μm at DESY and CERN, respectively.

3.1. Efficiency mapping over pixel boundaries

An example of the improvement of the novel pixel structure is illustrated in Fig. 3, using an efficiency mapping over two pixel regions projected on the long pixel side. The DUT is KEK46 and 150 μm thick with the Type 10 pixel structure, irradiated at 4.18×10^{15} n_{eq}/cm^2 and tested at DESY. The boundary of the bias rail side (Bias rail (hereafter referred to as BR)) is at 125 μm and the opposite side (No bias rail (hereafter referred to as NB)) is at 375 μm. The curves are fit to the data for guidance. The width of the efficiency loss is dominated by the pointing resolution. The efficiency losses in the BR and NB boundaries are nearly symmetric; the effect of the bias rail is nearly eliminated. In the plot, the efficiencies of the central region of the pixels are normalized to unity since the absolute efficiency was not reliable due to a technical issue in this test beam.

3.2. Efficiency loss per pixel – comparison of pixel structures

The efficiency loss at the boundary can be quantified as an “efficiency loss per pixel” by fitting a Gaussian function to the efficiency mapping over the pixel boundaries and dividing the integrated “area” of the Gaussian by the length of two pixels. The calculation of “area” eliminates the difference in the pointing resolutions at DESY and CERN. A compilation of the efficiency loss per pixel at the boundaries is shown in Fig. 4 for the DUT's of KEK84ch1 (150 μm, Type 2, p 3.03×10^{15}), KEK71ch3 (150 μm, Type 12, p 3.08×10^{15}), KEK93 (320 μm, Type 8, γ 2.4 MGy), using the CERN data and KEK49ch3 (150 μm, Type 13, p 3.20×10^{15}) and KEK53ch3 (150 μm, Type 19, p 2.35×10^{15}) using the DESY data. The letters “p” and “g” in the legend

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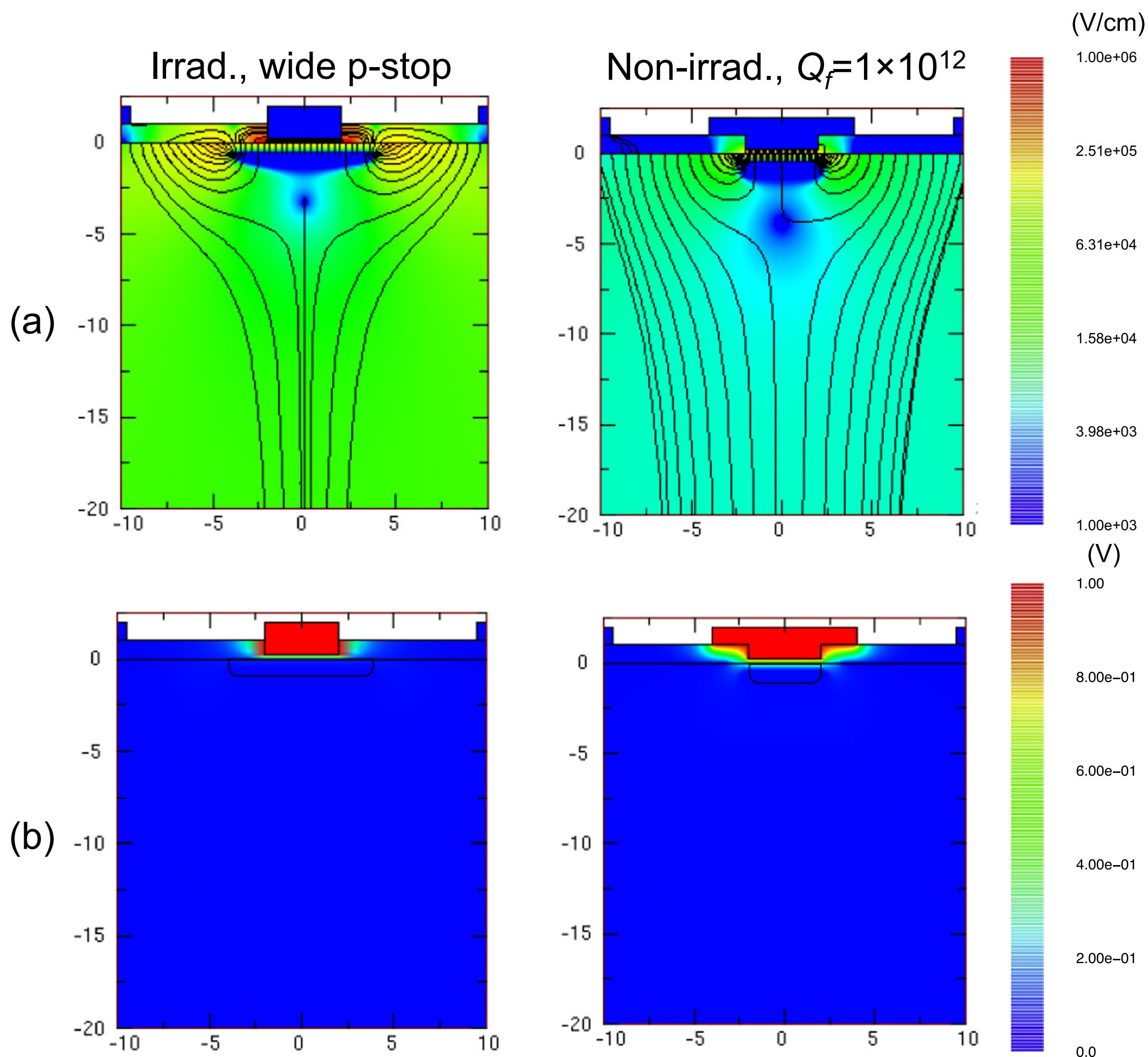

Fig. 9. 2D maps of the fields in the vicinity of bias rail of the wide p-stop geometry after irradiation and the narrow p-stop geometry before irradiation with the interface charge as that after irradiation in the left and right column, and in the rows of (a) electric field E overlaid with flow lines and (b) weighting potential of the bias rail V_{qA}, respectively.

indicate the proton and the γ irradiation, respectively. The efficiency losses at the boundary of the bias rail side or the no bias rail side are indicated with the BR (with solid line) or NB (with dashed line), respectively. The pixel structure of Type 2 is an equivalent of Type 10 but the bias rail is made from an aluminum material. Type 12 is a variation of Type 10 with the bias rails set at the edges of the pixels (hereafter referred to as "Small offset"). Type 8 is an equivalent of the old structure. Type 19 is the reference with no bias structure and represents the best case. The details of the pixel structures are presented in Appendix A.

There is a noticeable difference in bias voltage dependence between the DUT's of the CERN (Types 2 and 12) and DESY data (Types 13 and 19). The difference has been traced to the difference in the bias voltage dependence of the pulse height distribution, most likely due to different tunings of the readout ASICs at different bias voltages. This difference can be removed by normalizing the NB data points by each other because the NB side is basically the same as the no bias structure.

On the basis of Fig. 4, we have evaluated the pixel structure of the bias rail side (BR), finding that

(1) Type 2 (Large offset) is as good as NB (No bias) side, the loss is <0.5% per pixel at the bias voltage >400 V,
(2) Type 12 (Small offset) and Type 13 (Wide p-stop) are similarly good, the loss is approximately 1% at >600 V,
(3) These pixel structures exhibit greatly improved efficiency loss, compared with the ≥3% loss of the "old" design [16], and
(4) γ irradiation has no effect on the efficiency loss under the bias rail.

The result (4) especially indicates that the efficiency loss under the bias rail is not caused by the surface charge in the Si–SiO_2 interface but caused by the radiation damage in the silicon bulk.

4. Understanding the underlying physics

We have used a semiconductor technology CAD (TCAD) program, ENEXSS [18], to calculate the electric fields in detail, including the effect of trapped charges in the interface. The region of the pixel boundary with the bias rail is modeled and implemented as a 2D geometry in the TCAD simulations as shown in Fig. 5. We have approximated the conditions before and after irradiation with three parameters according to the method elaborated in Ref. [19]: effective space charge concentration (N_{eff}) and leakage current (I_{leak}) in the silicon bulk, and fixed interface charge (Q_f) at the

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Table 4
Variation of pixel structure of FE-I4 sensors in wafer layout #4.

Type no.	Pixel size (μm^2)	Bump pad	Bias type	PolySi routing	Bias rail	Bias rail offset	p-stop width	Bias rail material	Comment
(1)	50×250	End	PolySi	Inside	1	Large	Narrow	Al	
(2)					2				
(3)					1	Small			
(4)					2				
(5)					1	None	Wide		
(6)				Inside[a]					
(7)				Outside					
(8)							Narrow		Old default
9				Inside	1	Large	Narrow	PolySi	
10					2				New default
11					1	Small			
12					2				
13					1	None	Wide		
14							Narrow		
(15)			PT	–	Straight			Al	
(16)							Wide		
(17)					Zigzag	Small	Narrow		
(18)						Large			
19			None		–	–		–	
(20)	25×500	End	PT	–	Straight	None	Wide	Al	
(21)			PolySi	Inside[b]	1				
22					2	Large	Narrow	PolySi	
(23)		Center	PT	–	Zigzag			Al	
(24)			PolySi	Inside[b]	2	Small			
(25)						Large			
26								PolySi	
27		Staggered			1				
28		End	None	–	–	–		–	

[a] No opening in the DC-Al metal of the pixel implant under the PolySi trace.
[b] PolySi is routed along one side of the perimeter of pixel implant.

Table 5
Variation of pixel structure of FE-I3 sensors in wafer layout #4.

Type no.	Pixel size (μm^2)	Bump pad	Bias type	PolySi routing	Bias rail	Bias rail offset	p-stop width	Bias rail material	FE-I4 sensor equivalent
(1)	50×400	End	PolySi	Inside	2	Large	Narrow	Al	Type(2)
(2)						Small			Type(4)
(3)					1	None	Wide		Type(5)
(4)				Inside[a]					Type(6)
(5)				Outside					Type(7)
(6)							Narrow		Type(8)
7				Inside	2	Large		PolySi	Type10
8						Small			Type12
9					1	None	Wide		Type13
(10)			PT	–	Straight			Al	Type(16)
(11)					Zigzag	Small	Narrow		Type(17)
(12)						Large			Type(18)
13			None		–	–		–	Type19
(14)	25×800	End	PT	–	Straight	None	Wide	Al	Type(20)
(15)			PolySi	Inside[b]	1				Type(21)
16					2	Large	Narrow	PolySi	Type22
(17)		Center	PT	–	Zigzag	Large		Al	Type(23)
(18)			PolySi	Inside[b]	2	Small			Type(24)
19		Staggered			1	Large		PolySi	Type27
20		End	None	–	–	–		–	Type28

[a] No opening in the DC-Al metal of the pixel implant under the PolySi trace.
[b] PolySi is routed along one side of the perimeter of pixel implant.

boundary between the silicon bulk and the surface SiO_2. After irradiation, space charge concentration, leakage current, and fixed interface charge are taken to be increased by one order, three orders, and two orders of magnitude, respectively, caused by displacement and ionization damages. The parameters before and after irradiation are summarized in Table 2, in columns of "Non-irrad." and "Irrad.", respectively (hereafter referred to as Non-irrad. and Irrad.). The values of the geometry parameters are summarized in Table 3.

4.1. *Effect of electric potential of the bias rail*

In the DUTs with polysilicon bias resistors, the pixel electrode is connected to the bias rail through the polysilicon resistor. The pixel electrode is connected to the virtual ground of ASIC and thus the bias rail is at the ground potential. We used TCAD simulations to determine the electric field in the boundary region near the surface of the silicon (1 μm below the surface of silicon in the TCAD geometry) with and without the bias rail. The electric

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potentials before and after irradiation are shown in Fig. 6(a) and (b) for the narrow p-stop geometry (widths of bias rail and p-stop being 8 and 4 μm), with the Non-irrad. (bias voltage of −100 V) and the Irrad. (−430 V) conditions, respectively. The data obtained with and without the bias rail are shown by filled circles and squares, respectively. The existence of the ground potential induced a difference of approximately 1 V over the electric potential of 16 V before irradiation and of 2 V over 42 V after irradiation at the location of the bias rail. The differences are small and the fractions to the total potential are similar before and after irradiation. The difference of the interface charge before and after irradiation generates a subtle difference in the shape of the electric potential between the p-stop and the pixel electrode, but only slightly influences the values of the potentials with and without the bias rail. The existence or non-existence of the ground potential does not appear to be the source of efficiency loss at the boundary.

4.2. Charge induced on the bias rail

A moving charge in the presence of any number of electrodes kept at constant voltages induces a mirror charge on the electrodes according to Ramo's theorem:

$$Q_A = q \cdot V_{qA}, \tag{1}$$

where Q_A is the charge induced on an electrode A, q is the charge at a given position, and V_{qA} is the "weighting potential" of the electrode A at the position of the charge q. In a finite time, with a fast readout electronics, instantaneous induced current i_A is represented by the gradient of V_{qA} along the direction of motion multiplied by the drift velocity:

$$i_A = q \cdot \frac{dV_{qA}}{dt} = q \cdot \left(\frac{\partial V_{qA}}{\partial x}\frac{dx}{dt}\right) = q \cdot \vec{v} \cdot \overrightarrow{\frac{\partial V_{qA}}{\partial x}} = q \cdot \mu \vec{E} \cdot \overrightarrow{\frac{\partial V_{qA}}{\partial x}}, \tag{2}$$

where μ is the charge carrier mobility and E is the electric field. Although the current has to be integrated to evaluate the charge, an insight into the physics can be obtained qualitatively and visually from the maps of the electric field E, the flow lines of the electric field representing the drifting paths of the charge carriers, and the weighting potential V_{qA}.

Since the drifting carriers do not terminate on the bias rail, the current induced on the bias rail is bipolar. The collection time of charge carriers (electrons in n^+ electrode) is in the order of 10 ns. Since we use a fast-shaping amplifier (peaking time of approximately 20 ns), the early part of the bipolar signal will result in a finite amount of charges induced on the bias rail. Thus, it is natural to expect that charge will be lost to the bias rail, causing efficiency loss. However, it is unclear why we observe efficiency loss only after irradiation and not prior to it.

4.3. Visualization of the fields and predictions by TCAD

The weighting potential is independent of the space charge distribution and actual voltages, however, it depends on the geometry of the electrodes and the resulting electric field. In a semiconductor device the actual shape of the electrode is bias dependent due to the change in depletion volume, for instance. In the p-type device the effective extent of the n^+ electrode is bias dependent due to the existence of inversion layer in the n-side surface of silicon. The radiation damage by charged particles on the surface of device leaves positive fixed charge at the interface of $Si–SiO_2$. The inversion layer is created by the electric potential of the positive fixed charges that repels the holes from the silicon surface. The potential of the fixed interface charge is partially compensated by the potential at the surface of silicon generated by the bias voltage (see Fig. 6), thus the extent of the inversion layer is bias dependent.

Using the geometry setup and the conditions described above, we extract two-dimensional maps of fields. The inversion layer is indeed simulated in the TCAD as shown as the electron density in the surface of silicon in Fig. 7, (a) before irradiation (with Non-irrad. condition: $Q_f = 1 \times 10^{10}$ cm^{-2}, bias voltage −100 V), (b) as same as (a) but $Q_f = 1 \times 10^{12}$ cm^{-2}, and (c) after irradiation (with Irrad. condition: $Q_f = 1 \times 10^{12}$ cm^{-2}, bias voltage −430 V). There is little inversion layer before irradiation due to the low density of the interface charge. The inversion layer is visible with the interface charge density after irradiation; extends from the n^+ electrode toward the p-stop (edge at −2 μm) approximately to −3 and −5 μm with the bias voltage of −100 V and −430 V, respectively. Visual thickness of the layers in the plots should be due to the resolution of the calculation and plotting.

The weighting potential of the electrode of interest is calculated from the difference of the two maps of the electric potential: the map with the setup and that obtained by adding 1 V to the electrode of interest over the setup. The remnant is the potential where the selected electrode at unit potential, all other electrodes at zero potential. The extracted fields are shown in Fig. 8 for the narrow p-stop geometry in the rows of (a) electric field E overlaid with flow lines of the field and (b) weighting potential of the bias rail V_{qA}, in the columns of before (Non-irrad., −100 V) and after irradiation (Irrad., −430 V), respectively.

Examination of Fig. 8 shows that there are several distinctive differences between the fields before and after irradiation. Prior to irradiation, the electric field shows a large blob of low electric field region under the bias rail/p-stop, the flow lines of the electric field, i.e., the path of drifting carriers are deflected from the low electric field region toward the pixel electrodes distinctly, and the intensity of the weighing potential of the bias rail is not extending in the area and vicinity of the low electric field region. The area of low electric field region appears to function as a shield against the drift paths and the weighting potential. After irradiation, the blob of low electric field region under the bias rail becomes minute, the flow lines are not deflected very much, and the intensity of the weighting potential extends more near to the bias rail and more toward the backplane. The shrinkage of the blob is caused by the strong electric field generated by the large bias voltage applied to cope with the space charge (N_{eff}) increased by the radiation damage in the silicon bulk. The extent of the inversion layer shields the weighting potential to remain in the vicinity of the bias rail.

The charge induced on the bias rail is determined by the interplay of the weighting potential and the path of drifting carriers. By overlaying the flow lines over the weighting potentials, we observe that before irradiation the drifting carriers from most of the bulk do not pass high intensity region of the weighting potential, but after irradiation drifting carriers especially from the bulk under the bias rail pass through. On the basis of the visualization, we conclude that the charge induced on the bias rail is small (almost zero) before irradiation but finite after irradiation.

The TCAD simulations have also predicted only a slight efficiency loss in the pixel structure with the wide p-stop geometry (widths of bias rail and p-stop being 4 and 8 μm) after irradiation, and in the old pixel structure after γ irradiation. Fig. 9 shows in the rows of (a) electric field overlaid with flow lines and (b) weighting potential, in the columns of the cases of wide p-stop geometry after irradiation (Irrad., wide p-stop) and of narrow p-stop geometry before irradiation but with the interface charge as that after irradiation (Non-irrad., $Q_f = 1 \times 10^{12}$ cm^{-2}), respectively. The latter scenario corresponds to the case of γ irradiation. In both cases, the weighting potentials are very low and uniform over a wide region including under the bias rail/p-stop region. The low electric field

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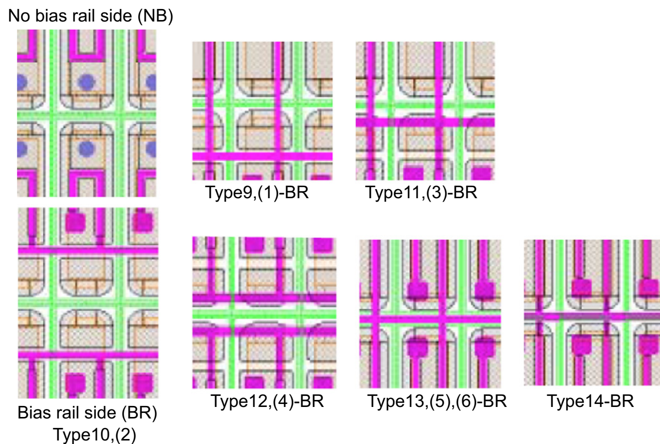

Fig. 10. Pixel structures in wafer layout #4 of Types 1–6 and 9–14 with variations of number of bias rails and their locations. Bias rail is made of polysilicon (Types 9–14) or aluminum (Types 1–6).

region under the p-stop and the extent of the inversion layer are nearly overlapping, thus seem to shield the weighting potential against extending into the silicon bulk. The γ irradiation study was motivated by the TCAD prediction.

5. Summary

We have developed n^+-in-p pixel sensors, using planar process in p-type 6-inch silicon wafers to obtain highly radiation tolerant sensors for extremely high radiation environments such those found in HL-LHC. We have designed novel pixel structures – wafer layout #4 – to eliminate the efficiency loss at the pixel boundary observed in the old pixel structure of the wafer layout #2, especially after irradiation. The new pixel sensors were irradiated with protons at a fluence of approximately 3×10^{15} n_{eq}/cm^2 at CYRIC or with γ rays at a dose of 2.4 MGy at TARRI, and evaluated with test beams at CERN and DESY.

- Among the novel pixel structures tested, the best pixel structure to retain high efficiency after irradiation is the one with "Large offset" where the bias rails removed far away from the boundary and the polysilicon biasing resistor routed inside the pixel implant region, achieving an efficiency loss of <0.5% per pixel at the boundary, as efficient as that without the bias rail.
- If offsetting the bias rail were not applicable, the one with "Wide p-stop" geometry could be an alternate solution, achieving a loss of approximately 1% per pixel at the boundary.

We have also obtained an understanding of the physics underlying the efficiency loss under the bias rail with TCAD simulations, by simulating the electric fields, especially the weighting potential of the bias rail.

- The efficiency loss is due to the loss of charge induced on the bias rail.
- The difference of the charge induced on the bias rail before and after irradiation is caused by the difference of the region of low electric field under the bias rail together with the extent of the inversion layer in the surface of silicon.
- Before irradiation, a large blob of low electric field region under the bias rail makes the weighting potential very low in the area and vicinity, deflects drifting carries out of high intensity region of the weighting potential.
- After irradiation, the blob becomes minute due to strong electric field in the radiation-damaged silicon, which together with the extent of the inversion layer makes the weighting potential to extend more into the silicon under the bias rail, makes drifting carriers especially from the region under the bias rail to pass through high intensity region of the weighting potential.
- The TCAD simulations have also shown that wide p-stop and large $Si–SiO_2$ interface charge (inversion layer, specifically) act to shield the weighting potential against extending into the silicon bulk. The pixel sensor with old pixel structures irradiated with γ rays has confirmed little efficiency loss at the boundary.

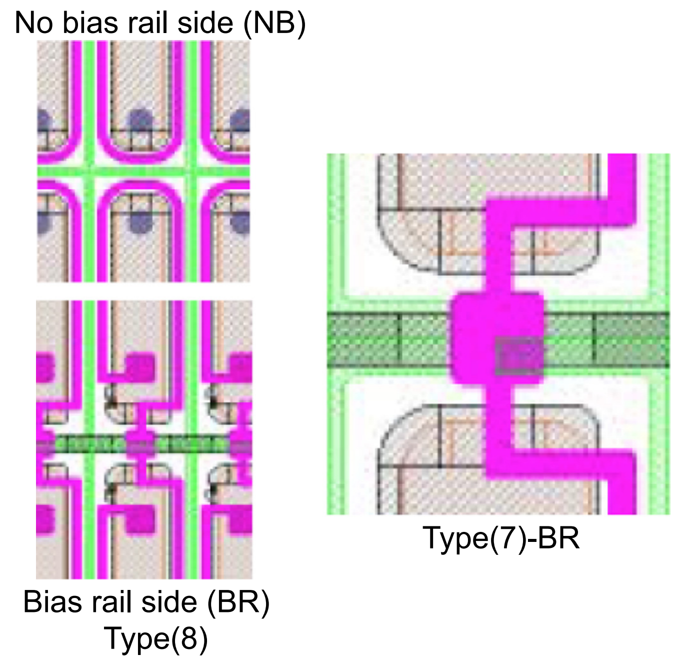

Fig. 11. Pixel structures in wafer layout #4: Type 8 with polysilicon bias resistor routing outside the pixel implant with the width of p-stop narrower than the width of bias rail (narrow p-stop, old design), and Type 7 with wide p-stop.

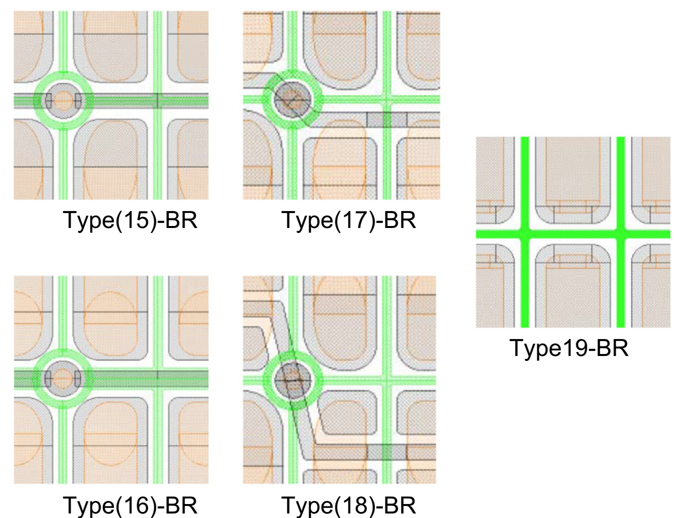

Fig. 12. Pixel structures of punch-through (PT) bias resistor in wafer layout #4: Types 15 and 16 with narrow and wide p-stop, and 17 and 18 with small and large offset of bias rails, respectively. Type 19 is without a biasing structure.

Acknowledgments

The irradiations were performed, with protons at Cyclotron and

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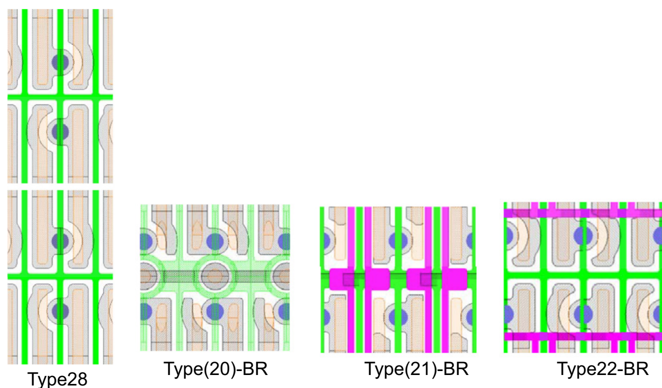

Fig. 13. Pixel structures of the 25 × 500 μm² pixel size with the bump bonding pads at the end of the pixels in wafer layout #4: Type 28 without a biasing structure, 20 with PT biasing and wide p-stop, 21 with PolySi biasing and wide p-stop, and 22 with PolySi biasing and large offset of bias rails.

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Appendix A. Pixel structures in wafer layout #4

In the wafer layout #4 (Fig. 2), we have designed several variations of the structures to investigate and evaluate the novel pixel structures in FE-I4 and FE-I3 pixel sensors. The characteristics of 28 variations in the FE-I4 pixel sensors and 20 in that of the FE-I3 pixel sensors are summarized in Tables 4 and 5, respectively. The material of the bias rail is either polysilicon (referred to as "PolySi") or aluminum (referred to as "Al"). The pixel structure with the Al bias rail is symbolized with the type number in parenthesis. The detailed views of the pixel structures are shown in Figs. 10–14. The pixel structures of bias rail side and no bias rail side are labelled with BR and NB, respectively.

A.1. FE-I4 sensors

The 19 variations from Types 1 to 19 are fabricated using a pixel size of 50 × 250 μm² (column "Pixel size" in the tables, Figs. 10–12). The 9 variations from Types 20 to 28 are fabricated with a pixel size of 25 × 500 μm², mating to the same grid of the bump pads of the FE-I4 readout ASIC, splitting the 50 μm of short pixel direction into two 25 μm pixels and merging two pixels to 500-μm-long pixels in the long pixel direction to study a finer pitch of the pixels (Figs. 13 and 14).

In the 50 × 250 μm² pixels, the location of the bump pads (column "Bump pad") is always at the end of pixel electrodes (referred to as "End", e.g. Fig. 10) in the NB side for Types 1–19. In the 25 × 500 μm² pixels, the locations of the bump pads are, (1) at the end of pixel electrodes for Type 20, etc. (Fig. 13), (2) at the center of pixel electrodes (referred to as "Center" in the tables, BP in Fig. 14) for Type 23, etc., or (3) at the center and the end alternately (referred to as "Staggered") for Type 27 (Fig. 14) to make the pixel electrodes to be staggered by half pitch in the long pixel direction. The staggered pixel layout is used to evaluate improvements in position resolution in the long pixel direction because more two-cluster hits are expected in the 25 μm pixels than in the 50 μm pixels.

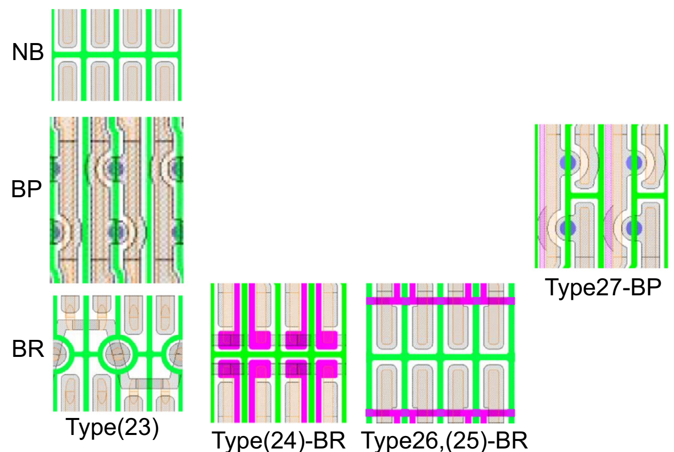

Fig. 14. Pixel structures of the 25 × 500 μm² pixel size with the bump bonding pads at the central region of the pixels or at staggered pixels in wafer layout #4: Type 23 with PT biasing and small offset of zigzag bias rail, 24 with PolySi biasing and small offset of bias rails, 26 and 25 with PolySi biasing and large offset of bias rails, and 27 with PolySi biasing with half-pitch (250 μm) staggered pixels.

The bias resistor is either formed with a resistive trace of polysilicon material, approximately 5 kΩ/μm (column "Bias type", referred to as "PolySi") or a punch-through structure with a narrow gap, approximately 18 μm between a bias dot (n^+ implant) and the pixel electrodes (n^+ implant) (referred to as "PT"). The PolySi resistor is routed (column "PolySi routing") to place the trace either "inside" the area of pixel electrode (Fig. 10) to mitigate the efficiency loss under the trace or "outside" the pixel area for Types 7 and 8 (Fig. 11) as a reference to the old design.

One approach for the removal of the bias rail out of the boundary region is to use two bias rails for a pair of pixel rows (column "Bias rail"), placing them in the pixel area largely away from the boundary (referred to as "Large offset", column "Bias rail offset", e.g. Fig. 10 Type 10) or just over the edge of the pixel electrode (referred to as "Small offset", Fig. 10 Type 12). The other is to keep one bias rail at the boundary (referred to as "None") but to increase the width of the p-stop under the bias rail while keeping the width of the bias rail narrow (referred to as "Wide", column "p-stop width", Fig. 10 Type 13), otherwise narrow (referred to as "Narrow", Fig. 10 Type 14).

In the case of PT structures, one PT dot is shared by four pixels in a pair of pixel rows to which one bias rail is placed [20]. The bias rail is either straight (referred to as "Straight", column "Bias rail") with the wide p-stop under the bias rail ("Wide", column "p-stop width") or zigzags ("Zigzag", column "Bias rail") by passing through the bias dot and then being largely removed away from the boundary region ("Large offset", column "Bias rail offset") or just over the edge of the pixel electrode ("Small offset", Fig. 12).

The material of the bias rail is listed in the column "Bias rail material". Historically, Al has been used. The resistance of the biasing network is a source of electrical noise (parallel noise). Larger resistance gives smaller noise, leading to our preference to "PolySi".

The similar structures of PolySi and PT are implemented in the 25 × 500 μm² pixels (Types 20–28, Figs. 13 and 14). The pixel structure without the biasing network ("None", column "Bias type") is used as the reference due to it showing the best performance (Type 19, Fig. 12 for the 50 × 250 μm² and Type 28, Fig. 13 for the 25 × 500 μm²pixels).

A.2. FE-I3 sensors

The characteristics of the variations in the FE-I3 pixel sensors

are summarized in Table 5. The pixel structures are limited to 20 variations due to the available space in the wafer layout. The 13 variations from Type 1 to 13 used $50 \times 400\,\mu m^2$ pixels. The 7 variations from Type 14 to 20 used $25 \times 800\,\mu m^2$ pixels. The basic structures are copied from the FE-I4 pixel structures. The pixel structures equivalent to the FE-I4 sensors are listed in the "FE-I4 sensor equivalent" column in Table 5.

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