Evaluation of Monolithic Silicon-On-Insulator Pixel Devices Thinned to 100 μm

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Abstract– **We are developing monolithic pixel devices utilizing a 0.2 μm Fully Depleted Silicon-on-Insulator (FD-SOI) process technology provided by OKI Semiconductor. We have investigated thinning the devices to 100 μm. Thinning enhances the feature of monolithic SOI sensors in views of minimizing the overall material and realizing full depleted devices. The latter is necessary for backside illumination, which is desirable to enhance the photo sensitivity. The wafer was thinned commercially by DISCO Corp. Small increase in the leakage current was observed associated with the thinning process. Excellent performance to infrared and red laser lights was obtained, demonstrating realization of the fully depleted pixel device.**

I. INTRODUCTION

THINNING of pixel sensors is crucial in several applications. In high-energy physics experiments, for example, the number of sensor layers tends to be large while requiring thinner sensors in order to reduce multiple Coulomb scattering [1]. This trend is a result of required smaller pixel sizes and development of low noise amplifiers where sensors of approximately 100 μm thickness can provide an adequate signal to noise ratio for traversing charged particle detection. In photo-imaging applications, back illumination is desirable to enhance the photo sensitivity [2], [3]. This is particularly important for pixels with smaller sizes, since the on-pixel structures may occupy the substantial area reducing the area necessary for front illumination. Thinning is mandatory in our Czochralski grown substrate for full depletion, which is required in back illumination.

We are developing monolithic pixel devices [4], [5], [6] based on a 0.2 μm silicon-on-insulator (SOI) technology provided by OKI Semiconductor Co., Ltd. Fig. 1 illustrates the schematics of our SOI pixel device. By using bonded wafers, we adopt a high resistivity (approximately 400 Ωcm) n-type substrate as the sensitive part and a normal resistivity (18 Ωcm) p-type SOI silicon as the electronics part. The SOI silicon of 40 nm thickness and the substrate of 725 μm, as processed, are separated by a 200 nm thick buried oxide (BOX) layer. In our standard procedure, the backside is ground to 260 μm and aluminum is deposited for backside contacts. The buried p-well (BPW) in Fig. 1 is a novel technique recently adopted [4]. The BPWs are either tied to the pixels or to the ground in the peripheral circuits, thus the potentials underneath the BOX layer can be fixed, which is

effective to suppress the effects of the backside detector bias to the electronics operation, so called the back-gate effects.

One of the advantages of monolithic SOI devices is reduction of the overall detector material. The advantage becomes more striking by thinning the sensor. We thinned a wafer to 100 μm by TAIKO process [7]. We examined the thinning process induced damage through the leakage current increase, and measured the warp profile. With 100 μm thickness, the device can be fully depleted. We evaluated the response to infrared and red lasers injected from the front and back sides.
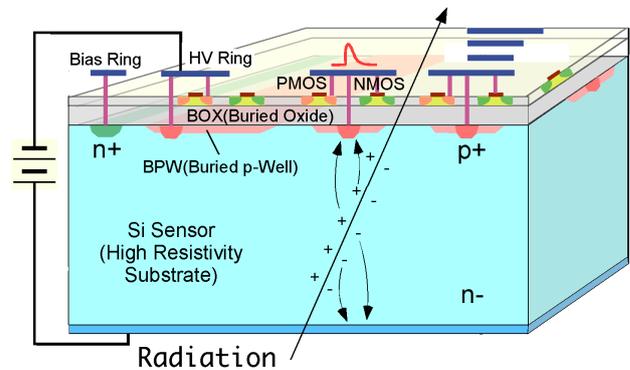

Fig. 1. Schematics of the SOI monolithic pixel device. The pixels, fabricated through the BOX layer, are connected to the SOI MOS transistors via metal layers on top of the device. The device can be biased from the back or from the front n^+ contact (Bias Ring).

II. INTPIX3 AND THINNING PROCEDURE

The SOI fabrication was carried out on a basis of multi project wafer runs, processing various types of sensors on a same 8" wafer. We picked up INTPIX3b chips [4] in order to quantify the thinning quality. The INTPIX3b chip is a signal integration type device having an array of 128 × 128 pixels of 20 μm square. The outer chip size is 5 mm square. Each pixel has an active pixel type circuit (see Fig. 2) integrated. The pixel charges extracted out one by one are digitized by a 12-bit ADC, which is implemented in a TCP/IP based readout system, SEABAS [8].

The INTPIX3 is a first device where BPW's are integrated. In order to optimize the BPW configuration, the pixels are divided into eight regions and different configurations are examined. Fig. 3 illustrates one of the configurations we used in this study. There is a window of 5 μm square where there is no metal layers at the center, allowing front illumination.
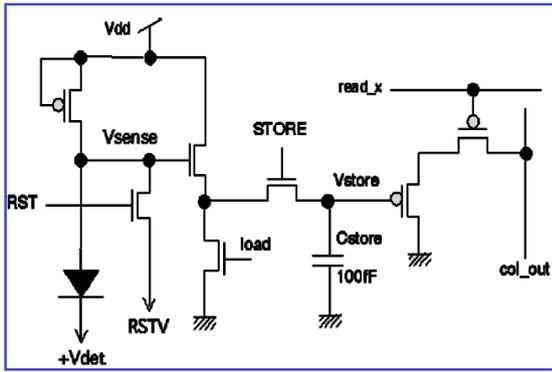
Fig. 2. Diagram of the INTPIX3 on-pixel circuit. The charge stored in `Cstore` is sent out to the common column line.
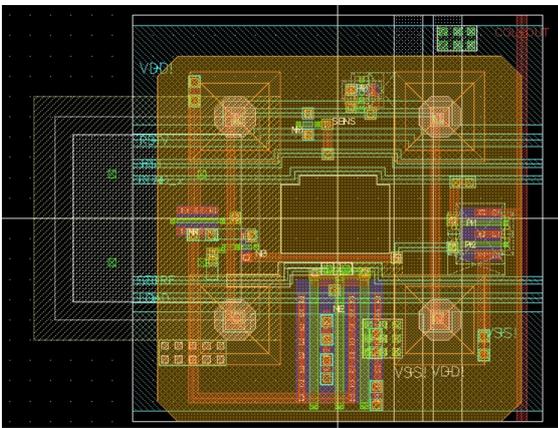

Fig. 3. Configuration around the pixel. The pixel size is 20 μm square, having four octagonal p^+ implants. The BPW (yellowish) which is tied to the implants covers the almost entire pixel area. At the center of the pixel, there is a no metal region of 5 μm square.

The wafer was thinned to 100 μm by TAIKO process provided by DISCO Corp. [9] With this process, the outer edge of the wafer is left un-ground. So thinned wafer is self sustainable, reducing the risk of handling such as at stress relief processing and backside aluminizing. The stress relief process removes the damages and residual strain created at grinding, consisting of dry polishing, chemical mechanical polishing, and wet and dry etchings. Finally the backside was aluminized.

III. LEAKAGE CURRENT

The leakage currents of the same INTPIX3b chips were measured on wafer before and on diced chips after thinning. Fig. 4 compares the I-V curves. The values are normalized at 25°C. The numbers in the plots indicate the positions of the measured chips distributed over on the wafer (see Fig. 5). The breakdown seen around 125 V – 130 V is caused at the corners of the HV ring (see Fig. 1), which is not affected by the thinning process. There are no data available for chips 1 to 7 after thinning: They were used for packaging and other studies.
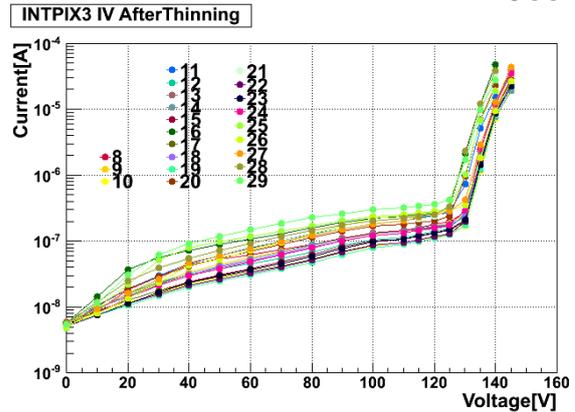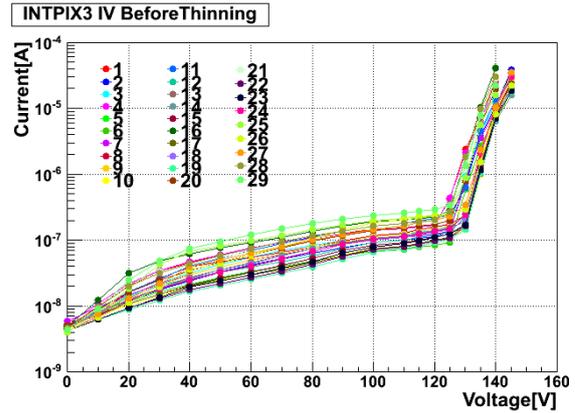

Fig. 4. IV curves of INTPIX3b chips (top) before and (above) after thinning. The thicknesses are 725 μm and 100 μm, respectively.
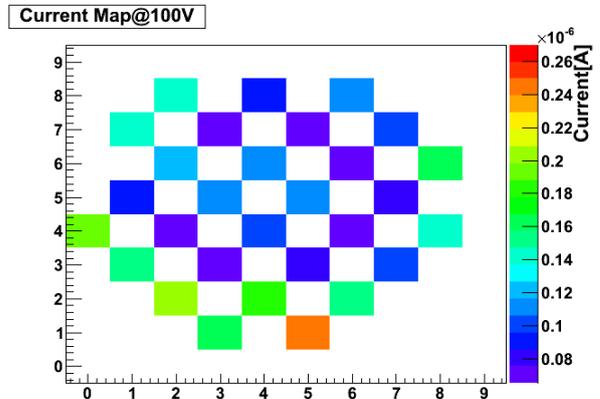

Fig. 5. Leakage currents at 100 V of 29 chips before thinning. Each colored area is 20 mm square, corresponding to the unit of the mask pattern. The measured chips, one per unit, are distributed over the whole wafer area.

The leakage current increases at 100 V are summarized in Fig. 6. All chips showed an increase by 12% to 26% of the values before thinning. There is a tendency that the increase is larger for the lower chips. As described later, the thinned devices are fully depleted at 90 V. The increase should be attributed to the backside structure, residual defects, and development of field lines towards the sides.
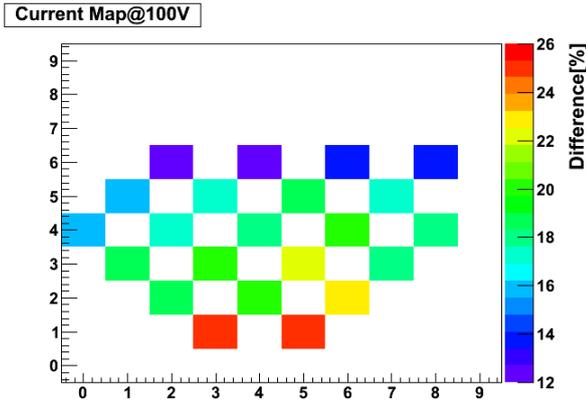
Fig. 6. Leakage current increase in percentage at 100 V.

IV. HEIGHT PROFILE

The height profiles of thinned devices were measured in blocks with side lengths of a few cm. Fig. 7 is an example of the profile measured for a block of 40 mm × 80 mm. With respect to the plane defined by the three corners, the center of the block and the fourth corner are high by 0.4 mm and 0.05 mm, respectively. Other blocks showed profiles similar in shape, and the heights are characterized by the side lengths. Such convex profiles with the electronics side up can be caused by different coefficients of thermal expansion between silicon and SiO_2, namely due to the residual strain created at the SOI processing. If the strain due to the thinning is substantial, the shapes may differ, although we cannot extract such contribution from the present measurement. The warp of diced chips is not large and can be manageable.
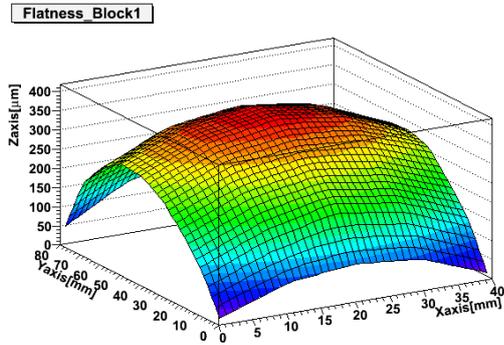

Fig. 7. Height profile of a block of 40 mm × 80 mm. The SOI circuits are on the convex side.

V. RESPONSE TO IR AND RED LASERS

We estimated the depletion depth by collecting the charge to 1064 nm IR laser as a function of the detector bias V. Since this laser penetrates the Si substrate [10], the collected charge which is proportional to the depleted depth should be proportional to $\sqrt{V}$ at biases below the full depletion.

Fig. 8 shows the collected charge of a 100 μm thick INTPIX3 when the IR laser was collimated and injected inside the front window of 5 μm square. As expected, the charge increases linearly with $\sqrt{V}$ and deviates from the line above 80 V. For 260 μm thick INTPIX3 pixels, the collected charge increases linearly up to the maximum voltage of 140 V.
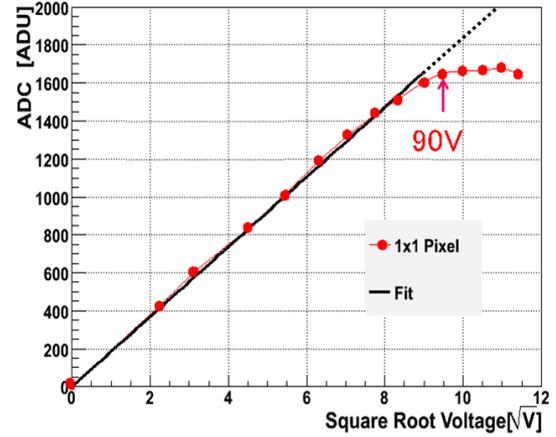

Fig. 8. Collected charge for IR laser injected from the top. The abscissa is square root of the bias voltage.

The ceramic package for the thinned INTPIX3 had a through hole under the sensitive region made with a waterjet cutter, and the backside aluminum was removed so that the device can be back illuminated. The response to the collimated IR laser is plotted in Fig. 9, which shows a similar dependence on the bias as the one obtained from front illumination.

Also shown in the figure are the results for a red (634 nm) laser [11]. Because the red laser was spotted to about 1 mmϕ, the response was evaluated from a single pixel, or from averages of neighboring pixels, all of the curves overlapping each other. The collected charge increases rapidly about 70 V and is saturated above 100 V, suggesting the device is fully depleted above around 90 V.
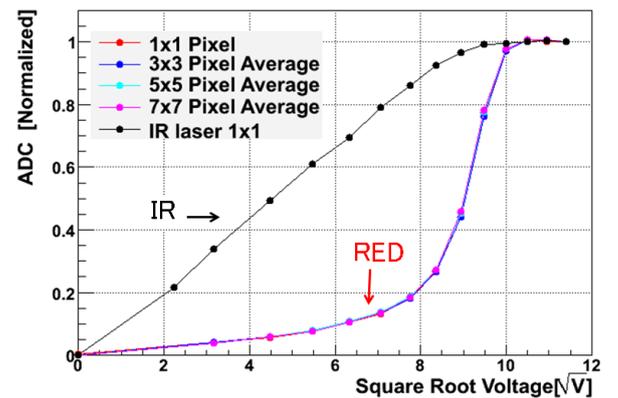

Fig. 9. Collected charge for IR laser and red laser injected from the back. The outputs are normalized at 100 V and above.

We notice that the charges are collected even at lower voltages while the red light should be absorbed at the surface: 3 μm is the absorption length in silicon. This suggests that a

fraction of the carriers diffuse out the non-depleted region and are collected.

The backside aluminum was removed only for the pixels at center. In order to investigate the effect of diffusion for the red laser, we evaluated the response of the pixels that are covered by the residual aluminum. The outputs are plotted in Fig. 10 at fixed bias voltages for the pixels across a column. The unit of CA is the pixel size 20 μm. The pixels with CA 81 and above are covered but show response, which is dependent on the bias. At a few 10 V, two to three pixels at the boundary are responding, meaning a diffusion of 40 μm to 60 μm is possible. At 100 V and above, there is a negligible contribution since the device is fully depleted and the diffusion is minimized.
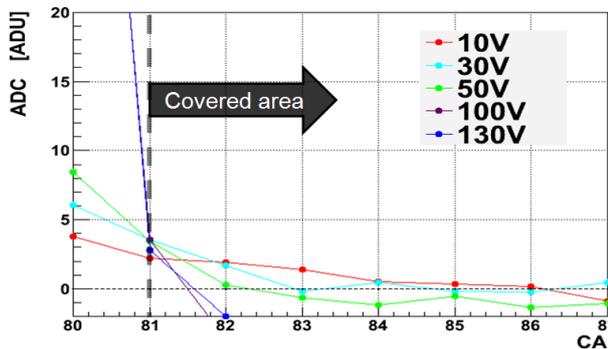

Fig. 10. Collected charge for red laser injected from the back. The abscissa is in unit of 20 μm extending to the pixels covered by aluminum.

VI. Summary

We are successful in thinning monolithic SOI pixel devices to 100 μm. There is a small increase in the leakage current and in the breakdown onset voltage. The thinned device was characterized by injecting penetrating infrared laser both from the front and back, and with back illuminated red laser. The bias dependence of the collected charge is as expected, showing that the device is fully depleted at around 90 V.

Acknowledgment

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