# Development of FD-SOI Monolithic Pixel Devices for High-Energy Charged Particle Detection

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***Abstract*– Monolithic pixel devices fabricated with a silicon-on-Insulator (SOI) technology are excellent candidates to realize particle detectors of fast response and least material yet simple in fabrication. In our SOI pixel devices the sensitive part is the "handle" wafer, to which we examined high resistive FZ wafers of both p- and n-types together with CZ wafer of n-type. Full depletion of the FZ wafers is easily achievable for typical thicknesses of 260 to 500 μm. We thinned these devices to 100 to 50 μm. The response was evaluated with infrared and red lasers, and in a high energy beam. Irradiation to $^{60}$Co γ was carried out to verify the radiation tolerance of the devices.**

## I. Introduction

THE potentiality of novel monolithic pixel devices utilizing the 0.2-μm fully depleted silicon-on-insulator (FD-SOI) technology provided by ROHM Lapis Semiconductor [1] has been intensively explored for various applications including γ/X-ray imaging and space applications [2]. The SOI handle wafer is high resistive silicon serving as the sensing part and the top is 40-nm thick silicon of 18 Ωcm, separated by a 200-nm thick buried oxide (BOX) layer, see Fig. 1. Such an SOI wafer is realized by adopting the bonded technique provided by SOITEC [3]. A notable feature is that the resistivity of the sensor part can be selected according to the application requirements.

There are several key issues in developing monolithic pixel devices for high-energy charged particle detection; e.g., least material, full depletion, and radiation tolerance.

- Least material is important for minimizing the multiple scattering. Thinning the sensor is particularly beneficial for the monolithic devices where the sensor itself is the main contributor to the amount of material, and is possible for the devices with least noise. We evaluated the sensor characteristics for the devices thinned to 50 μm and 100 μm. The thinned devices were tested in high energy beams.

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- With fully depleted devices, the charge is collectable faster, providing a constant amount for minimum ionizing particles. Fully depleted devices are realized by thinning (Czochralski, Cz sensors) and adopting high resistive FZ (Float Zone) wafers. We recently succeeded in adopting high resistive FZ wafers together with conventional Cz. While only n-type is available for high resistive Cz, both n-type and p-type are possible for FZ wafers. Fully depleted high resistive FZ wafers have an impact on hard X-ray and γ-ray imaging for increased detection efficiency.
- Radiation hardness is a rather complicated issue in SOI devices since the device is fully contained in oxide. We have carried out a detailed study on transistor basis characteristics [4]-[6]. Here we present the functionality of the devices irradiated to about 10 kGy following the annual radiation level of 1 kGy/y evaluated for ILD vertex detector to be located at a radius of 5 cm.

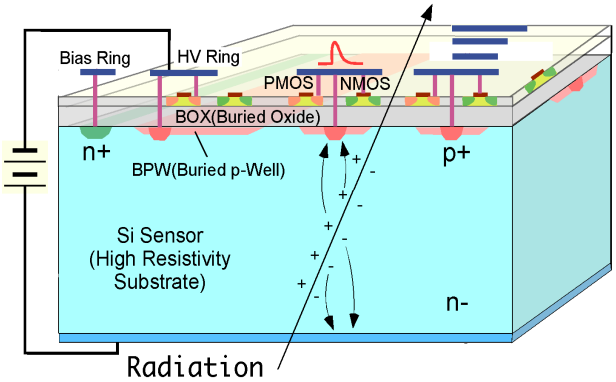


Fig. 1. Schematics of the SOI monolithic pixel device. The pixel electrodes, fabricated through the BOX layer, and SOI MOS transistor terminals are interconnected via metal layers on top of the device. The device is biased from the back or from the front $n^+$ contact (Bias Ring).

## II. INTPIX3 and DIPIX2

The SOI fabrication was carried out on a basis of multi project wafer runs [7], processing various types of sensors on a same 8" wafer. The main process parameters are summarized in Table I. As for the handle wafer, high resistive Cz (n-type) and FZ (n-type and p-type) are available. The default thicknesses are 260 and 500 μm, respectively. The FZ wafers are chosen to be rather thick to take full advantage of fully-depleted yet thick devices. The ground back surface was not annealed and found to produce large leakage current if the device is fully depleted and biased from the back though

aluminum. Therefore no aluminum was added to the FZ devices of the standard thickness.

TABLE 1. MAIN PROCESS PARAMETERS

| | |
|---|---|
| process | 0.2μm low leakage fully depleted SOI CMOS<br>1 poly+5 metal layers, MIM (1.5 μF/μm$^2$), DMOS<br>Core (I/O) voltage=1.8 (3.3)V, Buried p/n-Well |
| SOI wafer | diameter : 300 mmϕ<br>Top Si : Cz ~18Ωcm (p-type) ,40 nm thick<br>Buried oxide: 200 nm thick<br>Handel wafer: Cz(n, 0.7kΩcm), FZ(n,7k),FZ(p,40k) |
| Backside/ thickenss | Cz:thinned to 260μm, sputtered with Al (200nm)<br>FZ:thinned to 500μm (no Al)<br>Devices thinned to (50, 100 μm) available |

We evaluated two kinds of integration type devices [8], INTPIX3 and DIPIX2, see Table II. The INTPIX3e chips having an array of 128×128 pixels of 20 μm square are made on Cz(n) and FZ(n). The outer chip size is 5 mm square. Each pixel has an active pixel type circuit integrated, see Fig. 2. The pixel charges are extracted out of the chip one by one, then digitized by a 12-bit ADC, which is implemented in an SiTCP

TABLE II. CHARATCERISTICS OF DIPIX2 WAFERS AND AVAILABILITY OF THIN INTPIX3.

| WAFER TYPE | CZ (N) | FZ(N) | FZ(P) |
|---|---|---|---|
| RESISTIVITY [kΩcm] | 0.7 | 7 | 40 |
| THICK DIPIX2 [μm] | 260 | 500 | 500 |
| FULL DEPLETION [V] | 340 | 125 | 60 |
| THIN INTPIX3 [μm] | 50, 100 | 50, 100 | N/A |

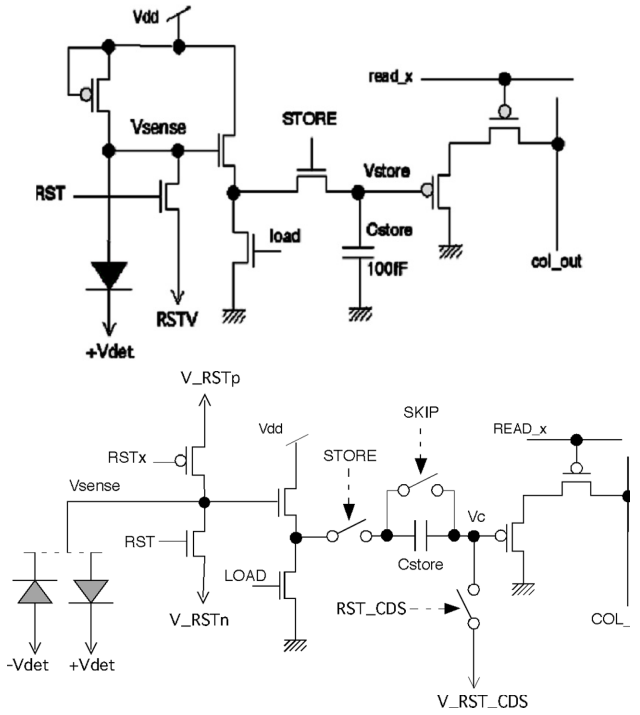


Fig. 2. Diagram of (top) INTPIX3 and (above) DIPIX2 on-pixel circuit. The charge stored in $C_{STORE}$ is sent out through the common column line.

based readout system, SEABAS [9]. Some of diced sensors were thinned to 50 μm or 100 μm by NIHON Exceed Co. [10]. Earlier version of INTPIX3a was thinned in a form of wafer by DISCO Japan [11]. The evaluation of the devices thinned by DISCO is reported elsewhere [12].

Since INTPIX3 is a first device where BPW's are integrated, the pixels of INTPIX3a are segmented into eight regions to examine various BPW configurations, including radiation hardness.

The DIPIX2 (Dual Integration type PIXel) was developed in order to read out both n- and p-type signals, as shown in Fig. 2. While other functions like CDS (correlated differential signal) and on-chip signal digitization are implemented, these were set inactive in this study. Therefore the DIPIX2 chips are similar to INTPIX3 chips except that there are 256×256 pixels of 14 μm square.

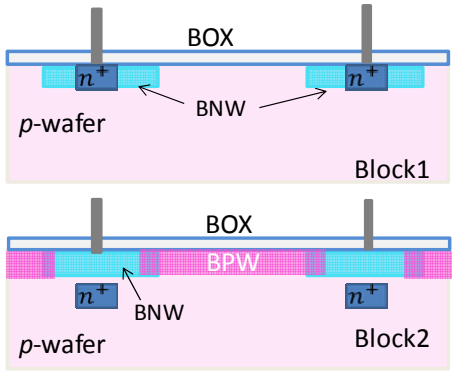


Fig. 3. Configuration of BNW and BPW in the case of p-bulk. All the charge polarities be inverted in the case of n-bulk.

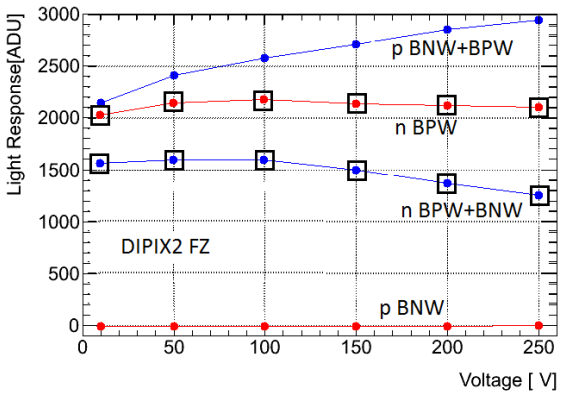


Fig. 4. Response to white light illuminated from the top of DIPIX2 chips. The curves are shown separately for the two blocks of FZ devices, BPW (BNW) only for n-type (p-type), and BPW+BNW.

In the DIPIX2 process, we added BNW for p-type sensor, which corresponds to BPW for n-type sensor. Half of the pixels (Block1) were processed in this way like INTPIX3. The rest half was processed adding both BPW and BNW together, as illustrated in Fig. 3. The BPW (in n) and BNW (in p) are tied to the pixel electrodes; sustaining the nearby potential and suppressing the back-gate effect not deteriorate the electronics performance. This is realized if the added electrodes are wide

enough while wider electrodes are easier to couple each other. The overlaid electrode, e.g. BPW for p-type, reduces the inter-pixel coupling, functioning like a p-stop. The effectiveness of additional BPW for the p-type device is evident in Fig. 4 where the response to white light is plotted as a function of the bias. The effectiveness of BNW for the n-type device is not clear from the data.

## III. Thinning

One of the wafers containing INTPIX3a chips was thinned to 100 μm [13] by TAIKO process provided by DISCO Corp. With this process, the outer edge of the wafer is left un-ground. So thinned wafer is self sustainable, reducing the risk of handling such as at stress relief processing and backside aluminizing. The stress relief process removes the damages and residual strain created at grinding, consisting of dry polishing, chemical mechanical polishing, and wet and dry etchings. Finally the backside was aluminized.

Thinned devices were examined on the full depletion using pulsed lasers. Fig. 5 shows the response of a 100 μm device to infrared and red lasers illuminated from the backside of the device [13]. The response to infrared increases with square root of the bias below the full depletion, reaching a constant above. The response to red laser is also consistent that the full depletion is achieved around 90 V.

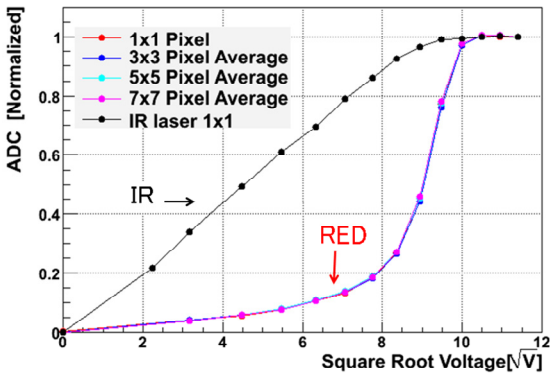


Fig. 5. Response to infrared (λ=1064nm) and red (λ=634nm) lasers injected from the backside of a 100 μm thick INTPIX3a[13].

Thinning by NIHON Exceed was made on diced INTPIX3e chips from the standard thicknesses. The surface was mechanically and chemically polished using abrasives developed to enable flattening to sub-micron precision. The backside of these devices were not aluminized.

The leakage current of the thinned devices is compared in Fig, 6. Although the leakage current increased by an order of magnitude for FZ devices, the device should be fully depleted already at 5 V for 100 μm, showing the increase is in the region above the full depletion. This increase should be attributed to the backside treatment at thinning. For Cz devices the full depletion is 90 V for 100 μm, showing that a contribution exists below full depletion for INTPIX3e. As a comparison, the I-V curve for INTPIX3a did not change by thinning process (by DISCO). We continue to investigate improvement if the devices are thinned by NIHON Exceed on a wafer basis or on a basis of block of chips.

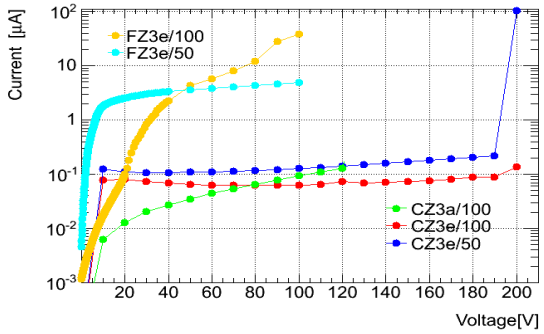


Fig. 6. Leakage currents measured at 20°C of thinned INTPIX3. Cz3b was thinned to 100 μm on a wafer basis; others are to 50 μm or 100 μm on a diced chip basis.

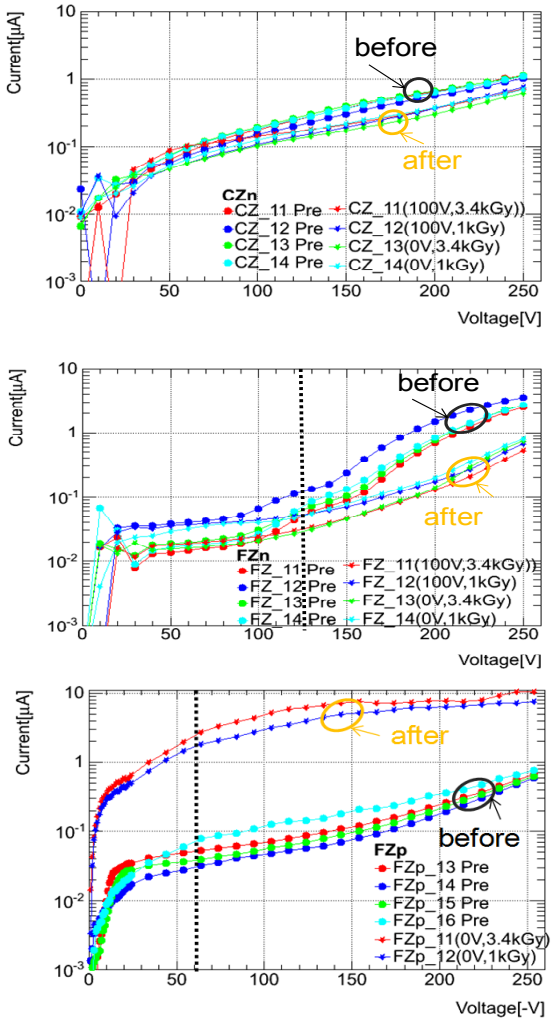


Fig. 7. IV curves of DIPIX2 chips before and after irradiation to 1 kGy and 3.4 kGy: (top) Cz n, (middle) FZ n, and (above) FZ p. The full depletion voltages are indicated by broken lines for FZ devices, which is 360 V for Cz n-type.

## IV. Cobalt Irradiation

### A. DIPIX2 irradiation

The DIPIX2 devices were irradiated with $^{60}$Co γ's, one group at 1 kGy/h and another at 3.4 kGy/h. The irradiation was interrupted every 15 min to evaluate the inter-radiation characteristics and lasted for 1 h in total. During the irradiation, all the terminals of the chips were ground.

The results are shown in Fig. 7 comparing the IV curves measured at 20℃ before and after the final irradiation. For the n-type devices both with Cz and FZ, the leakage current increase is small, or even decreases in the region above the full depletion for the FZ devices. The leakage current increases above the full depletion due to the field lines reaching the backside where many defects were created by thinning. Since there is no aluminum and the silicon surface should be oxidized. A possible interpretation is that the trapped holes created there develop an electron layer at the silicon surface after irradiation. This layer behaves like $n^+$, creating an ohmic contact which acts to reduce the leakage current.

Notable is the nearly two orders of magnitude increase of the leakage current in the FZ p devices. Some front side structure, most likely the bias structure should explain the increase since the leakage starts to increase below full depletion. The primary cause of irradiation is accumulation of holes in the oxide, which attract electrons at the silicon surface. These electrons are usually removed as the depletion develops. The removal is more efficient if the electron layer is near the junction. This preferable situation is realized in the n-bulk sensor, where the bias configuration is $p^+$-$n_e$(n)-$n^+$, with the electron layer being denoted as $n_e$ and (n) being the bulk to be depleted in competition with the electron layer. An explanation for the present observation is that the configuration is $p^+$-$n_e$(p)-$n^+$ in p bulk, where the p-bulk depletion starts at "ohmic" for the electron layer and hence the layer may be intact while the depletion develops. The surface layer depletion is less enhanced for higher resistive devices like our FZ p sensor. Addition of a floating p-stop ring between $p^+$ at edge (bias ring) and $n^+$ (HV ring) should shut the current flow through the radiation-induced electron layer.

The pixel response was measured in the same system used for pre-irradiation samples. The data shown in Fig. 4 are to be compared with the 1 kGy irradiated data shown in Fig. 8. For n-type devices, the difference between with and without BNW is small. The preference of having both BNW and BPW for the p-type device remains similar, while some response appeared after irradiation for the device without BPW. At a

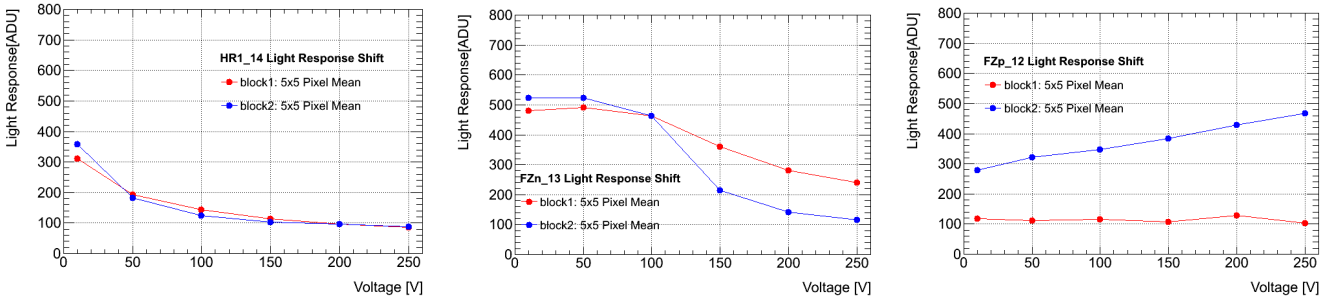


Fig. 8. Response to white light illuminated from the top of DIPIX2 chips, (top) Cz n-type, (middle) FZ n-type, (above) FZ p-type. The curves are shown separately for the two blocks, (red) BPW (BNW) only and (blue) BPW+BNW.

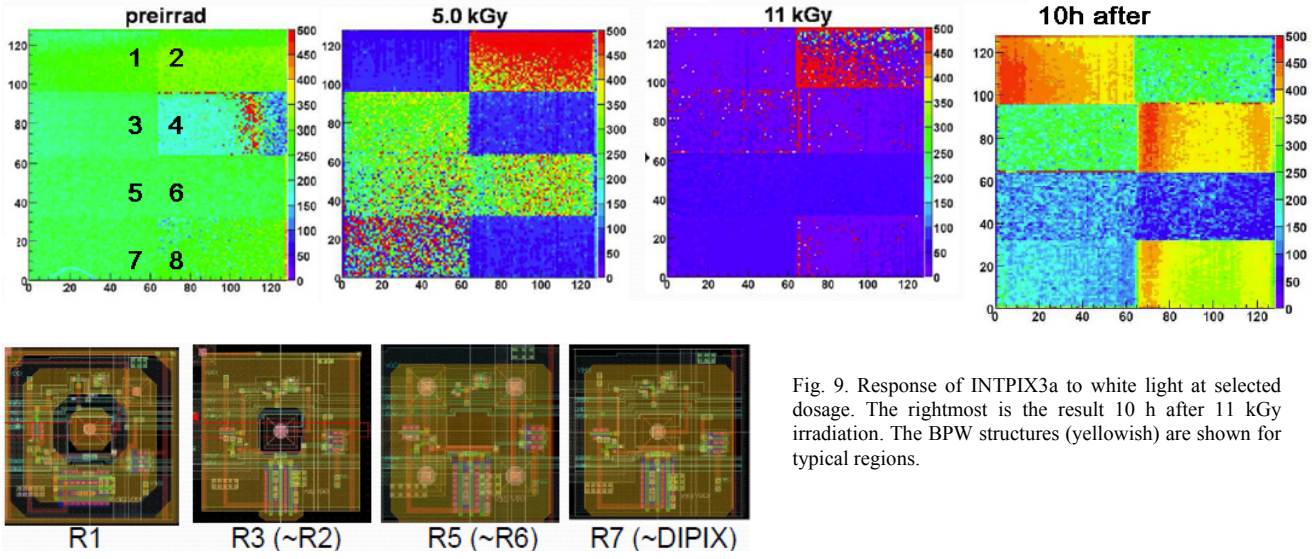


Fig. 9. Response of INTPIX3a to white light at selected dosage. The rightmost is the result 10 h after 11 kGy irradiation. The BPW structures (yellowish) are shown for typical regions.

bias of 100 V, the response is reduced to 1/15 for Cz-n, 1/5 for FZ-n, and 1/7 for FZ-p devices.

### B. *INTPIX3a irradiation*

The signal pulse height is dependent on the BPW/BNW structures since they contribute to the detector capacitance. Also the radiation tolerance is notably dependent on the structure. One INTPIX3a chip, where different BPW structures are implemented, was irradiated at 0.4 kGy/h to 3.4 kGy/h setting all the terminals at ground. The response was examined periodically by illuminating white light uniformly.

As shown in Fig. 9, the response diminished almost completely after 11 kGy where the irradiation was terminated. The device was kept in room temperature (ca. 15℃) for 10 h, then the response of some regions, R2 and R3, recovered to the level of pre-irradiation. The recovery is to compensate for the accelerated irradiation, but the response in some regions remained low. The DIPIX2 chip has single pixel electrode to which BPW/BNW is directly connected for n-type/p-type devices such that their potential is controlled by the pixel electrode. Region 7 is similar in configuration to DIPIX2, where the recovery is rather small.

In R3 the BPW potential can be set externally. Setting the BPW floating, or to positive voltage is necessary not to deteriorate the charge collection. The signal collection to charged particles is discussed below.

## V. Test Beam

### A. *Electron beam*

The INTPIX3a thinned to 100 μm was tested in electron beam of 673 MeV provide by 1.2 GeV electron synchrotron of Research Center for Electron and Photon Science, Tohoku University [13]. The cluster charge distributions are compared between the thinned INTPIX3a and 260 μm thick INTPIX3b. Although no identical BPW structures are available for INTPIX3a and INTPIX3b, INTPIX3a/R7 and INTPIX3b/R3 are picked up. The structures are similar but the area of BPW in INTPIX3b/R3 is smaller than INTPIX3a/R7.

The MPV of the distribution increases with the bias for the 260 μm thick device while it is consistent to be saturated for 100 μm one which is fully depleted at 90 V. The relative response at 100 V resulted in 1.4, which is consistent with 1.57 that accounts for the different sizes of the BPW and was extracted by a calibration using X-ray [8].

### B. *Pion beam*

The INTPIX4e devices thinned to 50 and 100 μm were tested in high energy pion beam provided by the SPS at CERN. Typical cluster charge distributions at 100 V for Cz and at 16 V for FZ are shown in Fig. 11 where the pedestal spread distributions are also shown. On a pixel basis, the on-beam pedestal spread is calculated as the sigma of a Gaussian fitted around the maximum of the charge distribution. The on-beam pedestal spread turned out to have somewhat wider distributions among the pixels than the off-beam pedestal spread.

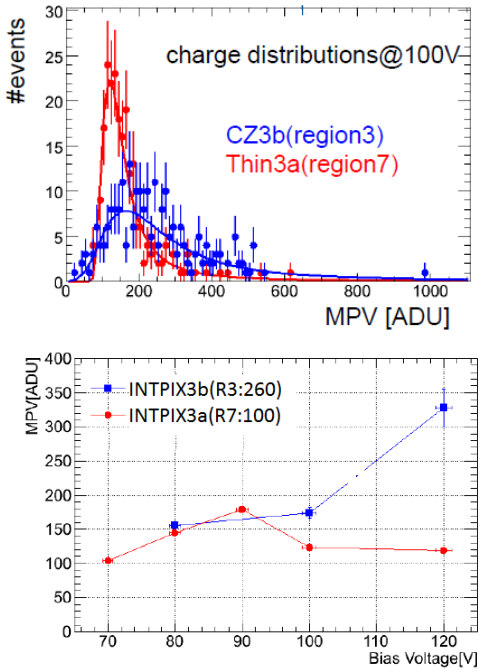


Fig. 10. (top) Cluster pulse height distributions compared between INTPIX3a (R7; 100 μm) and INTPIX3b (R3; 260 μm) at 100 V, (above) bias dependence of the most probable values.

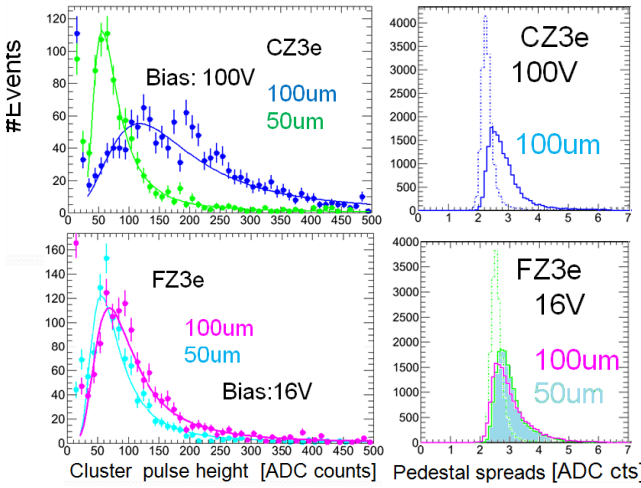


Fig. 11. (left) Collected charge distribution for pions compared between Cz and FZ INTPIX4e devices of 50 and 100 μm thicknesses. (right) The pedestal spread distributions are shown for on (solid) and off (dotted) beam.

The cluster charge distribution peaks corresponding to the charged pions. The MPV's are plotted in Fig. 12 as a function of square-root of the bias for Cz devices. The data for FZ devices are available only at 16 V. The ratio of the response of 50 μm and of 100 μm reflects the thickness ratio for Cz devices. The response ratio for the FZ is not described by the

thickness, although the data for 50 μm is similar to Cz of same thickness.

The signal-to-noise ratio is shown in Fig. 13 where the ratio is defined as the MPV of the signal distribution divided by that of the on-beam pedestal spread distribution. S/N ratio of about 40 is achievable for Cz devices of 100 μm thickness. Note that the devices were operated at room temperature and the noise can be reduced further by nearly a factor of three by lowering the temperature to 0℃ [14].

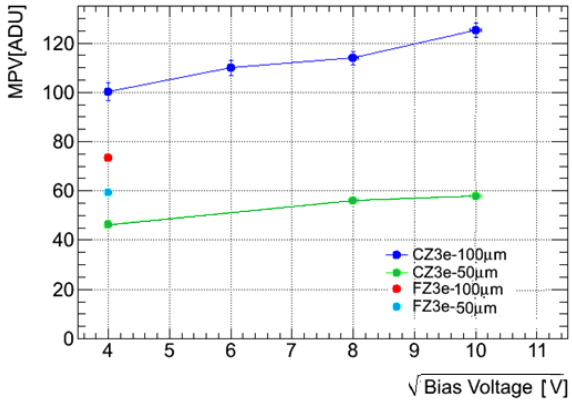


Fig. 12. The MPV of pedestal subtracted distributions as a function of square root of the bias voltage

The relative response of R3 to R7 of INTPIX3a was investigated in the CERN beam, which resulted in 1.48±0.11. Therefore, as discussed before, the BPW structure of INTPIX3a/R3 is radiation hard and emerges non inferior signal output as DIPIX2 and should be investigated further as radiation hard devices.

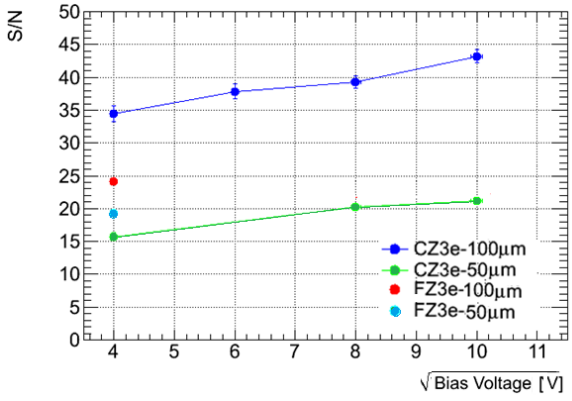


Fig. 13. The signal to noise ratios as a function of square root of the bias voltage.

## VI. Summary

Application of SOI pixel devices to high-energy particle detection is under investigation. Some key technologies such as thinning the devices to 100 μm or less and adopting high resistive FZ wafers have been realized successfully. Radiation hardness to 10 kGy and above has been demonstrated while the BPW/BNW designs need to be optimized both for signal collection and radiation hardness. The devices thinned to 100 μm were tested in a high-energy beam, providing a signal-to-noise ratio of 40 at room temperature.

## Acknowledgment

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