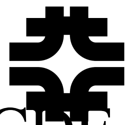

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CDF Run IIb Silicon: The New Innermost Layer

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Abstract— **The innermost layer (L00) of the Run IIa silicon detector of CDF was planned to be replaced for the high luminosity Tevatron upgrade of Run IIb. This new silicon layer (L0) is designed to be a radiation tolerant replacement for the otherwise very similar L00 from Run IIa. The data are read out via long, fine-pitch, low-mass cables allowing the hybrids with the chips to sit at higher z (~ 70 cm), outside of the tracking volume. The design and first results from the prototyping phase are presented. Special focus is placed on the amount and the structure of induced noise as well as signal to noise values.**

I. Introduction

THE design of the Run IIb upgrade of the CDF silicon detector [1] consists of six silicon layers. A critical part of the new design is the innermost layer, L0. This layer is essential for successful vertexing, tracking and for the second level displaced track trigger (SVT [2]). To minimize the scattering material in the first measurement layer, L0 follows the design of the Run IIa L00 detector. L0 sits at a radius of 2.1 cm. The main constraints for this innermost layer, close to the interaction region, are radiation hardness and low mass of the device. These lead to the development of a radiation hard readout chip (the SVX4 chip [3]) and to the usage of long, light-weight signal cables. These cables connect the sensors to the hybrids so that the hybrids with the chips and the associated cooling are outside of the tracking volume. A concern with these long cables is noise pick-up, and increased input capacitance, both potentially degrading the system performance. While offline algorithms can correct for the pick-up noise, this is not possible in the online data, feeding the displaced vertex trigger.

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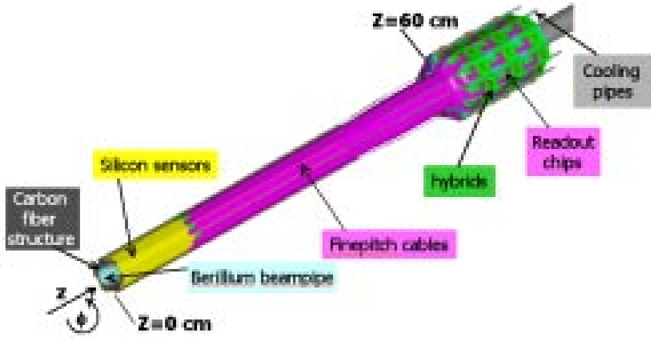


Fig. 1. Layout of the innermost layer L0

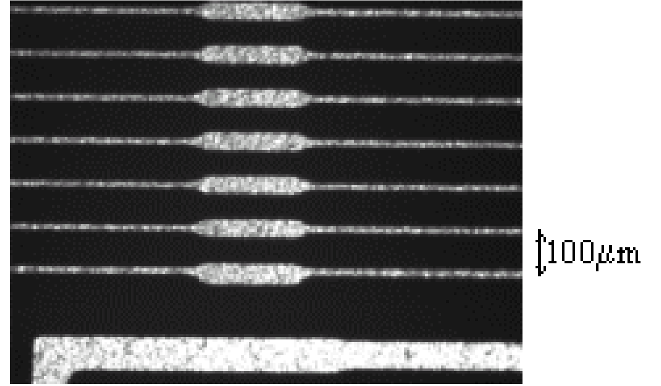


Fig. 2. A view of one of the DYCONEX prototype cables taken with a microscope

II. L0 Layout

L0 consists of two mechanically and electrically independent parts that are concentric to the Tevatron beams, one at positive, the other at negative z (the z-axis pointing along the beam direction with z=0 cm being the center of the CDF interaction region). A schematic view of the L0 layout is shown in Figure 1. L0 is a 12-fold symmetric axial layer. The silicon sensors are single sided with a strip pitch of 25 μm. Alternating strips are read out resulting in an effective pitch of 50 μm. Sensors are 14.85 mm in width and 78.5 mm in length for a total of 256 readout strips. They are made at HPK [4] and are identical to the L00 sensors used in Run IIa. Two sensors are ganged together and read out by one hybrid, housing two SVX4 readout chips. This assembly is called a module. Modules are mounted on a castellated carbon fiber (CF) structure with an aluminum/Kapton shield laminated to it. The CF structure consists of a ~ 0.5 mm CF skin and is built with a precision of $\sim 50\mu$m. Highly thermally conductive and extra stiff CF was used. The structure will be supported by the outer layers' barrel and is therefore independent of the beampipe it is surrounding. Three modules are glued to the CF structure along z for each of the twelve ϕ segments. The cables from lower-z modules run on top of higher-z modules. The length of L0 is twelve sensors plus gaps between modules for a total coverage of approximately 96 cm. In order to assure radiation hardness, the silicon sensors need to be actively cooled. This is achieved by embedded cooling tubes in the CF structure. The tubes run underneath the entire length of the sensors, cooling them to a temperature below -5 degrees C.

A. Fine-pitch Cables

To minimize scattering material in the first measurement layer, the frontend electronics (hybrids and readout chips) and the associated cooling are located just outside of the tracking region ($|z| > 70$ cm) and flare out to slightly larger radii (~ 4 cm) to reduce additional scattering. The hybrids are connected to the sensors via light-weight fine-pitch cables. The longest of the cables is 60 cm long. These cables supply the high voltage and ground to the sensors and send the analog signals from the sensors to the chips.

Two different cable designs were pursued by two different vendors, KEYCOM [5] and DYCONEX [6]. KEYCOM fabricated prototype cables on 50 μm thick Upilex substrate with a trace pitch of 100 μm over most of the length, necking down to 47 μm near both ends for bonding to the sensors and the chips. The achieved trace width is rather wide ($\sim 35\mu$m), which leads to a high cable capacitance. The extremely fine pitch at the end of the cables proved difficult to fabricate. One half of each sensor is bonded to a cable which is bonded to a single chip on the hybrid. At the sensor and the hybrid ends the two cables of one module are side-by-side while in the wide sections (100 μm pitch) they are on top of each other. DYCONEX, on the other hand, produced prototype cables with a 100 μm pitch over the full length. Narrow trace widths were achieved ($\sim 15\mu$m), leading to low capacitance cables (roughly 25 % less than the KEYCOM cables). A zoom-in view of one of the prototype cables is shown in Figure 2. The two cables of one module are in this case overlapped and staggered by 50 μm with respect to each other, giving an effective 50 μm pitch to match that of the chips and the sensors. Consequently, alternating channels are bonded to the top and bottom cables (all odd channels to one cable and all even channels to the other cable). This bonding scheme is mechanically more challenging, but the coarser pitch proved easier to fabricate.

B. Cooling

In order to fully deplete the silicon even after substantial radiation exposure, relatively high bias voltages will be applied to the silicon (up to 500 V). The associated heat has to be dissipated by means of active cooling of the silicon. This is achieved by cooling pipes that are embedded into every other of the twelve ϕ segments of the CF support structure, running throughout the entire length underneath the modules. For inlet and outlet of the coolant, coaxial peek tubes are chosen, with the coolant flowing into the structure (from large z to $z = 0$ cm) through the inner tube and out through the outer one. A simulation of this coaxial cooling concept, assuming a flowrate of 0.07 to 0.1 lpm and a coolant temperature of -15 degrees C,

shows temperature differences between inlet and outlet of only ~ 0.5 degrees C and a maximum temperature of ~ -5 degrees C at the silicon in accordance with the design specifications. In order to reach these low temperatures, a water-glycol mixture is used as the cooling fluid.

III. Prototype Performance

Two prototype modules were built, one with a KEYCOM cable and the other with a pair of DYCONEX cables. Both modules were mounted on a prototype CF structure and installed inside an Aluminum box as a means to protect the setup from external light and noise sources (Figure 3). Between the CF and the silicon modules a ~ 0.5 cm wide Aluminum strip and a ~ 1.5 cm wide Kapton strip were glued. The two modules were mounted such that the cables of the DYCONEX module run on top of the KEYCOM module. The KEYCOM module has only one cable bonded between sensors and readout chip, while the DYCONEX module has two cables that are bonded to the silicon and the two readout chips. In order to study the effect of the capacitive load of the sensors and the cables seperately, some channels on the DYCONEX module were only bonded to the cable plus one sensor, or to the cable only, without any silicon. DYCONEX cables were chosen for the prototyping phase of this detector upgrade due to their high quality, although they require a more challenging bonding scheme. Therefore, only the performance of the DYCONEX module is studied in greater detail here, while the KEYCOM module is only used to evaluate the influence of another module that is read out simultaneously. For all results shown here, the silicon was biased to $V_{bias} =$ 140 V, which corresponds to the depletion voltage of the sensors.

A. Signal-to-Noise Ratio

As a first test the signal-to-noise ratio was measured as a function of the bandwidth setting of the SVX4 chip, that is the time to integrate the charge from the silicon strips, where higher bandwidth (BW) corresponds to shorter integration time, and therefore smaller signals, but also smaller noise. The result is shown in Figure 4 for three different capacitive loads to the input channel of the readout chip: only the cable is bonded to the chip (blue, upper curve), the cable plus one silicon sensor are bonded (magenta, middle curve) and the cable plus both sensors are connected (green, lower curve). The qualitative result is as expected and as seen from the outer layers' measurements, that use the same readout chip [7], the signal-to-noise ratio increases monotonously with bandwidth and decreases with a larger capacitive load. However, despite the long cable length (59.5 cm) a signal-to-noise of about 13 can still be reached, which is found to be sufficient for quality physics data. It may be noted that one ADC count corresponds to about 500 electrons in our system.

B. Noise Pick-up

Of special importance is the study of the noise behaviour of the L0 modules. The long cables could act as an antenna.

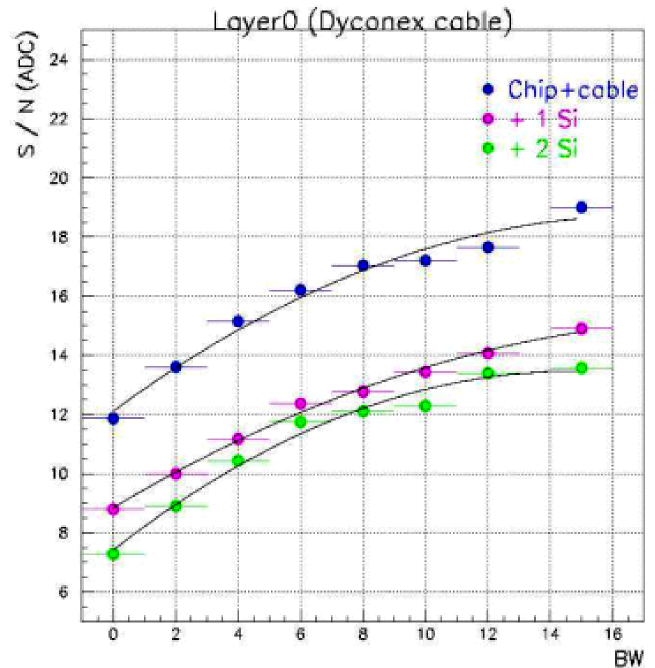


Fig. 4. Signal-to-noise ratio for the DYCONEX module as a function of bandwidth (or charge integration time) for three different capacitive loads

Running on top of adjacent modules, both the silicon as well as the cables, they could pick up environmental noise. As long as this extra noise is uniform across a chip, it can be subtracted at run time by the real time pedestal subtraction (RTPS) feature of the SVX4 chip. In the currently installed Run IIa L00 detector a non-uniform pick-up noise is observed, where higher noise is seen towards the edges of individual chips. The nature of this pick-up noise was studied and will be discussed briefly in the next section. In this section the noise behaviour of the L0 prototypes is presented.

In Figure 5 the noise and differential noise (i.e. common-mode subtracted noise) versus channel number are shown for the DYCONEX module. The difference between the two is a measure of the excess noise in the system. In this case the CF structure was left floating. As expected, non-uniform excess noise can be seen, with larger noise towards the center of the module, where the floating Aluminum strip is located.

Figure 6 shows the same plot where, on the other hand, the CF is grounded, via the Aluminum strip, to both the Aluminum box and the analog ground on the hybrid of the DYCONEX module. The amount of excess noise is largely reduced and is nearly uniform across the module.

Figure 7 shows a plot with the same configuration as in Figure 6 but with the RTPS feature activated. The excess noise is reduced (especially for the second chip, channels 128 to 255) but there is still small excess noise visible towards the edges of the first chip (channels 0 to 127). The amount of this noise is small and tolerable.

In addition to these grounding studies we also varied the position of the cables inside the Aluminum box and the separation between the two cables, and tried different shielding options for the assembly. By varying all these parameters, we

Fig. 3. Picture of the prototype test setup: two modules mounted on a CF structure

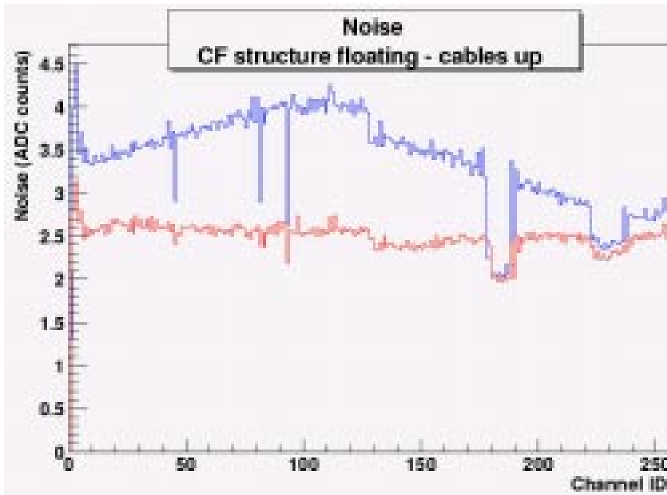


Fig. 5. Noise (blue, upper curve) and differential noise (red, lower curve) are shown versus channel number; the CF structure is floating

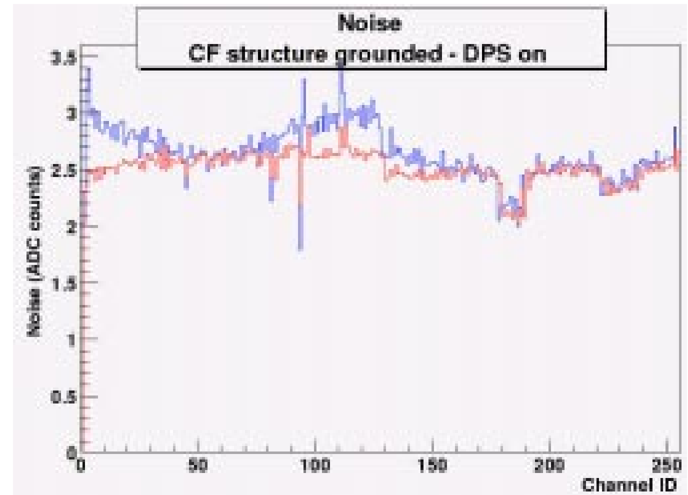


Fig. 7. Noise (blue, upper curve) and differential noise (red, lower curve) are shown versus channel number; the CF structure is well grounded and RTPS is activated

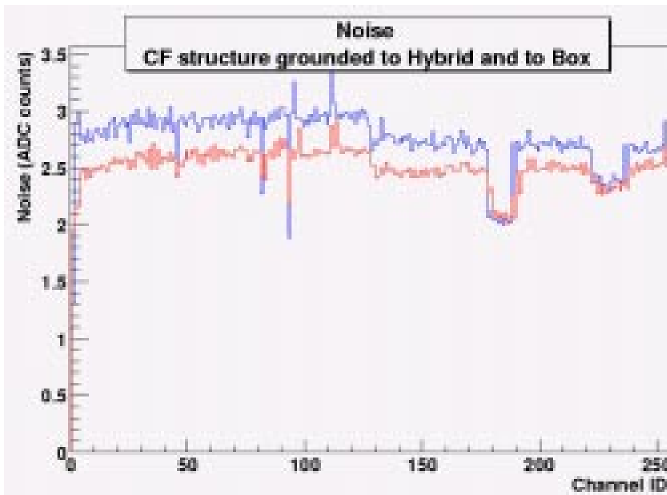


Fig. 6. Noise (blue, upper curve) and differential noise (red, lower curve) are shown versus channel number; the CF structure is well grounded

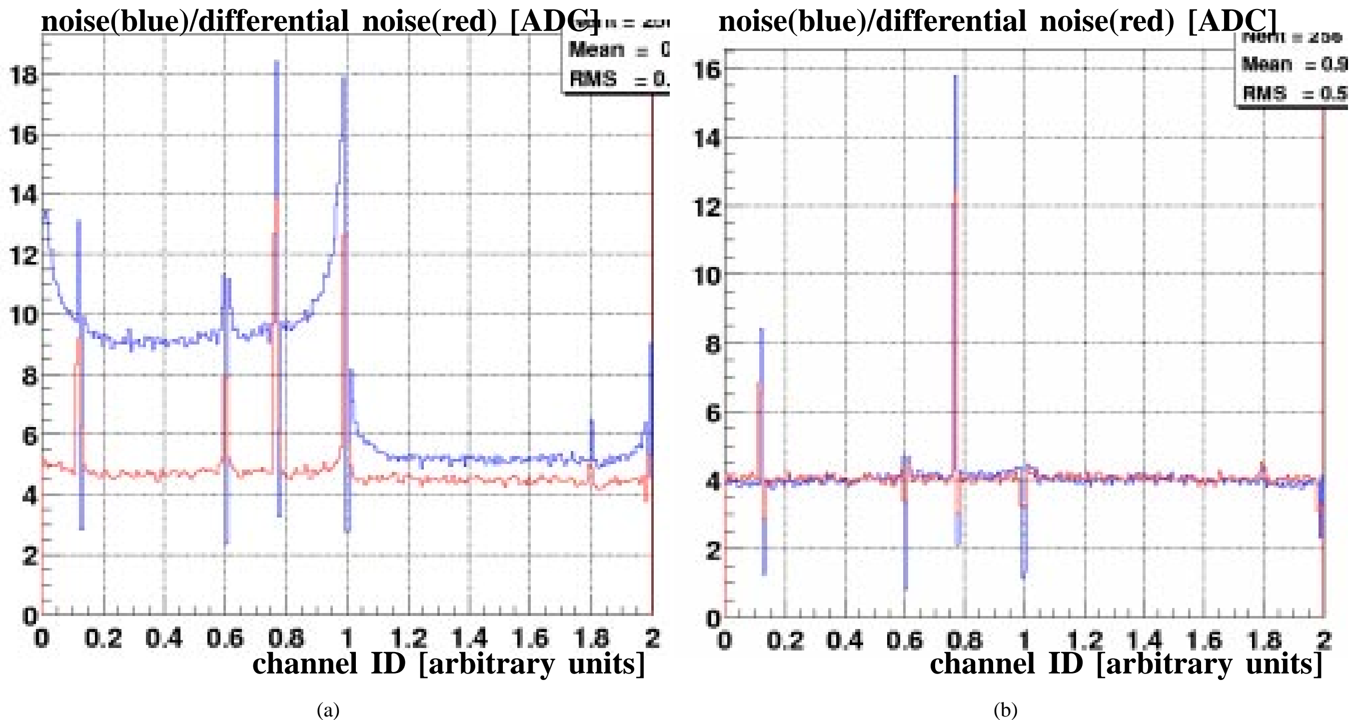
see different values and shapes of excess noise. Therefore, special care needs to be taken when dressing the final device. The state of the KEYCOM module, whether it was powered up and reading out or not during data taking of the DYCONEX module, did not have any effect on the performance of the DYCONEX module itself, nor on the value and shape of the excess noise in any of the configurations we tested.

IV. Comparison with L00 Studies

In the currently installed Run IIa L00 detector [8] a non-uniform pick-up noise is observed, where higher noise is seen towards the edges of individual chips. For this reason all channels of this layer have to be read out as opposed to the sparsification that is used for the outer layers. This leads to a large data volume and a long readout time. Furthermore, L00 can not currently be included in the second level silicon trigger that finds displaced tracks. This non-uniform noise is subtracted offline by fitting Chebychev polynomials to the raw data of every single chip in every event, thus making L00 data available for offline analyses. The nature and origin of this pick-up noise was studied with a spare module on the bench.

In Figure 8(a) the noise and differential noise are shown versus channel number for this L00 test module. The non-uniform excess noise, that can be seen especially on the first chip (channel ID's 0 to 1) and on the second, was induced by placing a wire underneath sensors, cables and the hybrid. The wire was connected to a waveform generator. As a comparison, data from the same module are shown in Figure 8(b), but shielded from the wire by an Aluminum foil. In this case no difference between noise and differential noise is observed and therefore no common-mode noise is present.

The dependence of the noise on the frequency of the injected signal from the waveform generator was studied. Between 0 and 500 kHz no large noise contributions were observed, but between 1 and 2.5 MHz a significant increase in excess noise was seen, while no extra noise was seen when going to even



(a) (b)

Fig. 8. Noise (blue, upper curve) and differential noise (red, lower curve) are shown versus channel number (a) without, and (b) with a shield; a wire was introduced as an external noise source

higher frequencies (up to 2.4 MHz). However, the shape of the noise was the same for all frequencies. The frequency used in Figure 8 was 2.4 MHz. Finally, moving the wire from below the module to the top, the behaviour of the two chips flips, i.e. the second chip shows a higher noise.

V. Conclusion

First prototypes of the innermost layer of the CDF Run IIb silicon upgrade were tested on a prototype carbon fiber structure. The achieved signal-to-noise values look good and comparable to the outer layers' results. A study of non-uniform noise as well as grounding and shielding issues was performed. The results were similar to those from a previous study using a Run IIa L00 module. From these tests we conclude that the new innermost layer of CDF will work as designed in the CDF environment, provided special care for grounding and shielding of the device, both internally and externally, is taken. We are currently building more prototype modules of L0 that will be mounted on another carbon fiber structure. Tests of this more complex assembly are still needed in order to draw final conclusions.

Acknowledgment

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