

# A control and monitor system for serial powering of silicon strip detectors at SLHC

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**Abstract**– A serial powering scheme is a promising solution to reduce the total power, number of cables, passive detector material and overall the cost for large-scale silicon tracking detectors. We present a control and monitor system for a serial powering scheme where the low-voltage lines of detector modules are chained in series and the power is supplied by a single current source. The voltage for each module is regulated using a local shunt regulator. We propose to implement MOS FETs to monitor and control to optimize the current passing through the shunt regulator. They also function as a bypass in case where the module in a chain needs to be excluded.

## I. INTRODUCTION

A serial powering scheme is considered as a solution to reduce the total power dissipation, number of cables, passive detector material and the overall cost for large-scale silicon tracking detectors, such as a silicon semiconductor tracker (SCT [1]) at the super-LHC (SLHC). In such a scheme, the low voltage lines of multiple modules are chained in series and the power is supplied by a single current source. The voltage for individual module is provided by a local shunt regulator. Intensive studies are being carried out, with emphasis on noise performance [2,3]. The modules are operational by serial powering with no indication of any extra noise increase in comparison by conventional independent powering.

We present a control and monitor system for a serial powering scheme, where low power operation is aimed at, thus reducing the heat generation. The power supply current is tuned to minimize the current passing through the shunt regulators by monitoring the shunt current. We propose to introduce MOS FETs for this purpose. They can also serve a flexible configuration for module calibration to increase the necessary current. They can function to bypass the current in the case where the modules in a chain become un-operational.

## II. SERIAL POWERING

A serial powering we consider is shown schematically in Fig. 1. N modules are chained in series where a single current source is used for providing the power. The individual module voltage is regulated using a local shunt regulator.

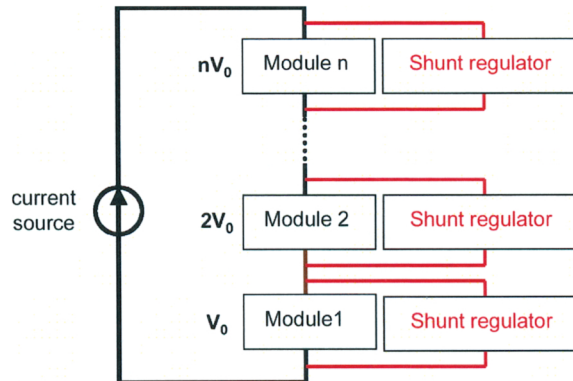


Fig. 1. Schematic diagram of serial powering.

Fig. 2 shows a simplified diagram of the module voltage, current, and shunt current, current passing through the shunt regulator, as a function of the source current. The blue dashed line indicates the critical operating point, below which the module voltage, for example, is not stabilized and DAQ communication error occurs. Above the orange dashed line region, the shunt regulators waste the power, generating excessive heat. Keeping the source current at the middle, e.g. on the green dashed line ensures a stable operation at a minimum power consumption. In the actual systems, the optimized operation should be dependent on the processing frequency (for example on the particle occupancy). We therefore propose to implement a monitoring system of the shut current to realize the optimum operation.

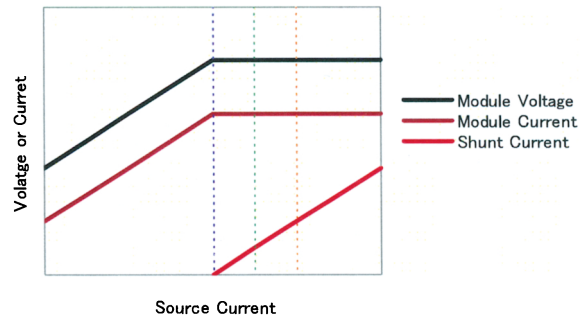


Fig. 2. Source current dependence of module and shunt current.

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We have manufactured a test board to evaluate the functionality of the proposed system.

#### A. Shunt Regulator

A circuit diagram of the shunt regulator is shown in Fig. 3. It consists of a programmable shunt regulator IC (TL431A) and a PMOS FET (2SJ494) as a current booster.

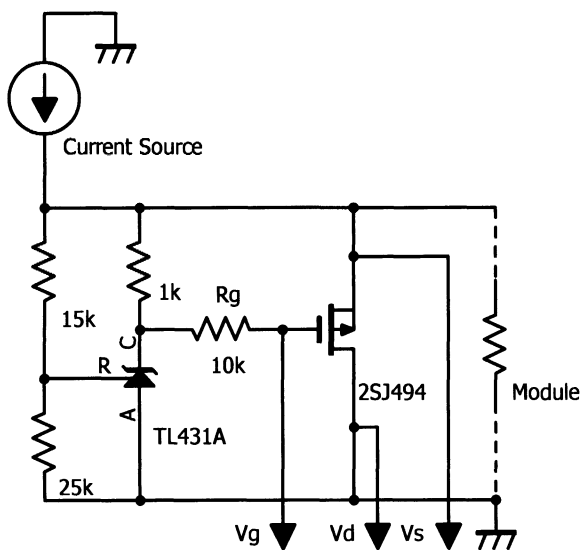


Fig. 3. Shunt regulator circuit. The voltages at three lines with arrow are monitored.

#### B. Shunt Current Monitor

Since the most of the current passing through the circuit is a contribution from the current booster FET (2SJ494), the measurement of the drain current of the FET is sufficient for the shunt current monitoring. The drain current of the FET could be obtained from measuring the gate ( $V_g$ ), drain ( $V_d$ ) and source ( $V_s$ ) voltages, using a lookup table which was measured beforehand. The voltage difference between the drain and source corresponds to the module voltage. The module voltage and the shunt current can be measured in general using three wires per module (as shown in Fig. 3). In this system, the voltage between the  $i$ -th drain and  $(i-1)$ -th source can be estimated, since there are only pure Ohmic components. We reduce the number of monitoring wires from  $3n$  to  $2n+1$  for  $n$  modules.

#### C. Bypass Scheme

In the serial powering system, the influence of stuck modules needs to be resolved. Fig. 4 shows a simplified diagram for such a case as a function of module conductance. We assume that modules work normally between the blue and the green lines. Below the blue line, modules are in “open failure mode”, where the shunt regulator could manage the voltage but wasting the power a lot. On the other hand, above the green line, modules are in “short failure mode”, where the regulator can provide the module voltage ( $=V_0$ ) less than

required. The module voltage will not exceed  $V_0$  in both cases. Therefore, the system can deliver the power to other modules, even if stuck modules exist in the chain, as far as the system is allowed to deliver large enough current.

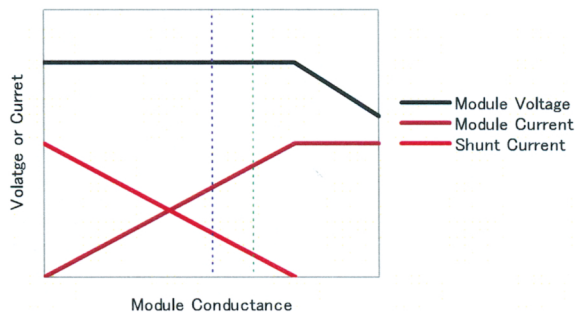


Fig. 4. Module conductance dependence of module and shunt current.

A scheme of bypassing stuck modules, shown in Fig. 5, is efficient in reducing the un-necessary power consumption. The switches are the PMOS FETs introduced as current boosters, shown in Fig. 3. The bypassing was achieved by keeping the gate voltage  $V_g$  minus against the drain voltage. In this condition the PMOS FET works as a low  $R_{on}$  switch. The gate resistance  $R_g$  works as a current limiter in bypassing operation.

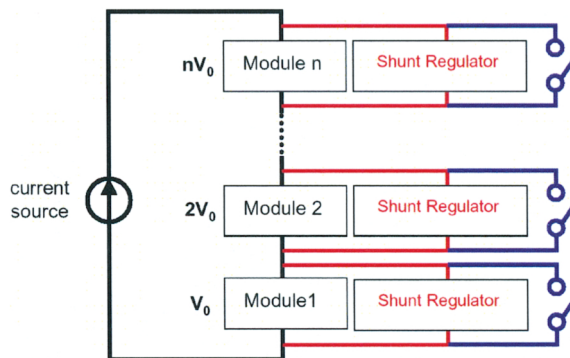


Fig. 5. Schematic diagram of bypass scheme for serial powering.

#### D. AC Coupling

In the serial powering, the ground levels are different in the modules in chain. AC coupled LVDS are used for communication in order to isolate the module grounds from the general ground of the DAQ system. Fig. 6 shows a circuit diagram of AC coupled LVDS signaling for data and clock/command communications.

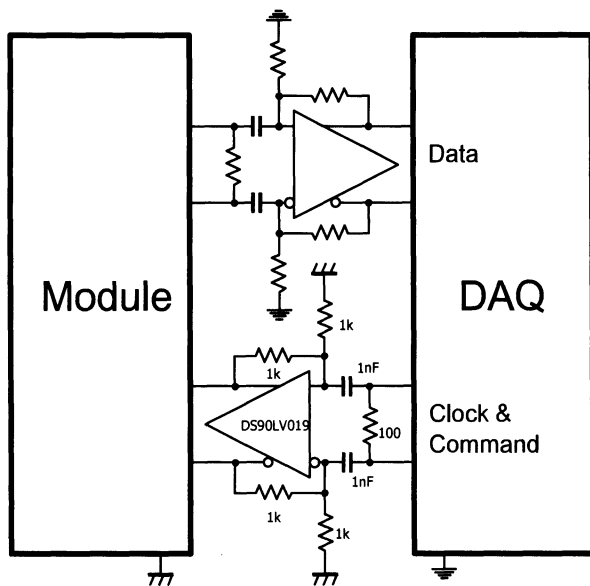


Fig. 6. AC coupled LVDS circuit.

### III. ENC MEASUREMENTS

The noise performance with the proposed system is evaluated using ATLAS SCT modules [1]. Fig. 7 shows an SCT module (green box) and a serial powering PC board (red box). Each SCT module is equipped with 12 readout front-end chips, each with 128 readout channels. The silicon microstrip electrode, 12 cm long, is AC coupled to the amplifier. The equivalent noise charge (ENC) measured in the SCT system using the standard SCTLV module was about 1,500e.

The SCT module requires an analog (+3.5V) and a digital (+4V) power. In the proposed system, the digital power is regulated by the shunt regulator directly and the analog power is doubly regulated through a low voltage drop voltage regulator (TPS7101). Ambient temperature of modules and shunt regulators was kept at 15°C. Temperature of readout hybrids was about 32°C, which was measured by thermistors attached on the hybrids. High voltages to the sensors, served by four isolated high voltage power supplies, were fixed to 200V.

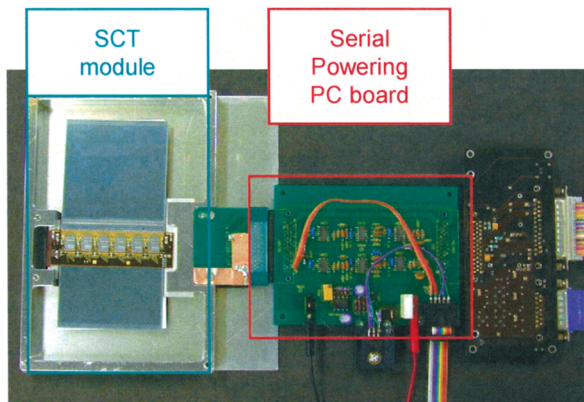


Fig. 7. SCT module connected to serial powering PC board.

#### A. Source Current Dependence

Fig. 8 compares the chip averaged ENC values in the serial powering (SP) and the conventional individual powering (IP). In this measurement single module was operated. The current in the individual powering scheme was about 1.5 A. In the serial powering scheme, we measured ENC data with changing the source current. The ENC was observed to change by a few percent during the measurement period of several hours, due to accumulation of surface charge on the SCT sensor. We evaluated this effect as the difference in two ENC measurements at  $I = 1.6$  A. No significant difference was found between the two powering schemes. Note that the preamp gain was about 5% lower at  $I = 1.4$  A, reaching the critical point, and communication error occurred below  $I = 1.3$  A.

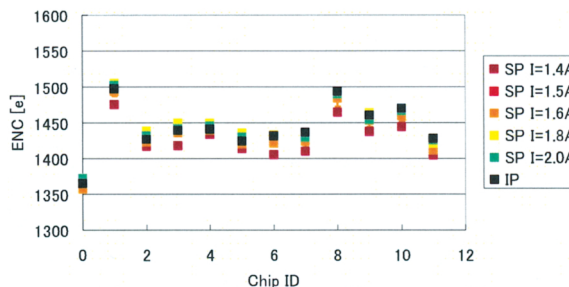


Fig. 8. ENC values for different source current values in the serial powering (SP) in comparison with individual powering (IP).

An example of shut current monitoring is shown in Fig. 9 where  $V_{sg}$  is measured as a function of the power supply current. Also plotted is the shut current, which was measured beforehand as a function of  $V_{sg}$ . The optimum power supply current of 1.6 A is located above the threshold in terms of the shunt current. In the monitoring scheme, we propose to measure  $V_{sg}$  and feedback to the power supply to keep the shunt current at the optimum.

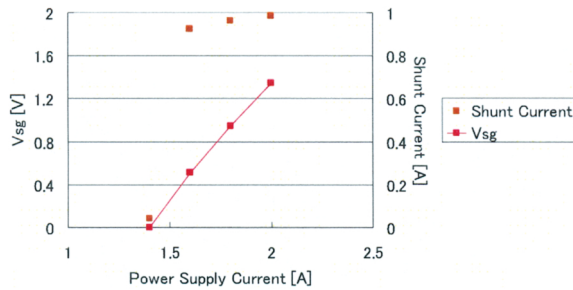


Fig. 9. Shunt current Monitoring.

### B. Dependence on the Module Location

Fig. 10 shows the ENC data in the serial powering scheme where four SCT modules (SP1-4) were operated at a power supply current of 1.6A. To eliminate the individual module dependence, we measured the ENC for a same module, replacing it at different positions in the serial powering configuration. In the “SP1” configuration, the target module was placed nearest to the current source supply ground. In the “SP4” configuration, the module was operated with the highest voltage levels. No significant difference was found in these configurations.

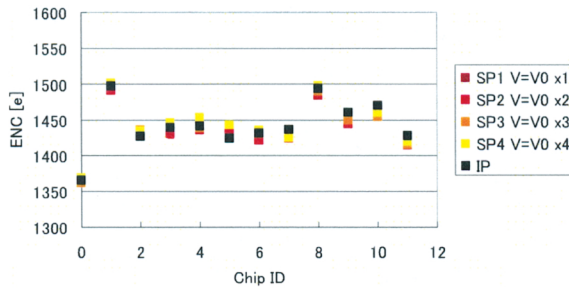


Fig. 10. ENC values shown for four module positions in the SP.

### C. Dependence on Bypassed Modules

The ENC data were taken in configurations where one or two modules were bypassed. The ENC results are shown in Fig.11. The module to be measured was set in the “SP2” configuration. “Bypass M1” means that the module with the lowest voltage levels was bypassed. “Bypass M1 & M4” means that both modules at the lowest and highest voltage levels were bypassed. No significant difference was found between the six bypass configurations we tested. The voltage between the drain and source of the PMOS FET which was bypassed was found to be about 50 mV at a  $-20V$  gate voltage.

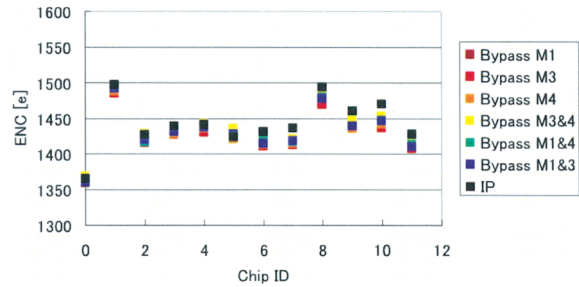


Fig. 11. ENC values of the module at SP2 for different configurations where one or two modules were bypassed.

## IV. EFFECTS OF PIN HOLE FAILURE

A couple of hybrids will be installed in an SCT short strip module for the SLHC application. A serial powering operation may be applied among these hybrids, providing different ground potentials in one module. This will not cause any problem as far as the AC coupling is preserved between the amplifier and the strip. However, pinholes in the oxide layer cannot be excluded completely, tying the corresponding strips to their local grounds. We investigated the influence of such channels tied to the DC offset in the serial powering environment. Fig. 12 shows an equivalent circuit diagram for a readout channel DC or AC coupled. The left side corresponds to the sensor and the right a simplified bipolar preamp part. An external voltage of  $V_{ex}$  simulates the DC offset between the sensor and preamp grounds. The current from  $V_{ex}$  was limited by  $R_{bias}$ , such as  $I_{ex} = V_{ex} / R_{bias}$ .

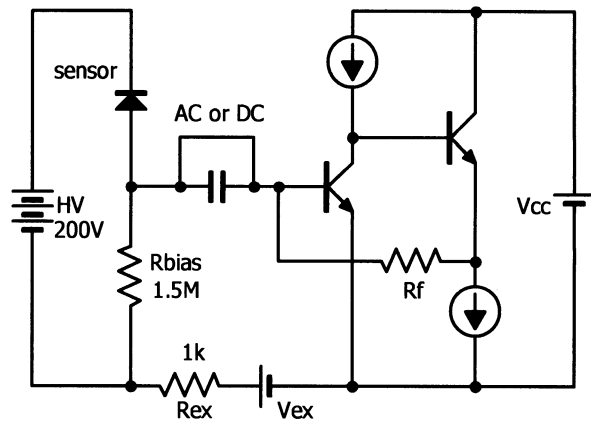


Fig. 12. Equivalent circuit for DC or AC coupled readout channel in serial powering at the ground level  $V_{ex}$ .

### A. Effects of DC Coupled Strip

Fig. 13 shows the ENC data for a simulated DC coupled strip with changing the DC offset  $V_{ex}$ . The results for AC coupling case for the same strip are also plotted for

comparison. Typical uncertainty size is attached to the AC coupled data, which was derived from repeated ENC measurements. The plotted ENC data are the same within uncertainty. The data could not be obtained for  $V_{ex} < -1$  V or  $V_{ex} > 4$  V due to fitting errors in the ENC calculation. In fact the bipolar transistor at the first preamp stage could not set the bias in working region. In  $V_{ex} < -1$  V, the base-emitter voltage of transistor could not activate the transistor. In  $V_{ex} > 4$  V, or  $I_{ex} > 3$   $\mu$ A, the base current of the transistor exceeded a normal base current of about 3  $\mu$ A. The results conclude that the strips DC coupled to the local ground at higher level will not function properly.

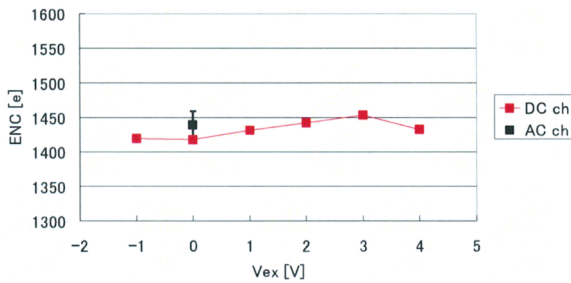


Fig. 13. ENC values for AC or DC coupled strip, which is tied to the potential of  $V_{ex}$ .

### B. Influence to Neighbor Strip

Fig. 14 shows the ENC data for the strips neighboring to the DC coupled strip. The DC offset  $V_{ex}$  was varied. The location of the DC coupled strip is at Ch.0. The neighboring strips did not show significant increase for the DC offsets between  $-25$  V and  $25$  V. For the larger offset, several strips at neighbor showed increased ENC values but the other strips are not influenced.

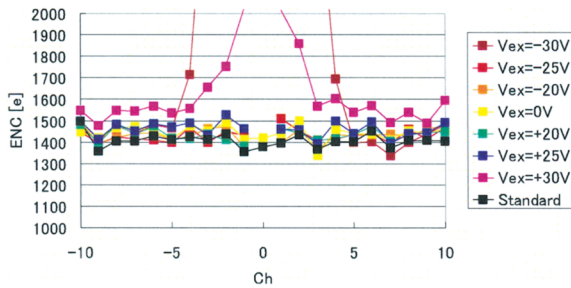


Fig. 14. ENC values around the DC coupled strip, of which the local ground was varied by  $V_{ex}$ .

## V. SUMMARY

A control and monitor system is presented which can minimize the power consumption in a serial powering system

by measuring the shunt current of the regulator. We detailed the method of monitoring the shunt current and effectiveness of a bypass scheme for stuck modules. In a test system with serial powering, the SCT modules were operated stably without introducing any extra noise. We found small dependence of the noise level on the source current, ground voltage levels, number and locations of bypassed modules. The noise is degraded on and around the DC coupled strips if a higher ground voltage is applied to the DC coupled strip. The influence is, however, limited and in most configurations the degradation is not significant.

## REFERENCES

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- [2] D.B. Ta, et al., Nucl. Instr. and Meth. A 557 (2006) 445.
- [3] M. Weber, et al., Nucl. Instr. and Meth. A 579 (2007) 844.