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Construction and performance of the ATLAS silicon microstrip barrel modules

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ATLAS SCT Barrel Module Collaboration

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Abstract

The ATLAS Semiconductor Tracker (SCT) consists of four barrel cylinders and 18 end-cap disks. This paper describes the SCT modules of the barrel region, of which more than 2000 are about to be constructed. The module design is fixed. Its design concept is given together with the electrical, thermal and mechanical specifications. The pre-series production of the barrel modules is underway using mass-production procedures and jigs. The pre-series modules have given satisfactory performances on noise, noise occupancy, electrical as well as mechanical and thermal properties. In addition, irradiated modules were demonstrated to work successfully. Also first results from a 10-module system test are given.

1. Introduction

ATLAS is a multi-purpose detector designed for the new physics in the TeV mass range, especially for the search of the Higgs and SUSY particles at LHC [1]. Three sets of large aperture superconducting toroids generate toroidal magnetic field for the muon chambers. Inside the muon system, there are scintillation-tile hadron calorimeters, LAr electromagnetic calorimeters and Inner Detectors (ID) [2]. A central solenoid generates magnetic field of 2 T in the ID volume. From inside to out, the ID consists of the pixel detector, the Semiconductor Tracker (called SCT) of silicon microstrip sensors, and the straw transition radiation tracker. Its overall dimension is 2.3 m in diameter and 7 m in length. Its main requirement is the precision tracking of charged particles using ionising detection devices that are capable of 40 MHz bunch crossing identification and that can tolerate large radiation doses with minimal possible material.

The SCT [3] covers the region from 300 to 520 mm in radius from the beam line. It is divided into the barrel part of 4 cylindrical layers in the central region and the forward part of nine disks in each side. Total area of the silicon microstrip sensors is 61 m^2. The $r\phi$ position resolution per SCT layer is aimed to be around 17 μm, covering a rapidity range of ± 2.5.

When LHC operate at its design luminosity of $10^{34} cm^{-2} s^{-1}$, the annual fluence at the inner-most sensors at $r = 30$ cm is about $1.8 \times 10^{13} n_{eq}/cm^2$ expressed in terms of equivalent 1 MeV neutron flux. Thus 10-year operation at LHC requires the radiation tolerance up to $2 \times 10^{14} n/cm^2$ in 10 years including 50% uncertainty.

ATLAS decided to use the p-in-n type of silicon microstrip sensors for its radiation tolerance and cost. The temperature of the sensors is kept below 0°C, preferentially at around −7°C all year around including non-operation time to suppress the anti-annealing while keeping beneficial annealing of radiation induced effective doping. Low-temperature operation also helps in reducing bulk leakage current.

2. Design of the barrel module

In the barrel SCT system, exactly the same modules are used for all 4 cylindrical layers. The module is a basic detector unit carrying stand-alone mechanical rigidity together with electrical as well as thermal functionalities. It consists of four single-sided p-in-n silicon sensors and a hybrid for readout. The required tracking precision is obtained by modules with an intrinsic point resolution of 23 μm in the $r\phi$ coordinate per single side measurement. The precision is obtained for the binary readout scheme (on-off readout) using silicon microstrip sensors with 80 μm readout pitch. Two sensors on one side of the module are connected together strip-by-strip to form an effective strip length of 126 mm. These strips are aligned at a ± 20 mr half-stereo angle with respect to the module axis. Adjacent modules are overlapped longitudinally each end, requiring that they are staggered in radius by 2.8 mm to leave a 1 mm stay clear between sensors. A tilt angle of 10° allows adjacent rows of modules to be overlapped, providing hermetic detector coverage.

The barrel modules are mounted on four concentric carbon-fibre cylinders through attachment

to CFRP brackets that are located by precision inserts in the cylinders. The mean radii of the barrel modules are 300, 370, 450 and 525 mm.

The mechanical tolerance for positioning sensors within the back-to-back pair must be $\sim 5\,\mu m$ lateral to the strip direction. In this way, the fine alignment for tracking can be handled at the module as one solid object.

Another important property of the module is a thermal function. The 12 ASICs dissipate a power of 6 W for nominal operating conditions and nominal process parameters, up to a maximum of 8.1 W for the worst case combination of process parameters, supply voltages and radiation effects in electronics. As the dose accumulates, the heat generation in the sensor bulk become appreciable due to leakage current. The maximum heat generation q_{max} per unit area of the sensor is estimated by multiplying the maximum designed applied bias V_{max} of 500 V and the leakage current deduced from the current related damage constant α of 4×10^{-17} A/cm at 20°C as

$$q_{max} = \alpha \cdot 2 \times 10^{14}/\mathrm{cm} \cdot F_T \cdot V_{max} \cdot 285\,\mu m = 120\,\mu W/cm^2$$

(normalized at 0°C) in which F_T is the reduction factor of $\sim 1/1000$ in leakage current at 0°C with respect to 20°C and 285 μm is the sensor thickness. If all 4 sensors are at 0°C, total bulk heat is 1.8 W. Since the bulk leakage current grows non-linearly with sensor temperature (approximately it doubles every 7°C), so called thermal runaway may occur if the cooling is not adequate [4]. Including a safety factor, the goal for thermal runaway point is set at $240\,\mu W/cm^2$ (at 0°C). The effective in-plane thermal conductivity must be increased beyond that of silicon. In practice this is achieved by the use of high-thermal conductivity material thermalized pyrolytic graphite, referred to as VHCPG (very high-thermal conductivity pyrolytic graphite) or TPG, in a baseboard which is laminated as part of the detector sandwich.

After considering the combined electrical, thermal and mechanical requirements, the optimized design of the barrel modules has a hybrid placed near the centre of the module, above and below the sensors, and connected to the strips near the middle of their total length, as shown in Fig. 1. This configuration minimizes the space conflict with neighbouring modules. The central signal tapping is better electronically as it results in minimum spread resistance of metal readout strips seen by the front-end circuits. A piar of 128 mm long units is back-to-back aligned with a stereo angle of 40 mrad and glued together with a baseboard in between. Two hybrid circuits with a flexible wrap-around connection in between make

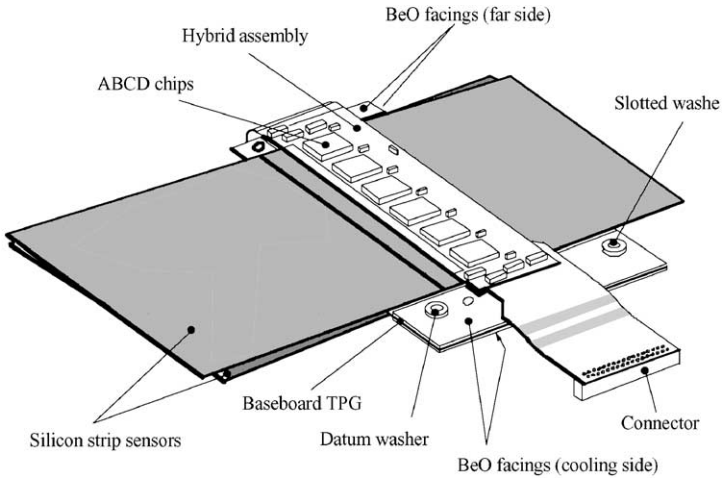

Fig. 1. 3D view of the ATLAS barrel SCT module.

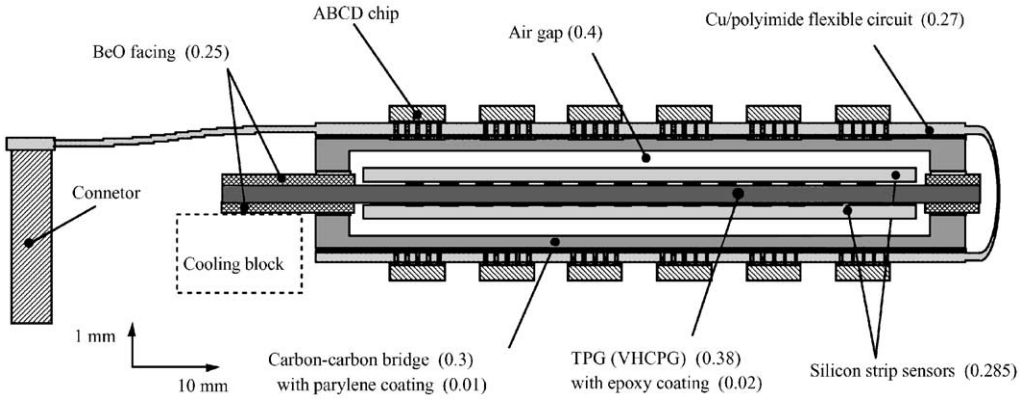

Fig. 2. Cross-section of the module at the location of the hybrid. Note that the vertical direction is magnified by 5. The numerals are thicknesses in unit of mm.

a single-piece construction of the hybrid possible using Cu/polyimide laminates. The baseboard extends outwards, with BeO facings epoxy-fused to the VHCPG surfaces, on both lateral sides of the module. These facings are the places at which the readout hybrids are attached. Each module is fastened by 2 points at the longer facings onto a supporting CFRP bracket and by a third mounting point situated at the shorter facing onto the adjacent bracket. The module mounting accuracy is achieved by precision set screws locating on the internal bore of a circular and a slotted hole on the longer facing of the baseboard.

Fig. 2 shows the cross-section of the module with magnification in vertical direction. It is noted that the hybrid 'bridges over' the sensors with an air gap of 0.4 mm. Thus the sensor surfaces are intact except bonding wires. This has the advantage of avoiding gluing to the active sensor surface, which would carry the potential for damage and uncertainties associated with long-term ageing and radiation effects. The hybrid bridge must be strong enough to make the supersonic wedge wire-bonding possible. In this configuration, the thermal path for the ASIC heat is largely decoupled from the path of the bulk heat, keeping the sensors as cold as possible.

The cooling of the modules is provided by a thermal contact over an area of 420 mm^2 between the lower BeO facing of the module and an aluminium-cooling block. Two spring clips compress two pieces together. The grease for thermal contact is Dow Corning 340 which has demonstrated both good thermal conduction and high radiation tolerance [5]. The cooling block encapsulates a CuNi cooling tube which carries the evaporative fluid of C_3F_8. The module and the cooling block are electrically isolated in the baseline but an option is kept open for grounding connection.

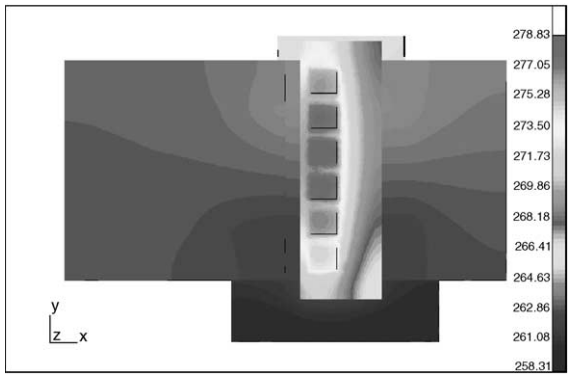

Fig. 3. Thermal profile of the barrel SCT module with a ASIC power of 6 W.

A thermal FEA simulation has been carried out as shown in Fig. 3 for an ASICs power of 6 W and nominal heat generation in the sensors. The profile indicates that the hybrid and sensors are fairly well decoupled thermally. Fig. 4 shows the temperature

of the furthest sensor corner as a function of the bulk heat generation, at three coolant temperatures. The simulation shows that the thermal runaway occurs at 220 μW/mm^2 at coolant temperature of −14°C satisfying nearly the required factor of 2 from runaway point.

The major module parameters are summarized in Table 1. The overall weight of the module is 25 g and the radiation length averaged over the silicon sensor area is 1.17%X_0.

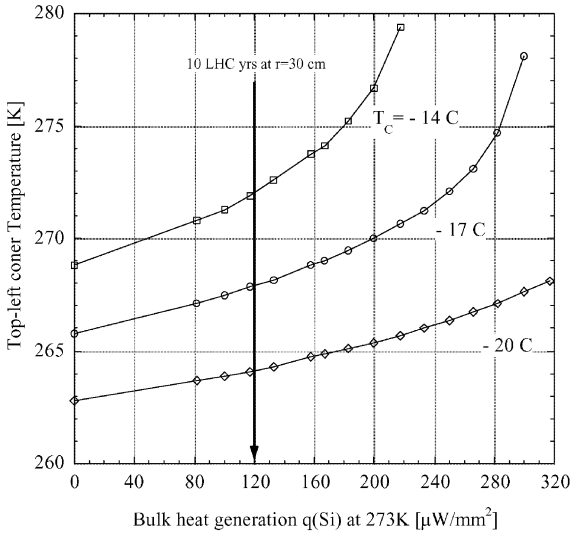

Fig. 4. Temperature of the furthest sensor corner as a function of heat flux with three coolant temperatures T_c for the case of ASIC power at 8.1 W.

Table 1
Major parameters of the module

Number of sensors	2 in top, 2 in bottom
Number of ASIC chips	6 in top, 6 in bottom
Sensor directions	±20 mrad
Sensor operating temperature	<0°C, optimum −7°C
Hybrid power consumption	6 W nom., 8.1 W max.
Thermal runaway heat flux	>240 μW/mm^2 at 0°C
Module thickness (sensor part)	1.15 mm
Module thickness (hybrid part)	3.28 mm
Mechanical accuracy	
Back-to-back in-plane lateral	<5 μm
Back-to-back in-plane longitudinal	<10 μm
Back-to-back out-of-plane	<50 μm
Fixation point, in-plane	<30 μm
Radiation length/module	1.17%X_0

3. Module components

3.1. Silicon microstrip sensors

The silicon barrel sensor is made of four 63.96 mm × 63.56 mm (cut-edge to cut-edge) single-sided p–n junction detectors with capacitively coupled readout strips [6]. Two sensors are aligned to form a 128 mm long unit. Strips of the two sensors are wire-bonded to form 126 mm long strips. The pitch of the strips is 80 μm and there are 770 strips physically with the first and the last being connected to the strip bias potential for the electric field shaping and defining the strip boundary. Table 2 summarizes the major parameters of the barrel SCT sensor. The detail description and quality assurance of the sensors are given in separate paper [7]. The sensor bows at the level of 60 and 80 μm, intrinsically limiting the overall module flatness. Sensitive region to cut edge distance is 1 mm.

3.2. Readout ASICs

The main parameters of the readout ASICs, ABCD3TA, are shown in Table 3 [8]. The analogue part uses the bipolar technology, while the digital part is made by CMOS. The front-end circuit is optimized for 128 mm long strip sensors. Any pulses exceeding the threshold of typically 1 fC are stored as 1-digit hits for three consecutive clock buckets. No analogue information is kept. In

Table 2
Main specifications of the sensors

Type	p^+-n-n^+ single sided
Thickness	285 ± 15 μm
Lenght × width	63,960 ± 25 μm × 63,560 ± 25 μm
p implant pitch/width	80 μm/16–20 μm
Initial full depletion	<150 V
Total initial leakage at RT	<6 μA(150 V), <20 μA (350 V)
Good readout strips	>99%
Post-irradiation characteristics with 3×10^{14} p/cm^2	
Voltage for >90% CCE	<350 V
Interstrip capacitance	<1.5 pF/cm at 350 V, 100 kHz
Total leakage current	<250 μA at −18°C up to 450 V
Micro-discharge	<5% increase for 300–400 V
Good strips	>99% at 350 V

Table 3
Major parameters of the ABCD3T-A chip

Type of circuit	Binary readout
Gain	50 mV/fC
Peaking time	20 ns
No. of input channels	128 ch/chip
Equivalent noise charge	1500 e (un-irradiated) 1800 e (irradiated)
Threshold tuning	Individual 4-bit trimDAC with 4 selectable ranges
Timewalk at 1 fC threshold	<16 ns for 1.25–10 fC
Readout redundancies	By skipping a bid chip
Process technology	0.8 μm BiCMOS (DMILL)

this type of binary readout, the uniformity of thresholds is a critical parameter. The threshold is adjusted by a 4-bit trim DAC (TrimDAC) attached to each channel. In addition, 4 selectable ranges in the TrimDAC, 60, 120, 180 and 240 mV, are implemented to cover the increased spread of the threshold offsets (of about a factor of 3) caused by radiation. A hit can be generated by an internal calibration pulse. Every fourth channel is pulsed simultaneously with variable amplitude of 0–10 fC. The calibration strobe time can be delayed with respect to the clock phase.

The module has 6-ABCD chips on each side forming a readout unit. The left-most chip is the master chip connected to a fibre–optic interface. Upon the receipt of a level-1 trigger, the master chip initiates a readout sequence from left to right. In the event of the failure of one of the slave chips, the chips can be programmed to route around the failed chip. In the event of the failure of one of the master chips, the other working master can control and readout 10 slaves chips by routing around the failed master chip.

Wafers of the ASICs from the foundry need to be fully tested before dicing. The acceptance limits for various parameters are defined with sufficient margins allowing for chip degradation after full irradiation. All chips are put through the full configuration tests as well as measurements of power consumptions, gains, offsets, noises, thresholds, trimDAC settings and ranges. The wafers screening data are also used to monitor the production yield by comparison against the foundry data. The chip parameters extracted from the wafer screening are transferred to the database via a java application.

3.3. VHCPG baseboards

The baseboard substrate is thermalized pyrolytic graphite VHCPG. Its thermal conductivity at room temperature is 1450–1850 W/mK in-plane with 0.4%/C and typically 6 W/mK out of plane. Its thickness is 380 ± 15 μm. The VHCPG material, however, is intrinsically friable and easily delaminated. An epoxy encapsulation technique was developed to make up for such weaknesses for this project. Four BeO facings are attached to the VHCPG sheet. They have precision holes and Gold HV contact pads. A picture of an assembled baseboard is given in Fig. 5. The shape of the baseboard is a result of material minimization.

The baseboard fabrication is being carried out at CERN. After laser cutting to the shape specified, a fine matrix of 120 μm diameter holes is made in the substrate as an integral feature of the encapsulation. The positioning of the four BeO facing plates is provided by a set of precision jigs with the appropriate quantity of epoxy being

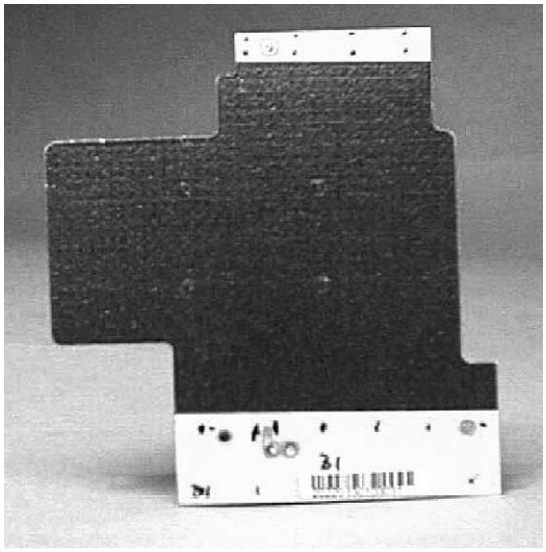

Fig. 5. Encapsulated VHCPG baseboard with BeO facing plates.

applied by screen printing to each side of the substrate board. The assembly is cured under an appropriate temperature cycle, pressure and surrounding vaccuum to achieve a bubble-free epoxy coating and graphite–BeO intra-surface junctions. The encapsulation is typically 20 μm thick. Four small spots of epoxy are removed from each side to provide openings for electrical connection to be made to the rear side of the silicon sensors using conducting epoxy. This complements drilled and filled holes in the upper BeO cooling facing for gold HV contact pads.

Each baseboard is subject to a quality assurance of thermal and electrical properties. Injecting known heat at defined points around with a heat sink attached to the lower cooling facing, a temperature contour is taken with an intra-red thermal imaging camera. The contour for each board is stored in a database to compare with standard images and FEA simulations.

3.4. Cu/polyimide flexible circuits

The technology of flexible multiplayer circuits of Cu/polyimide are now commercially used [9]. The layer structure of the Cu/PI circuit is listed in Table 4. The starting core for build-up is a double-sided Cu/PI sheet in the middle. A single-sided Cu/PI sheet is glued on each side of the core sheet. In the wrap-around section the top and bottom copper layers are removed. Electrical connections among different layers are realized by either through-holes, penetrating all layers, or laser-cut via-holes between two adjacent layers. The top L1 and bottom L4 layers have extra copper for plating these through-holes and via-holes. All Cu/PI sheets are made with adhesive-less technology. As shown in the layout picture of Fig. 6, the top layer L1 has bonding pads, branch traces, the second layer L2 contains most of longitudinal bus lines between chips and the sensor HV line, L3 carries analogue and digital grounds all through the circuit, and L4 is the power supply plane with copper meshes. The digital and analogue ground connection is made on the hybrid aside of every ASICs.

Seventeen thermal through-holes are added underneath the analogue part of each ASIC. These vertical copper holes are filled with thermally as well as electrically conducting glue. This ensures thermal and electrical connections between each chip and the carbon–carbon bridge material. The

Table 4
Layer structure of the Cu/polyimide circuits

Layer	Material	Thickness (μm)
Top cover	Solder resist mask	20
Through-hole plating	Cu, 50% mesh	20
Single-sided Cu/PI	12 μm Cu, 1-mil PI	37
Adhesive		25
Double-sided Cu/PI	12 μm Cu, 1-mil PI	49
Adhesive		25
Single-sided Cu/PI	12 μm Cu, 1-mil PI	37
Through-hole plating	Cu, 50% mesh	20
Cover film	1/2-mil PI, 33 μm adhesive	46
Total (circuit part)		279
Total (wrap-around part)		149

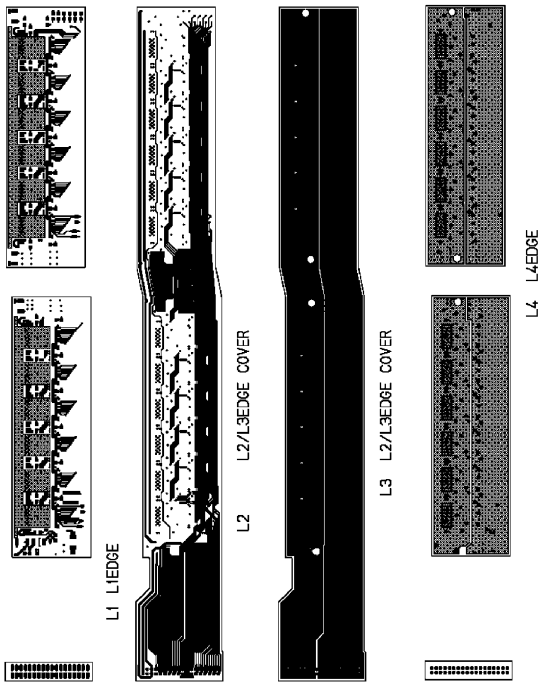

Fig. 6. Layout of the Cu/PI flexible circuit. The first and second top layers L1 and L2 are used for signal circuits, L3 is for digital and analog grounds, and L4 supplies the power plane.

effective thermal conductivity of this pillars is 40 W/mK.

3.5. Carbon–carbon bridge

The bridges reinforcing the Cu/PI flexible circuit is required to have a good thermal conductivity, high young's modulus, and low radiation length. It also functions electrically as a ground plane. The bridge is made of carbon–carbon with unidirectional fibres. The properties of the carbon–carbon material are summarized in Table 5 [10]. The bridge is machined to a thickness of 0.3 mm with legs on both ends 0.5 mm high. The surface of the bridge is coated with a polymer called Parylene of 10 μm thick. The coated surface is roughened with a laser where adhesion is required. A part of coating is removed to open windows to make a thermal and electrical contact for ASICs.

The Cu/PI flexible circuit and the carbon–carbon bridges are glued together with thermally conductive adhesive sheets, ABLEFILM 563 K-.002 with Alumina filler except the chip pillar parts where an electrically conductive sheet of ABLEFILM 5025E-.002 silver loaded is used [11]. During the curing at 125°C for 2 h, the flexible circuit and the bridges are pressed together at 4 kg/cm^2 by a press jig with a curved press surface for compensating a bend due to the difference in temperature expansion coefficients of two materials.

3.6. Glass pitch-adaptor

The basic pitch of input pads of the ASIC is 48 μm, while that of the silicon microstrip sensor is 80 μm. In order to make a simple parallel wire-bonding, a pitch-adaptor is used in front of the ASICs. Since a fine pitch of 48 μm is required, the pads and traces are fabricated on a separate piece with aluminium deposition of 1–1.5 μm thick on a glass substrate. A tape-peel test of the A1 traces and a wire-bond pull test are performed for samples. The wire-bond pull strength must be greater than 6 gr.

Table 5
Properites of the carbon–carbon for the bridge

Material	Unidirectional carbon fibres
Thermal conductivity (∥ fibre)	700 ± 20 W/m/K
(⊥ fibre)	35 ± 5 W/m/K
Density	1.9 g/cm^3
Young's modulus (∥ fibre)	294 Gpa
Tensile strength (∥ fibre)	294 Mpa
Thermal exp. coeff. (∥ fibre)	−0.8 ppm/C
(⊥ fibre)	10 ppm/C
Resistivity (along fibre direction)	2.5×10^{-6} Ω m

3.7. Passive components and mounting onto hybrid

All chip capacitors are of type X7R which has a capacitance change of $<5\%$ between -20 and $+40$°C. The resistors are of metal film precision type. A thermistor is mounted one each side to monitor the hybrid temperature. Each surface-mount part is temporally fixed on the Cu/PI surface with a dot of epoxy and then soldered manually. Solder re-flow technique is not used to avoid temperature application of higher than 60°C.

After soldering all passive components, two glass pitch adaptors are glued onto the hybrid with a room temperature curing epoxy Araldite-2011. Its low viscosity makes the glue layer thin and bubble free. The pitch-adaptor is positioned under a microscope to align to the fiducial marks within ± 50 μm.

All the hybrids, after thermal-cycling between -30 and $+60$°C for 5 times, are electrically checked via the I/O connector for bus line terminations as well as capacitances between power and ground. The hybrids with all passive components mounted but without ASICs are then delivered to the module assembly sites. Fig. 7 is a photograph of the hybrid with all components mounted on.

4. Module assembly

The barrel module assembly is carried out in the four assembly cluster in Japan, UK, Scandinavia and US. Assembly jigs are slightly different in some technical details, but each assembly clusters is required to assemble the modules to meet the exactly same specifications.

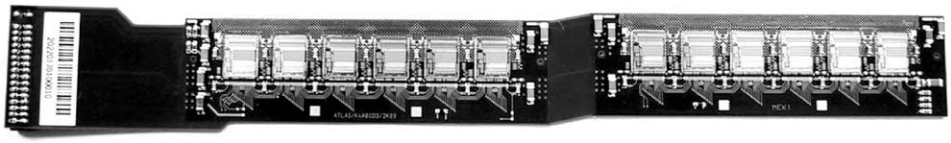

Fig. 7. Picture of the hybrid with chips and components mounted on.

4.1. Sensor-baseboard assembly

A great amount of effort was devoted to developing procedures and fixtures since the most demanding mechanical precision is required at this step. Requirements are to align not only each pair of sensors in the plane but also the top-bottom pairs. In addition sensors must be aligned to the module reference point, the dowel holes of the BeO facings. It is also important to minimize module distortion out of the module plane.

(1) Sensor alignment: Two silicon sensors are placed strip-side up vacuum chucked on a pair of precision $x-y$-rotation stages under a microscope. Two sensors may be pre-aligned in a separate jig and transferred using a vacuum chucking. Fig. 8 shows an example of such precision $x-y$-rotation stages which is equipped with 6 piezo actuators for sub-micron adjustment. An automatic pattern recognition program may be used to identify and precisely locate the fiducial marks on the sensors. The surfaces of silicon sensors are protected at all stages, when in contact with jigs by a new piece of disposable pre-cut clean room paper.

(2) Sensor pickup: A pair of sensors thus individually and precisely aligned under the microscope is transferred to a pick-up jig with vaccum-chucking. A definite sequence of vacuum-chucking and releasing is needed in order to keep the alignment precision during the sensor transfer. A precision alignment between the stage and the transfer jig is realized with a set of linear bearings. One can see these linear bearings in Fig. 8.

(3) Sensor-baseboard gluing: After positioning of the baseboard on a precision glue fixture, a 3 axis dispensing workstation is used to dispense the high viscosity adhesive mix of Araldite-2011 and boron nitride filler on the baseboard. Drops of the adhesive are applied to one side of the baseboard according as a pre-defined pattern. Then two sensors are placed with appropriate pressure and gap spacing. The silver loaded conducting epoxy Eotite p-102 is applied at two spots each per sensor manually for electrical connection between the baseboard and the sensor back-side.

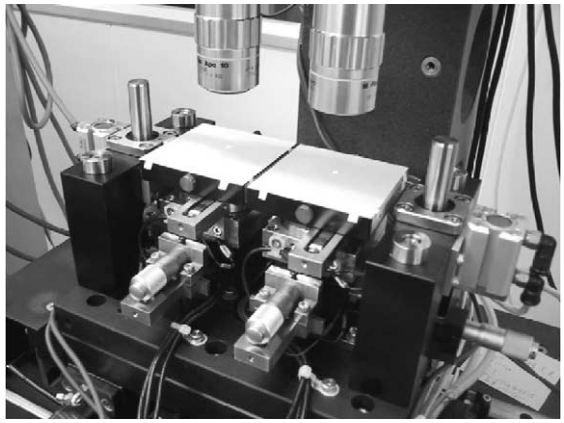

Fig. 8. Typical assembly microscope unit for sensor alignment.

(4) After curing, another pair of sensors is glued on the second side of the baseboard in the same way.

(5) After the detectors are glued to the baseboard, the $I-V$ curve is recorded for each sensor individually up to 500 V. If any current at 500 V bias differs by more than 1 μA from that last recorded, the assembly is put aside for checks.

4.2. ASICs stuffing

The chips are glued on the hybrid with electrically conductive epoxy, Eotite p-102. Four fiducial marks on the hybrids are used for aligning

the chip. The epoxy is cured at 50°C for 2 h. All nearby bonding pads are masked during gluing. After all (but for input channels) wire bonds are made, an electrical test is done to ensure that all ASICs perform properly and that all wire bonds are functional. Bad chips can be replaced using a simple jig with local heat application. In addition, a longer duration test at elevated temperature of 45°C with nominal L1A trigger frequency of 100 kHz is performed for 100 h in order to catch infant mortality problems in the ASICs. It is noted that experience to-date has shown no such long-term failures. The temperature and duration will be adjusted during production phase in the light of experiences gained.

4.3. Mounting the hybrid on the sensor-baseboard assembly

This process is comparatively simpler using a set of special jigs which carry wrapping-around motions over the sensor-baseboard assembly. Great care must be paid not to touch the surfaces of both objects. The required accuracy of positioning is mild and $\pm 50\,\mu m$. The long pot life of the adhesive allows ample time for repositioning. After curing and visual inspection, the assembly is mounted into a special protection box for storage, interim performance checks (including HV application) as well as for full wire-bonding.

4.4. Full wire-bonding

Firstly, connections for the HV line and ground between sensors and hybrid are made via bonding wires. Then the high-density wire-bonds of 768 channels are made with dedicated automatic wire-bonder between the chip input and the pitch adaptor, between two sensors, and finally between the pitch adaptor and the sensor. There are in total 4608 of these wire-bonds per module. Particular care is required in wire-bonding between pitch adaptor and sensors for 1 mm difference in height. Typically one module can be bonded and inspected within 4 h. Fig. 9 is a picture of the module completed.

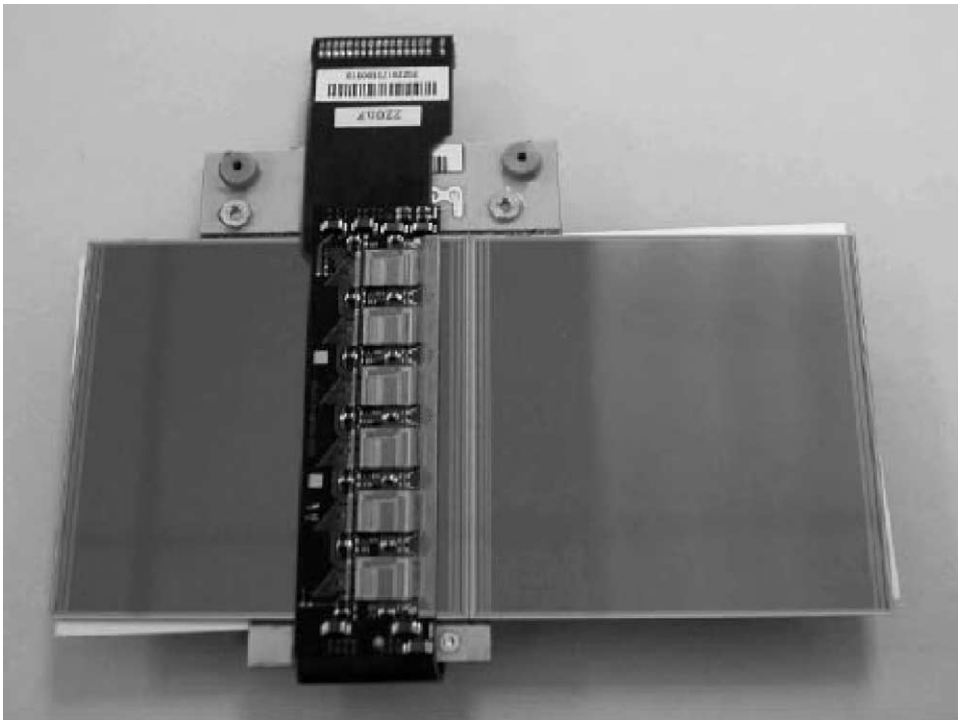

Fig. 9. A picture of the ATLAS barrel SCT module.

5. Quality assurance of the module

The following QA steps are performed on fully assembled modules. The criteria for accepting a module as 'good' are for initial use, and may evolve with experience on mass production.

5.1. Sensor test

With the ASICs unpowered, the detector $I-V$ curve is recorded up to 500 V. The total leakage current of good modules at 500 V should not be more than 4 μA than the sum in the database. Then all modules will be tested for long-term leakage current stability at 150 V over 24 h in a cold inert atmosphere. This test is performed in parallel with the long-term electrical test on modules with ASICs powered on. The current drawn is monitored periodically. The maximum increase in leakage current should be $<4\,\mu A$ per module, after an initial settling time of 5 min.

5.2. Metrology

Each completed module is surveyed for mechanical precision with a 3D measuring machine. For the measurement, a module is placed on a frame and is held at three points. The frame has a number of transparent fiducials so that the measurements of the front and back sides can be correlated.

(1) *In-plane survey*. The in-plane survey characterizes the relative positions of the four sensors and the dowel hole/slot of the baseboard. The locations of a sensor are obtained by measuring eight fiducial marks on sensors. The centres of the dowel hole and slot are obtained by measuring their perimeters. From 34 $x-y$ measurements, the module coordinate and a reduced parameter set are obtained as shown in Fig. 10. In this coordinate system, the reduced parameter set is listed in Table 6 with the design values and the tolerances specified. Some typical deviations from the design values are plotted in Fig. 11 for seven modules constructed by the Japanese cluster. For all the parameters, the main parts are well within the tolerances. However, occasionally, there is a measurement at the limit of the tolerance. Similar results are accomplished for modules made by the UK-B cluster.

(2) *Out-of-plane survey*. The z-height of each sensor in the module is measured at a matrix of 5×5 points. In addition, three points are measured on the surfaces of the cooling contact and the far-end facings on the back

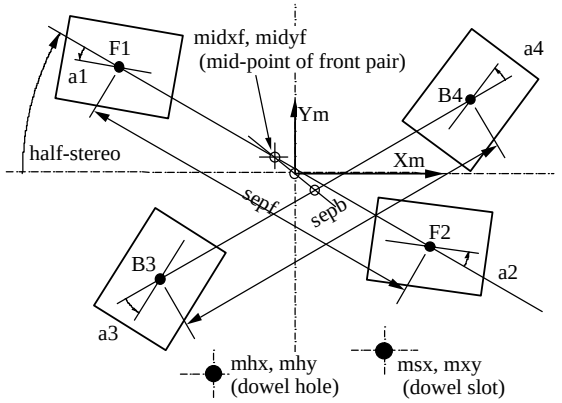

Fig. 10. Thirteen parameters to describe the module geometry. F1, F2 and B3, B4 are the front and back sensors respectively. The coordinates origin is the centres of four sensors. The values (midxf, midyf) are the coordinates of the front sensor pair, (sepf, sepb) are the sensor separations, (mhx, mhy) and (msx, msy) are the coordinates of the dowel hole and slot of the baseboard respectively, a1, a2, a3, a4 are the sensor angles stereo the half-stereo angle.

Table 6
Module in-plane geometry parameters

Parameter	Design value	Tolerance
Dowel hole, mhx (μm)	−6500	30
Dowel hole, mhy (μm)	−37,000	30
Dowel slot, msx (μm)	38,500	100
Dowel slot, msy (μm)	−37,000	30
Mid-point of front pair, midxf (μm)	0	10
Mid-point of front pair, midyf (μm)	0	5
Separation of front pair, sepf (μm)	64,090	10
Separation of back pair, sepb (μm)	64,090	10
Sensor1 angle, a1 (mrad)	0	0.13
Sensor2 angle, a2 (mrad)	0	0.13
Sensor3 angle, a3 (mrad)	0	0.13
Sensor4 angle, a4 (mrad)	0	0.13
Half-stereo angle, half-stereo (mrad)	−20	0.13

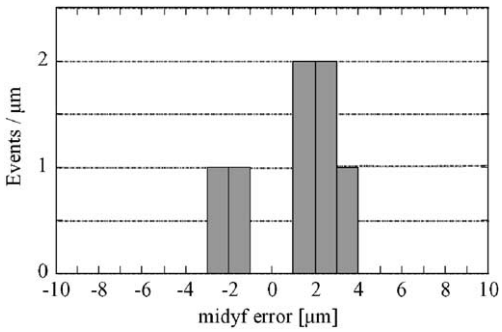

Fig. 11. An example of in-plane survey: deviations from the nominal of midyf for 7 KEK prototype modules.

side of the module, defining the module plane as mounted on the supporting CFRP brackets. The out-of-plane tolerances are constrained by two factors; the maximum height of a sensor surface from the nominal should be $<200\,\mu m$ to keep at least a 1 mm 'stay clear' distance between modules and the residuals in z-flatness should be $<50\,\mu m$ for global track fitting. Fig. 12(a) plots the maximum deviation of the sensor surface from the nominal z position with respect to the module plane. The z-profile measurement includes an intrinsic and systematic bowing in the sensors of about 50 μm. The intrinsic bowing can be expressed by a universal shape function. In addition, the left-right mid-planes (defined by the average of top and bottom sensor heights) are not on a flat single plane. The latter can be fitted with $z = ax + by + c$ separately in the left and the right sides, requiring 6 parameters. Fig. 12(b) plots the maximum deviation of ray sensor from the 'predicted' z-profile with these two corrections of sensor bowing and left-right asymmetry. All modules satisfy the specification of $<50\,\mu m$ for deviation.

(3) *Thermal cycling and long-term tests*. The same in-plane and out-of-plane metrology is repeated after thermal cycles ($-30 \sim +60^{\circ}C$, repeated 5 times) and long-term test (24 h with hybrid power on, hybrid temperature at $\sim 30^{\circ}C$). Though the in-plane surveys show no change, a change was observed in the out-of-plane profile, majority being within 20 μm,

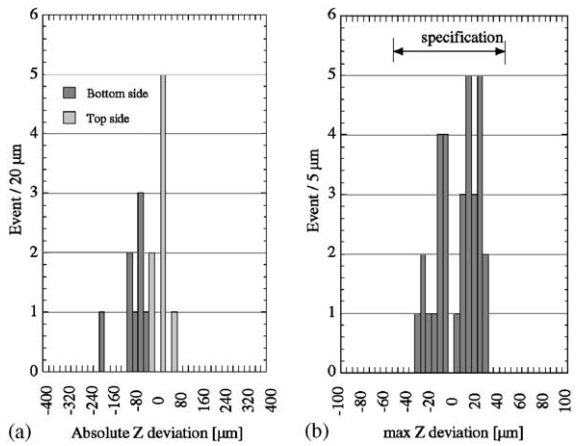

Fig. 12. (a) z-Deviation of the sensor surface height from the nominal z position, and (b) z-deviation after the corrections of sensor bowing and left-right asymmetry.

except the one showing a change from 83 μm before to 123 μm after the thermal cycles.

5.3. Electrical tests

An extensive suite of both hardware and software has been developed to facilitate module testing. The readout system is based around the VME modules CLOAC, MuSTARD and SLOG, together with low voltage and high voltage modules SCTLV and SCTHV. Two largely automated series of tests have been devised. The Characterization Sequence is to perform full measurements of a module and they are

(a) power-on/verification of response to hard reset,
(b) clock and command reception test,
(c) bypass functionality test,
(d) pipeline efficiency test,
(e) strobe delay scan,
(f) three point estimation of gain, noise and offset,
(g) trim-range scan,
(h) determination of the response curve,
(i) noise occupancy scan,
(j) time-walk scan,

whereas the shorter Confirmation Sequence of (b), (c), (e) and (f) provides a minimal set to ensure the digital functioning and analogue performance.

The analogue performance is measured with respect to the internal calibration circuitry of the ABCD chip with a correction for the variation of calibration capacitance between batches of wafers. A summary of the results of each test will be recorded in the database. A module is classed as good if at least 99% of its readout strips operate efficiently with low noise occupancy at 1 fC threshold.

A very small sample of the completed barrel modules will be uniformly irradiated at the CERN PS to a fluence of $3\times10^{14}\,\mathrm{p/cm^2}$ 24 GeV/c protons. After annealing for 7 days at room temperature, they will be checked including mechanical integrity, noise performance, full ASIC functionality and detector leakage current. Several of these modules will also be tested in the beam for S/N and efficiency performance.

6. Thermal performance

Over a period of several years during development of the module design, several thermal modules were built for detailed thermal study, in particular to check the FEA calculations regarding thermal runaway of irradiated detectors. Agreement has been good.

The temperature profile has been measured for a sample of un-irradiated modules by using a infrared thermo viewer. The measurement is only useful, due to reflection by sensor surfaces, for estimating the temperature of the hybrids and the facings. Thermo viewing is not a technique that will be used for every module during production, but can be a useful diagnostic tool. A typical example of the measured temperature profile showed that the highest temperature on the hybrid was 11–12°C at the location of the ASICs with respect to that of the baseboard. The thermal FEA simulation is consistent with these measurements.

A thermal module was built using irradiated silicon sensors in which the ASIC heat generation was simulated with dummy heaters. This module was cooled via a cooling pipe thermally attached to the BeO cooling facing as planned in the final setup. With the hybrid power of 8.1 W and at a coolant temperature of around −10°C, no thermal runaway was observed. The power dissipation in the sensor bulk was about $130\,\mu\mathrm{W/mm^2}$ normalized to 0°C. The result is in agreement with FEA simulation.

7. Electrical performances

The number of electrical barrel modules is limited by the supply of ASICs. So far 26 modules were constructed including modules with previous ASIC versions of ABCD2Ts and ABCD3Ts.

7.1. Noise and noise occupancy of un-irradiated modules

At room temperature, the measured noise is in the region of 1400–1700 ENC. At the operating temperature of ~0°C on the hybrid, the noise is reduced to typically about 1350 ENC. This corresponds to an expected S/N value of better than 14. The noise of each individual readout channels of an ABCD3TA module, operated warm, is shown in Fig. 13. A uniform noise distribution is seen, apart from a single channel on the module that is bonded to only a 6 cm length of sensor.

Fig. 14 shows the hit occupancy dependence of the threshold, summed over all channels of a module with un-irradiated sensors and ABCD3T-A chips. Its smooth Gaussian-like shape is a strong evidence of the electrical stability of the readout system. The target threshold is set at 1 fC to ensure

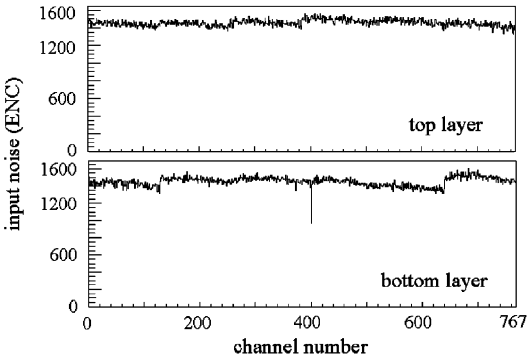

Fig. 13. Measured noise values (ENC) on all channels of ABCD3T-A module 20220170100018.

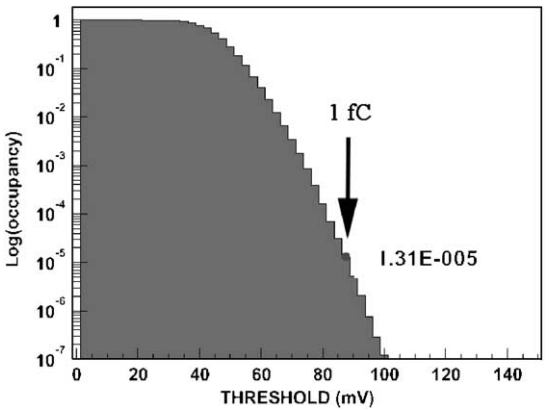

Fig. 14. Mean noise occupancy of all channels of ABCD3T-A module 20220170100018, measured warm.

high tracking efficiency for particles traversing the silicon at inclined angles. As shown in the plot, the noise occupancy at 1 fC threshold is an order of 10^{-5} satisfying well the requirement of 10^{-4}, at least at the stand-alone module level.

7.2. Timewalk

The timewalk should be <16 ns where the timewalk is defined as the difference in time stamp threshold over a signal range from 1.25 to 10 fC, with the comparator threshold set to 1 fC. It can be measured by changing the pulse height and strobe delay of the internal calibration pulses. All modules showed the timewalk of about 5 ns well below the limit [12].

7.3. Noise and threshold uniformity of irradiated modules

Four modules with chips of ABCD3T or ABCD3T-A (with 4 trim ranges) have been irradiated to the full dose of $3\times10^{14}\,\mathrm{pcm}^{-2}$. The trim circuitries after the exposure was fully functional, as Fig. 15 shows, all channels being aligned using trim range #2 (0–180 mV) with maximum channel-to-channel threshold variation within 12 mV. Corresponding trim DAC settings are also plotted, indicating fairly large threshold changes due to radiation. The measured ASIC noise value when operated cold, with the hybrid around 0°C, averages about 2050 ENC, resulting

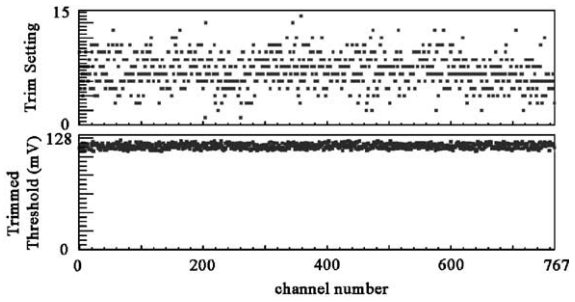

Fig. 15. Trim DAC setting (upper graph) and trimmed threshold (lower) versus channel number for a module with ABCD3T-A after irradiation to $3\times10^{14}\,\mathrm{p/cm}^2$.

the S/N ratio of 10. Though this ratio is lower than the target value, the noise occupancy at 1 fC threshold is about 3×10^{-4} as measured in the test beam.

7.4. Test beam results

Various modules have been tested at CERN and also at KEK. Both irradiated and non-irradiated modules have been measured in the beam tests. During these tests, the modules are all kept cold, with the hybrids operating at about 0°C.

(1) *Charge collection and S/N ratio*. The median charge of three modules (two unirradiated, one irradiated), obtained from the 50% efficiency point in threshold scans, as a function of detector bias voltage is shown in Fig. 16a. The detectors of the two un-irradiated modules have depletion voltages of ~80 V, and are normally operated at ~150 V bias. The irradiated module is operated at ~400 V bias, at which point it is seen that the collected charge on a single strip is similar to that for unirradiated modules. Fig. 16b plots the S/N values in which any uncertainties in the calibration circuitry are cancelled out.

(2) *Efficiency at 1 fC threshold*. The efficiency of the modules at the nominal operating threshold is typically measured to be $>98\%$ at the operational bias voltages over the full range of particle incident angles, with or without a magnetic field. This is illustrated by data from the CERN beam test. In Fig. 17, the efficiency

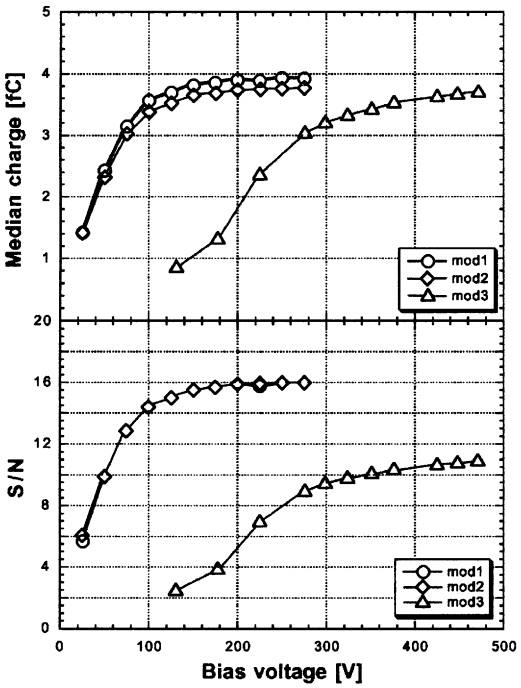

Fig. 16. Median charge in fC (top) and the S/N ratio (bottom) versus bias voltage for two un-irradiated modules and one module irradiated up to $3 \times 10^{14}\,\mathrm{pcm}^{-2}$.

for an irradiated module is shown as a function of angle. The maximum efficiency recorded is a function of tracking cuts, and plateau values in excess of 99% can be obtained.

(3) *Space resolution*. The measured resolutions are consistent with the expectation of the 80 μm binary strip pitch (i.e. 23 μm) for tracks at normal incidence with the magnetic field on. The resolution for inclined tracks is slightly better because two strip clusters occur with greater frequency.

7.5. System test

The goal of the system test is to run as many modules as possible in a physical configuration which is as close as possible to the planned ATLAS configuration, thereby testing the performance of the modules in such a system and comparing it to their stand-alone performance. Modules are mounted on a sector of the carbon-

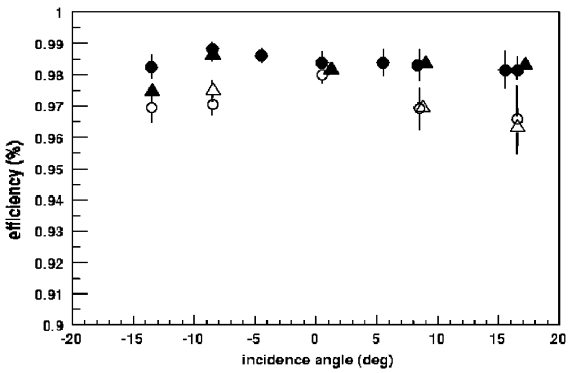

Fig. 17. Measured efficiency of the fully irradiated module at 1 fC threshold as a funciton of the beam incident angle. The triangles are with the magnetic filed of 1.56 T, the circles with zero field. The open symbols are with a bias voltage of 300 V, the full symbols for 450 V.

fibre-corex cylinder with dimensions very near to those of the innermost ATLAS barrel. Modules are powered and read out via prototype barrel opto-harnesses, which transmit power to the modules, decode the optical clock and commands, transmit these signals electrically to the modules, and transform the data from the modules into optical signals for transfer to the readout electronics. Each opto-harness serves up to six modules, as in the final system. Almost all patch panels and power tapes used are true to the planned final ATLAS design. A photograph of the barrel sector can be seen in Fig. 18.

For the measurement reported here, there were ten modules in the system test. Eight of these are considered 'good' modules. With the exception of one module, all the modules showed approximately the same noise values (within about 100 ENC) when running alone on the sector as they did on the bench. A typical multi-module test is to measure the gain and noise with many modules running in parallel. This has been performed, using a three-point gain calculation, with the ten modules on the sector. For this test there were two harnesses on the left-hand half of the sector, mounted immediately adjacent to one another, with each harness holding five modules. The measured noise values of all ASICs on the modules, with all 10 modules in operation at a hybrid temperature of 26–30°C, are shown in

Fig. 18. Photograph of 10 barrel modules mounted on the carbon-fibre structure for system test.

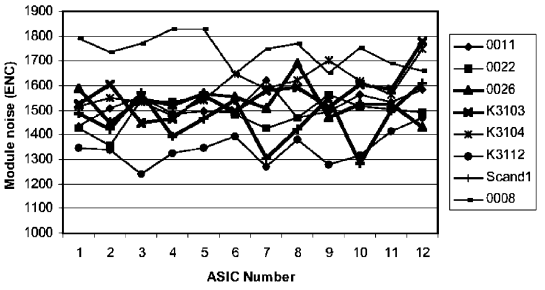

Fig. 19. The measured average noises for each ASIC with 10 modules operating together on the barrel system test sector.

Fig. 19. With the exception of module 0008, the noise values lie in the anticipated range. Module 0008 showed $\sim$200 ENC more noise on the sector. This may be of significance, since this is the only module made with the ASICs attached to the hybrid via non-conducting glue. The first results presented here are clearly encouraging.

8. Summary

The final module design was successfully reached at the final one by devoted efforts of the ATLAS SCT group and institutes involved. So far 26 modules were fabricated and tested. Almost all stringent mechanical, thermal and electrical requirements on the barrel SCT modules for precision tracking as well as for the survival over 10 years under the LHC environment are satisfied by the present module design.

Many new technologies are for the first time employed such as VHCPG baseboards, Cu/Polyimide flexible hybrids, carbon–carbon bridges. The pre-series modules produced at various assembly clusters showed satisfactory mechanical, thermal and electrical performances. High precision assembly was well demonstrated. Various beam tests with irradiated sensors proved the functionality of the modules up to the highest dose expected. The trimADCs to achieve uniform thresholds are demonstrated to work and to be crucial for irradiated modules.

The system test with 10 barrel modules with close-to-final configuration started to show good electrical stability.

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