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Beam study of irradiated ATLAS-SCT prototypes

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Abstract

Prototypes of ATLAS-SCT modules with ABCD readout chips were tested in a 4 GeV/c pion beam at KEK's proton synchrotron. Of both SCT module geometries—barrel and forward—three identical modules were placed in the beam. One module of each type had been irradiated to 3×10^{14} protons/cm^2 in the CERN PS previous to the beam test. A method has been developed to reconstruct the time-resolved shaper pulse from the binary hit information, allowing a more detailed study of the timing properties of the ABCD. The present results will be compared to a simulation of the charge collection and Front End electronics response.

1. Introduction

In December 2000 a 4 GeV/c pion beam line ($\pi 2$) of KEK's proton synchrotron was made available for a beam test of module prototypes. Of both barrel and forward SCT geometries, three identical modules were submitted to the beam test, one of which had previously been irradiated in the PS at CERN to a dose equivalent to that expected after 10 years of operation in ATLAS: 3×10^{14} protons/cm^2 [1].

All modules were built with the same version of the SCT readout chip, the ABCD3T [2]. Each channel of this chip has a preamplifier, shaper and comparator circuit. Comparison of the signal to a settable threshold produces the binary (hit/no hit) output.

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With the binary readout scheme, statistical methods must be developed to extract pulse height and timing information. Here, the binary hit information is combined with a measurement of the incidence time of the particle to reconstruct the time-resolved shaper pulse. Comparison of the pulse shape at different bias voltages in non-irradiated and irradiated modules provides information on the timing relations of detector signal and Front End electronics.

A simulation of the time-resolved detector signal was convoluted with the approximate transfer function of the ABCD. The results will be compared to those obtained in the test beam.

Results of earlier SCT beam tests can be found in Refs. [3,4]. The detailed results from the KEK test beam have been submitted for publication at a later date [5].

2. Setup

Fig. 1 shows the arrangement of the six modules under test in the beam line. Modules of the barrel and forward geometry have quite distinct layouts and use different hybrid technologies [6,7]. The three KEK modules are of the barrel type, whereas the forward modules were built by IFIC Valencia and CERN-Geneva. One module of each type—KEK03 and VAL166—had been irradiated to 3×10^{14} protons/cm^2.

The KEK-PS produces a continuous beam, whereas in the LHC the bunch crossing and readout clocks will be synchronous. Therefore, the time of incidence of the particles with respect to the system clock is measured using a time to digital converter. Off-line, the time information can be used to minimise the effect of the continuous beam and evaluate the performance of the prototypes in circumstances similar to those envisaged for the LHC.

A beam telescope, made up of three pairs of silicon microstrip detectors with analogue readout, is used to reconstruct the tracks of passing particles. The three pairs of telescope planes are interleaved with SCT modules inside the light tight climate chamber to reduce the effect on track reconstruction of multiple scattering.

Each of the DUTs was contained in a test frame equipped with cooling contacts similar to those envisaged for ATLAS and the possibility to cool the modules using cold liquid from a chiller. The temperature on the forward hybrids was found to be considerably higher than that on the barrel hybrids, at least partly due to the different hybrid topology.

In the irradiated modules some of the ASICs showed a problem in the receiver circuit that handles token passing. Also, on some chips the trim range was not set correctly when operated at low temperature.[2] Both the problems could be avoided by raising the digital supply voltage and thus the temperature of the ASICs. VAL166 and

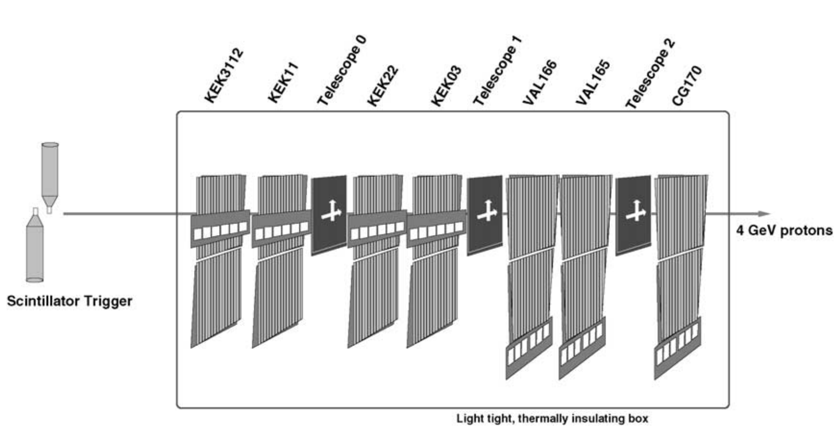

Fig. 1. Schematic setup of the setup of the December 2000 beam test.

KEK03 were supplied with a digital voltage of 5.1 and 4.8 V, respectively, where the nominal digital supply voltage is 4 V.

3. Calibration

In order to relate the comparator threshold voltage to input charge, a full characterisation of the Front End shaper-amplifier is made using the ABCD's internal calibration circuit. In the various calibrations performed the input charge was varied in the range between 0.5 and 8 fC. For each of these charges a threshold scan is performed. The 50% occupancy threshold corresponding to each charge is found from an error function fit of the S-curve.

The absolute accuracy of the calibration depends critically on the accuracy of the various components of the calibration circuit. Measurements on test structures from the same wafer [8] and on some of the modules [9] have found small deviations from the nominal values. The analysis uses a parameterisation of these measurements to correct the charge scale.

4. Analysis

To facilitate the analysis, the raw data from all sub-systems are processed off-line into summary files that present all data in an accessible format. Importantly, all DUT and telescope planes are internally aligned at this stage and tracks are reconstructed from the space points measured by the telescope modules. The off-line pre-processing of the data includes the reconstruction of the tracks measured by the telescope.

The analysis compares the response of the binary prototypes to the "known" position of the tracks, extrapolated from the beam telescope information. A detector plane is considered efficient if a cluster centre is located within 100 μm of the known track position. Traditionally only events in a narrow time slice were accepted in the analysis in order to simulate a synchronised readout. The present analysis tries to make a full use of the available information by explicitly reconstructing the dependence of the signal on the charge deposition time.[3] The time axis is extended to cover 75 ns using the hit information from the previous and next clock cycle, as provided by the ABCD. For each 1 ns time interval, the variation of efficiency with comparator threshold (S-curve) is constructed. The median charge is then found as the threshold where 50% efficiency is obtained (VT50).

Charge sharing between adjacent strips will lead to relatively low signals that can distort the pure pulse shape. Also, this effect is hard to estimate in the simulation. Therefore, only tracks "right on the strip", where the extrapolated track position lies within 20 μm of the nearest strip, are accepted in the analysis.

5. Simulation

An algorithm originally developed by Leslie, Seiden and Unno [10] was used to simulate the detector signal. A discrete map of the electrical field in the silicon is obtained by solving Poisson's equation on a two-dimensional mesh. A fixed charge density is assumed, related to the depletion voltage by $V_{\mathrm{FD}} = ed^2|\rho|/2\varepsilon_0\varepsilon_{\mathrm{Si}}$ In the non-depleted region, covering a fraction $w = 1 = \sqrt{V_{\mathrm{bias}}/V_{\mathrm{FD}}}$ of the detector width, the charge density is assumed to vanish. The depletion voltage of non-irradiated detectors is set to 60 V in agreement with wafer measurements.

The charge deposition by 4 GeV pions is simulated by generating a random charge according to a Landau distribution, convoluted with a Gaussian [11], in small intervals along the particle's track. The charge carriers are drifted through the silicon according to a parameterisation by Muller and Kamins [12]. The induced signal on the strips by moving charges in the silicon depends on

[2] The trim range problem has been solved in later versions of the chips. Later batches do not show the token passing problem.

[3] The relative charge deposition time is measured as the delay between the raw trigger from the scintillators and the next rising edge of the 40 MHz system clock.

amount of charge, the drift velocity of the carriers and a weighting field, found by solving the Laplace equation.

For the irradiated modules, it is assumed that type inversion has taken place and the p–n junction forms at the backplane. Partially depleted operation is still possible, but the signal has to be induced across the non-depleted region. The depletion voltage after beneficial annealing will be assumed to be 250 V, a rough estimate on the basis of the charge collection versus bias voltage behaviour measured in the same beam test, to be published at a later date [5].

The total input signal to the electronics is taken to be the sum of the currents induced by both types of carriers. To obtain the ABCD front end's response to the simulated detector signals, the strip current is convoluted with the response function of a $CR(RC)^3$ shaper with an extra differentiation step.

6. Results

The pulse shape of six modules has been reconstructed for a whole range of detector bias voltages.

Fig. 2 compares the pulse shape obtained from a non-irradiated forward module (VAL165) with the detectors biased at 150 V to a simulated pulse using the same voltage.

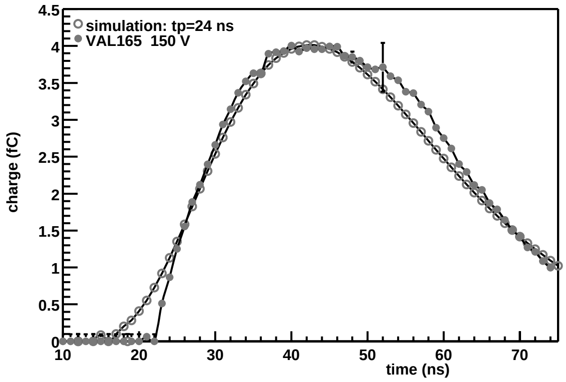

Fig. 2. Pulse shape for a non-irradiated forward module.

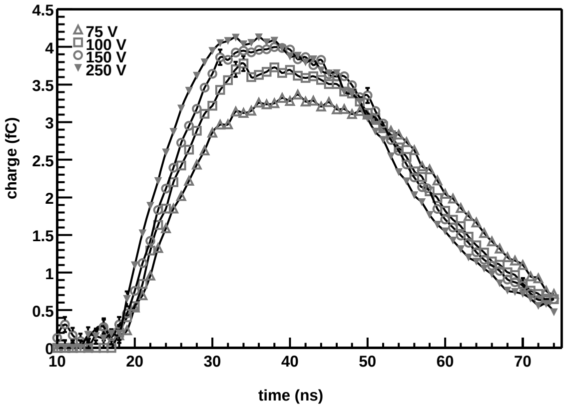

Fig. 3. Pulse shapes for a non-irradiated barrel module.

A shoulder is found on the falling edge of the pulse that cannot be reproduced by the simulation. It is probably due to feedback of the discriminator switching. Apart from this shoulder, the dependence of the pulse shape on bias voltage in non-irradiated modules is described rather well by the simulation throughout the measured bias voltage range (25–275 V). The pulse shape hardly changes between 150 and 275 V. At lower voltages it is stretched due to ballistic deficit of the shaper (Fig. 3).

For the barrel modules the best agreement between simulation and data is obtained for a simulated peaking time of 22 ns, in agreement with the ABCD specification. A consistently longer peaking time—best-fit value 24 ns—is observed on the forward modules. This difference is most likely due to the higher ASIC temperature on the forward modules.

As becomes clear in Fig. 4, for the irradiated modules the deviation of the pulse shape from the prediction by the model, the shoulder, is more pronounced. Moreover, irradiated modules are found to have a longer pulse shape than non-irradiated modules of the same type. For the irradiated barrel module, the best fit between data and simulation is obtained for a peaking time of 24 ns. The increase in peaking time in the forward module is even more pronounced. This increase is thought to be the result of the combination of slower charge collection in the irradiated detectors

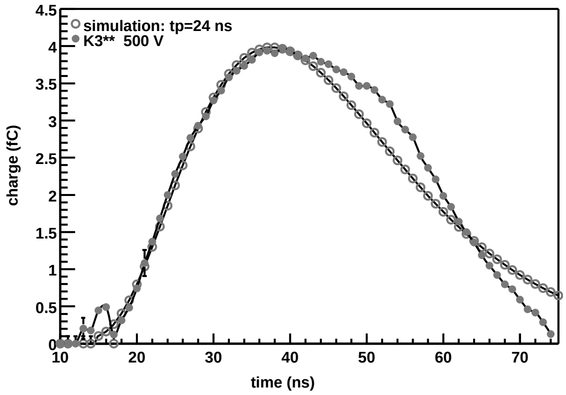

Fig. 4. Pulse shape for an irradiated barrel module.

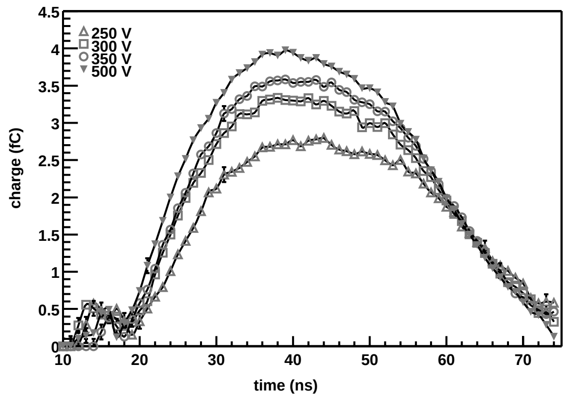

Fig. 5. Pulse shapes for an irradiated barrel module.

and the degraded speed of the amplifier after irradiation.

Figs. 5 and 6 present the pulse shape in the two irradiated modules for a number of bias voltages.

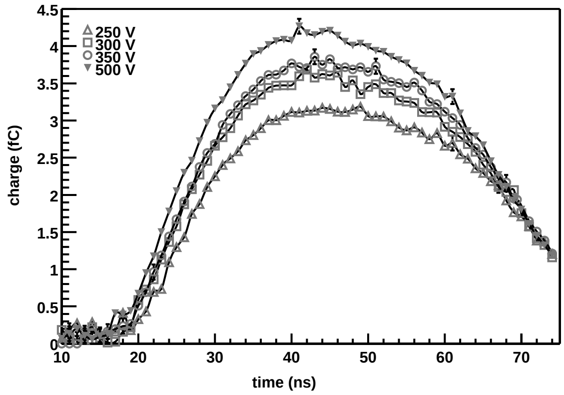

Fig. 6. Pulse shapes for an irradiated forward module.

7. Conclusions

A statistical method to extract the pulse shape of the ABCD Front End amplifier/shaper has been applied to test beam data taken at KEK. Comparison of the reconstructed pulse shapes in a range of detector bias voltages to simulation yields good agreement for non-irradiated modules.

The peaking time of the shaper in non-irradiated barrel modules was found to be approximately 22 ns, in agreement with the design value. Forward modules have slightly longer peaking times of approximately 24 ns. The difierence is thought to be an effect of the higher ASIC temperature on the forward modules. In either case, the pulse is not affected significantly by ballistic deficit of the shaper down to 150 V.

In modules irradiated to 3×10^{14} protons/cm^2, the pulse shape depends strongly on the bias voltage. In the irradiated modules an increase in pulse length was observed with respect to the non-irradiated modules, even when the detectors are biased to 500 V. This increase is attributed to the slower charge collection in the irradiated detectors and the degraded speed of the amplifier.

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