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Evaluation of OKI SOI technology

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Abstract

The silicon-on-insulator (SOI) CMOS technology has a number of advantages over the standard bulk CMOS technology, such as no latch-up effect, high speed and low power. The fully depleted SOI (FD-SOI) technology provided by OKI Electric Industry Co., Ltd. is realizing the full features of the advantages with lowest junction capacitance. Test element group (TEG) structures of transistors were fabricated and irradiated with protons. The first results are presented.

Keywords: SOI; CMOS; FET; Radiation damage

1. Introduction

The silicon-on-insulator (SOI) CMOS technology has a number of advantages over the standard bulk CMOS technology, such as no latch-up effect, high-speed and low-power dissipation. A monolithic pixel detector featuring these advantages [1] is being developed under KEK Detector Technology Project. The fully depleted SOI (FD-SOI) CMOS technology provided by OKI Electric Industry Co., Ltd. is realizing the full features of the advantages with lowest junction capacitance [2]. In addition, high-radiation tolerance is expected, especially against single-event latchup, since the devices are fabricated using a very thin (40 nm) silicon layer. Therefore, we are investigating front-end circuits using the same technology [3] to apply them in high-radiation environment. In this paper, we report the first results concerning the total dose effects for transistors fabricated using the OKI 0.15 μm FD-SOI CMOS process.

2. Transistor TEG circuit

The test element group (TEG) chip consists of a matrix of 32 NMOS and 32 PMOS transistors in order to extract DC characteristics efficiently [4]. Fig. 1 shows a schematic diagram of the transistor TEG circuit. Each transistor is selected by 3-bit column and 3-bit row decoders and NOR and NAND gates. ESD protection diodes are implemented in all IO terminals of the TEG chip. PMOS transistors are located from 0 to 3 rows. NMOS transistors are located from 4 to 7 rows. The transistors in 0, 1, 4, and 5 rows have body-tie contacts, which connect the source electrode to the body of the transistor via metal layer. The device structure of body floating and body-tied transistors is shown in Fig. 2. In the shuttle service, OKI provides three types of transistors: I/O transistors (IO) with 5 nm thick gate oxide layer, and high-VT (HVT) transistors for logic circuits and low-VT (LVT) transistors for analog circuits with 2.5 nm thick gate oxide layer. The voltage tolerances are 1.8 V for I/O circuits, and 1 V for core circuits. The parameters of each type of transistors are listed in Table 1. With fixing the W/L ratio to 2000, we tested two to three width and length combinations for each transistor type, as

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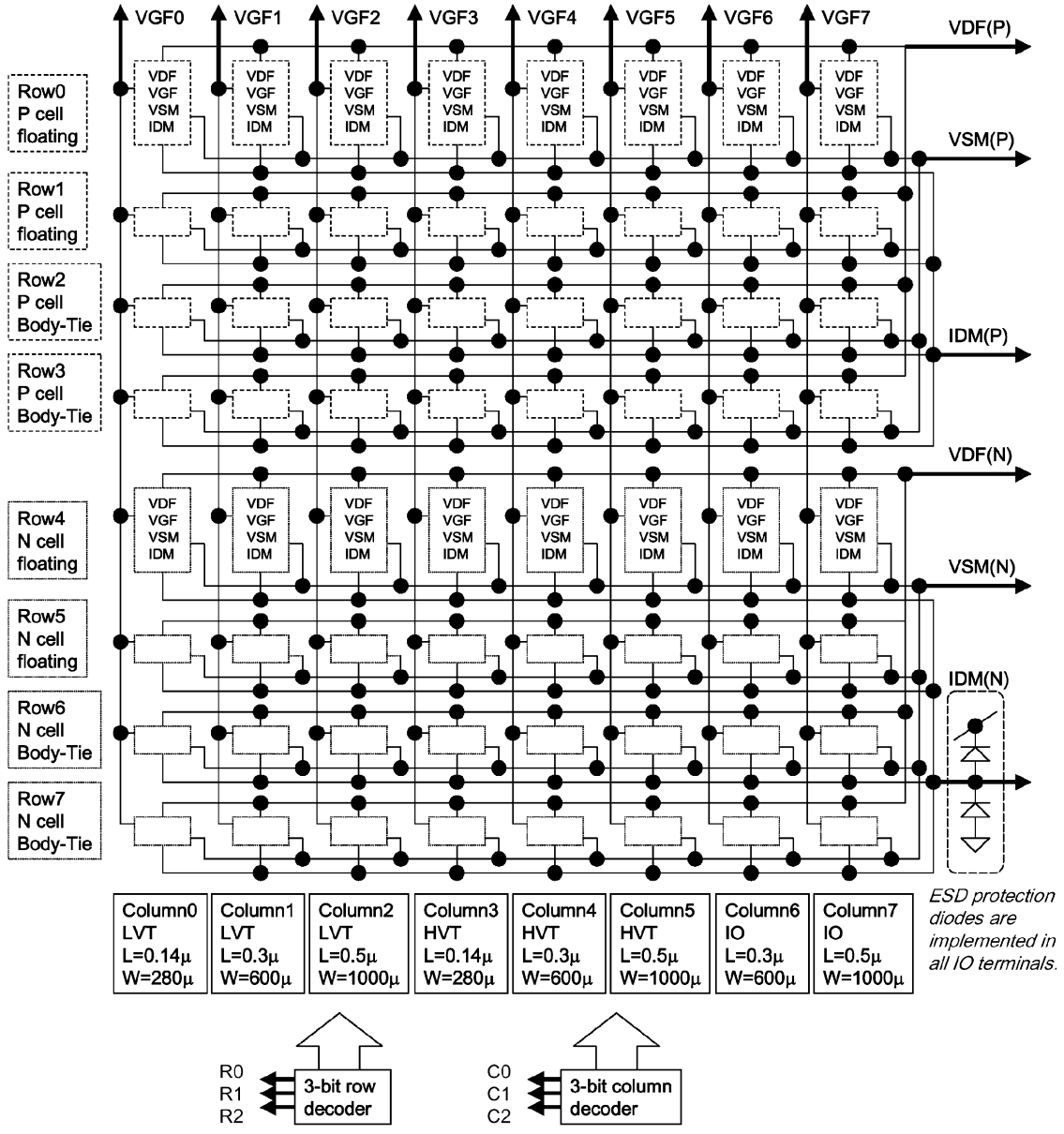

Fig. 1. Schematic diagram of the transistor TEG circuit.

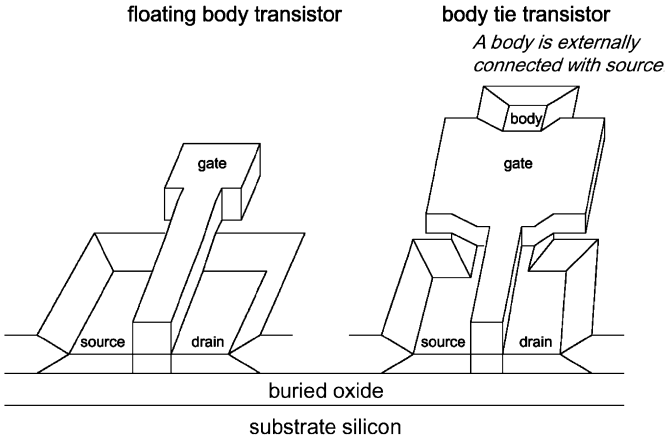

Fig. 2. Device structure of floating body and body-tie transistors.

summarized in Table 2. The buried oxide layer is 200 nm thick. The backside of wafer was ground down mechanically from 650 to 350 μm thickness, and then plated with 200 nm of aluminum, which is used for back-gate biasing.

Figs. 3 and 4 show details of N and PMOS transistor cells. The drains of all N and PMOS DUT (device-under-test) transistors are ganged together, respectively. The gates in the same column are connected to a common. The sources are connected to another common via M2 and M3 switches. These switches are operated by 3-bit column and 3-bit row decoders. The voltage of IDM is fixed to 0 and 1 V for N and PMOS cells, respectively. The TEG characterization is to measure the drain current (I_{ds}) as a function of the gate-source (V_{gs}) voltage while keeping constant the drain-source voltage (V_{ds}). The voltages of V_{gs}

and V_{ds} are controlled by the external voltages of VGF and VDF with taking account of the finite on resistance of the M2 switch. The voltages of V_{gs} and V_{ds} were actually adjusted iteratively by monitoring the voltage of VSM. The M8 switch was set off during measurement.

3. Irradiation

Sample TEGs were irradiated with 70 MeV protons at Cyclotron and Radioisotope Center (CYRIC), Tohoku University on June 26, 2006. The beam was about 5 mm full-width at half-maximum (FWHM) in size, which covered the TEG chip fully. Assuming an SCT environment in the SLHC operation [5], we planned to irradiate six chips each up to 0.1, 0.2, 0.5, 1.0, 2.0, and $5.0 \times 10^{15}\, n_{eq}/cm^2$. For a beam current between ~10 and ~300 nA, the irradiation time was in the range between ~10 and ~50 min. The samples were irradiated at room temperature with their terminals shorted using conductive sponge. The condition of terminals shorted does not necessarily correspond to the worst case for the radiation-induced damage. Irradiations with different bias conditions would be useful in future tests. The fluence was calculated later by measuring the Na24 product from the Al foil attached to each TEG chip. Unfortunately, the obtained fluence values turned out to about $\frac{1}{5}$ of those expected from the beam current and exposure time. The beam current was a measurement from a monitor located in the beam pipe upstream of the samples. The beam tuning was not appropriate inducing substantial loss hitting the beam flange. Finally, the obtained fluence values were 0.03, 0.05, 0.09, 0.2, 0.4, and $1.0 \times 10^{15}\, n_{eq}/cm^2$. The ionization dose to SiO_2 was 0.026 MGy (SiO_2) for 3×10^{13} 1 MeV n_{eq}/cm^2 and 0.85 MGy (SiO_2) for 1.0×10^{15} 1 MeV n_{eq}/cm^2, respectively.

Table 1
Transistor parameters

Transistor type	HVT, high-threshold basic logic	LVT, low-threshold analog	IO, high-threshold I/O
Voltage tolerance (V)	1.0	1.0	1.8
Gate oxide thickness (nm)	2.5	2.5	5.0
Minimum gate length (μm)	0.14	0.14	0.30
Threshold voltage (V)	0.4	0.2	0.5

Table 2
Transistor TEG types and sizes

Column ID	Transistor type	Gate width (μm)	Gate length (μm)
0	LVT	280	0.14
1	LVT	600	0.30
2	LVT	1000	0.50
3	HVT	280	0.14
4	HVT	600	0.30
5	HVT	1000	0.50
6	IO	600	0.30
7	IO	1000	0.50

LVT, low threshold; HVT, high threshold; IO, I/O transistors.

4. Results

The DC characteristics were evaluated before and after irradiation by measuring the drain current as a function of the gate-source voltage. V_{ds} was fixed to 0.5 and −0.5 V for N and PMOS DUTs, respectively. Due to a layout failure, all M2 switches are always on for the 1, 2, 4, 5, and 7 columns: four N and four P DUT transistors with the same type and size are connected in parallel in one column. Although distinction of N and P is possible by using corresponding terminals, the four DUT transistors cannot be measured individually. Since the difference among the four is whether body floating or body tied, and the results were almost identical among these in the data for 0, 3, and 6 columns, we regard those data as a sum of four

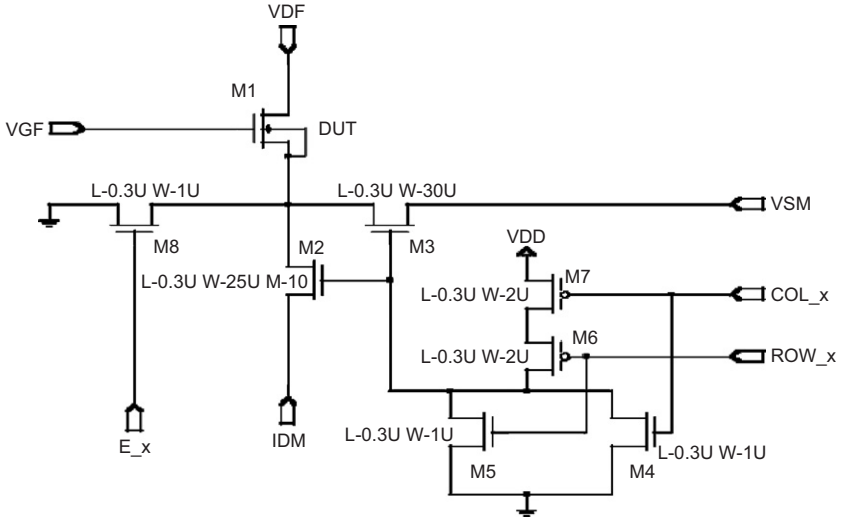

Fig. 3. NMOS transistor cell circuit.

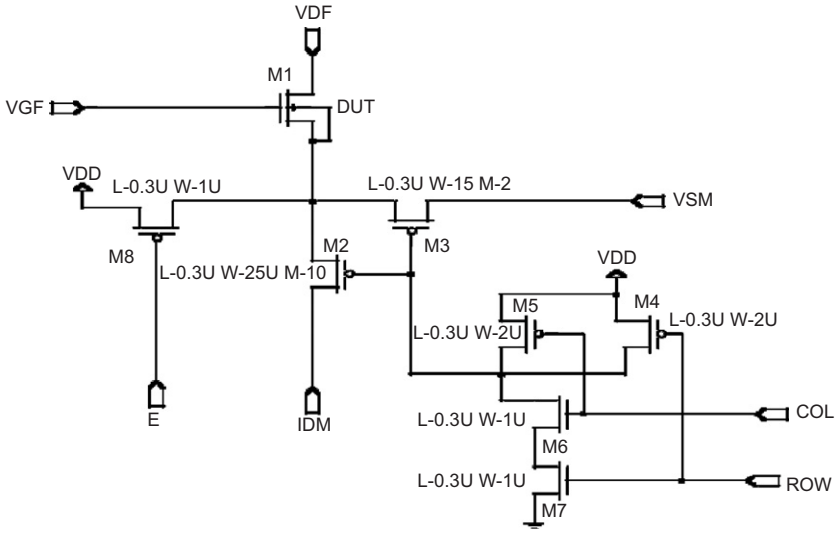

Fig. 4. PMOS transistor cell circuit.

transistors connected in parallel. The current corresponding to one transistor is obtained as one-fourth of the measured current.

Fig. 5 shows the I_{ds}–V_{gs} characteristics of typical NMOS transistors, LVT with body floating, before and after irradiation. The measurement relevant to the highest fluence is truncated at $V_{gs} = 0.5\,V$ due to current compliance. Since the threshold voltage decreases after irradiation, the drain current increases at the same V_{gs}. Only minor differences can be observed between curves relevant to different fluence values: they seem to be already saturated at the lowest fluence. A large increase in the leakage current to a 0.1 mA level is also seen in the sub threshold region. The leakage of the pre-irradiation samples shold be in the range of 10^{-8}A at $V_{gs} = 0\,V$ [2]. The observed large values are probably due to an influence from the leakage current of ESD protection diodes implemented in the TEG IO terminals.

Fig. 6 shows the I_{ds}–V_{gs} characteristics of typical PMOS transistors. The threshold voltage also decreases after irradiation. However, the drain current decreases, contrary to the NMOS transistors. No increase is seen in the leakage current in the sub-threshold region. In the case of PMOS transistors, slight fluence dependence can be seen. This could be attributed to incorrect VSM measurement, since on resistance of M3 PMOS switch rises with irradiation, and cannot be ignored with respect to the input resistor of the voltmeter (1 MΩ). On the other hand, in the case of NMOS transistors, VSM can be measured correctly, since there is no rise of the on resistance. In order to clarify this point, new TEG chips without having cell structure (transistor terminals will be led directly) will be designed for the next irradiation test.

The total dose damages are primarily explained [6] by radiation-induced charge buildup in the oxides. As the SOI-buried oxides are exposed to ionizing radiation, radiation-induced charges are trapped throughout the buried oxide. The trapped charges are predominantly positive. The FD-SOI transistors are sensitive to the trapped charges in the oxide layer and at the silicon/oxide

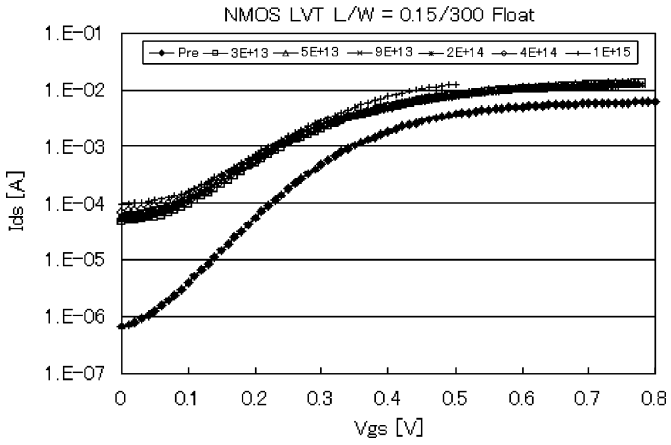

Fig. 5. I_{ds}–V_{gs} characteristics of typical NMOS transistors before and after irradiation.

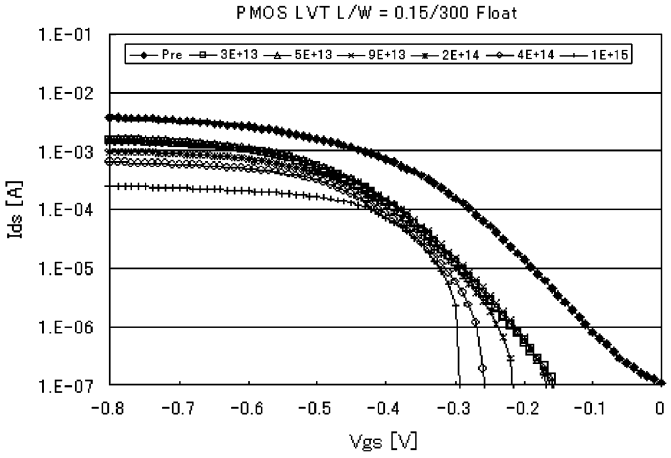

Fig. 6. I_{ds}–V_{gs} characteristics of typical PMOS transistors before and after irradiation.

interface, since the top-gate transistor is electrically coupled to the back-gate transistor. For NMOS transistors, charge trapping in the buried oxide decreases the top-gate threshold voltage. The oxide charges can invert the body at the oxide interface and increase the leak current of the back-gate transistors. This also affects the top-gate characteristics.

Fig. 7 summarizes the threshold voltage shift. The voltage reference is defined by V_{gs}, where ID = 500 μA. The threshold voltage shift is given by the difference of the references before and after irradiation. The threshold shifts are found to be about −0.1 V for NMOS (LVT) and PMOS (LVT, HVT), −0.2 V for NMOS (HVT), and −0.35 V for N and PMOS (IO), respectively. Since the gate oxide layer is thicker for IO transistors, the shifts are substantial.

Our results are compared with recent results from the bulk CMOS technology. According to Ref. [7], a 24 GeV proton irradiation test was performed for 0.13 μm bulk CMOS process transistors up to 10^{16} 24 GeV protons/cm^2. No threshold shift was observed for N-type CMOS transistors at the highest fluence. On the other hand, about 20 mV threshold shift was observed at the fluence of 2.0×10^{15} 24 GeV protons/cm^2 for P-type CMOS transistors. This fluence of 2.0×10^{15} 24 GeV protons/cm^2 is about twice higher than our highest fluence. Since the back-gate transistor does not exist in bulk CMOS, the threshold shift is considerably small compared with FD-SOI CMOS.

In order to reduce these large threshold shifts in the FD-SOI CMOS technology, compensation by the back-gate voltage is investigated for the TEG chip with largest fluence. Figs. 8 and 9 show the I_{ds}–V_{gs} characteristics for some back-gate voltages. The threshold shift compensation by biasing the back gate is shown in Fig. 10. Since we found only minor differences in the characteristics of transistors having different gate length, the results for the shortest gate length only are shown. The threshold of NMOS transistors decreases with the back-gate bias almost linearly. On the other hand, the threshold of PMOS transistors changes steeply in the region below −25 V. First, the threshold shift for NMOS (LVT) is recovered by biasing the back gate to about −20 V. Secondly, the threshold shift for NMOS (IO) and PMOS (LVT and HVT) is recovered by biasing the back gate to about −25 V. Lastly, the threshold shift for NMOS (HVT) and PMOS (IO) is recovered by biasing the back gate to about −30 V. We will check again in the next irradiation

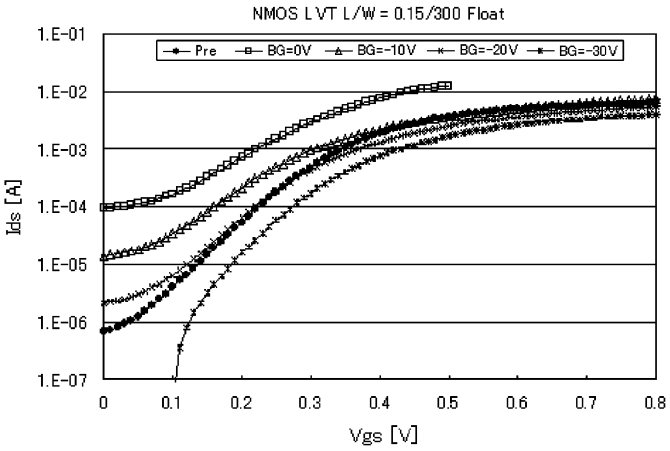

Fig. 8. I_{ds}–V_{gs} characteristics of typical NMOS transistors for some back-gate voltages.

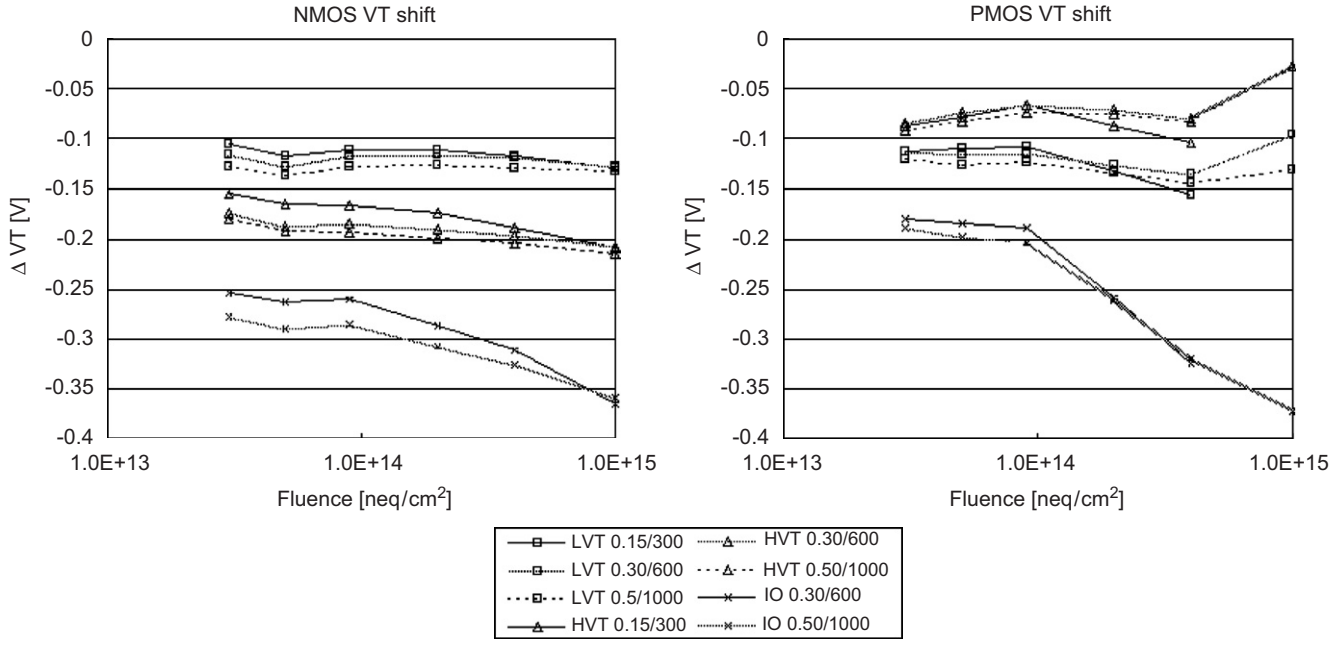

Fig. 7. Threshold voltage shift summary.

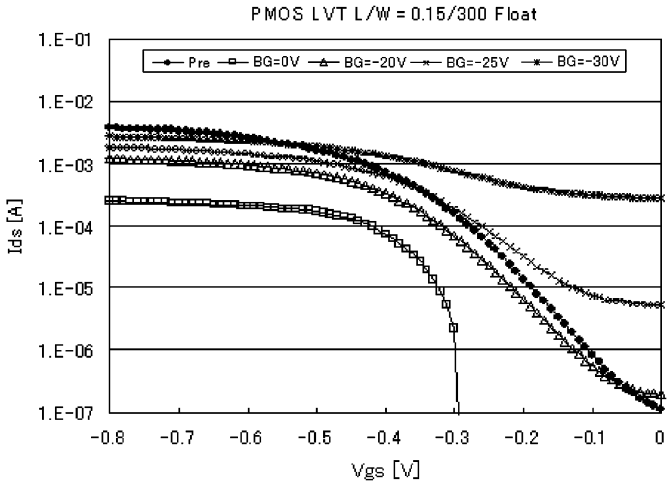

Fig. 9. I_{ds}–V_{gs} characteristics of typical NMOS transistors for some back-gate voltages.

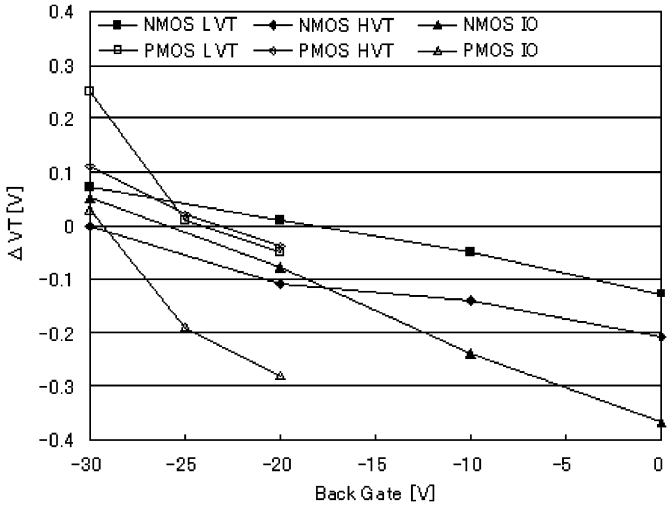

Fig. 10. Threshold shift compensation by back-gate voltage.

test, whether the difference among these compensation voltages is essential or not.

Fig. 11 shows the leak currents in the sub threshold region evaluated by the current at $V_{gs} = 0$ V. The optimal value of the back-gate bias is found to be about −20 V. It turns out that the optimal back-gate voltage for threshold shift compensation agrees mostly with the optimal value for the leak current. The leak current after compensation is of the order of 1 μA.

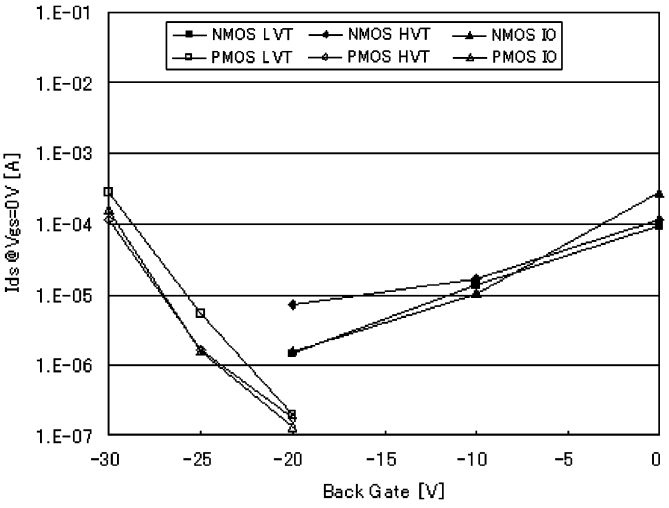

Fig. 11. Leakage current compensation by back-gate voltage.

5. Summary

We have irradiated OKI SOI CMOS transistors up to $1.0 \times 10^{15}\, n_{eq}/cm^2$. The threshold shifts are found to be about −0.1 V for NMOS (LVT) and PMOS (LVT, HVT), −0.2 V for NMOS (HVT), and −0.35 V for N and PMOS (IO), respectively. For the sample irradiated to $1.0 \times 10^{15}\, n_{eq}/cm^2$, compensation by biasing the back-gate was investigated, resulting that the threshold shifts are recovered at about −20 V for NMOS (LVT), −25 V for NMOS (IO) and PMOS (LVT, HVT), and −30 V NMOS (HVT), respectively.

We are planning a next irradiation test up to $5.0 \times 10^{15}\, n_{eq}/cm^2$. New TEG chips without having cell structure will be introduced in order to measure the detailed characteristic directly.

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