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Hybrid and module designs for ATLAS silicon tracker upgrade for super LHC

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Abstract

Based on the ATLAS SCT experience, hybrid and module designs of a short strip silicon detector for an upgraded ATLAS inner tracker for the super LHC have been pursued. At the super LHC, which provides 10 times more intense beam collisions than the LHC, the detectors envisage a very high rate operation in a much harsher radiation environment. Immediate concern is an increase of leakage current due to a radiation damage, which may induce a catastrophic break down of a thermal runaway. We have deduced a simple model for the thermal runaway, which can be conveniently utilized for the module designs. The thermal runaway model was verified by comparing with the corresponding FEM thermal analyses.

The upgraded module is structurally similar to the present SCT barrel module. Two rectangular sensors, each of $12.5 \times 6.4\,cm^2$, are sandwiched along with a thermo-mechanical baseboard to provide two-dimensional space points. A one-piece wrap-around hybrid bridged over the sensors serves both the top and bottom sensors. Mounting and cooling schemes also follow the present barrel SCT designs with necessary modifications and improvements.

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Keywords: Silicon strip detector; Thermal runaway; SCT barrel module; ATLAS tracker upgrade; Super LHC

1. Introduction

The module and service structure designs of the present ATLAS silicon tracker (SCT) have evolved as a result of a number of technical and performance considerations [1]. In pursuing a silicon strip detector design for an upgrade of the ATLAS inner tracker, it is imperative to carefully evaluate the technical and performance issues of the current SCT to understand how the current design can be modified to adapt to the super LHC that becomes ten-fold intense in luminosity than that of LHC [2].

Unlike starting from scratch, in order to avoid unnecessary hardship in the replacement, a new inner tracker has to follow many constraints not only an overall tracking volume but also cabling and cooling routes and dimensions set for the present inner tracker. A harsher radiation environment will introduce severe radiation damage on the module, particularly, a serious increase of leakage current. Therefore, the module needs to be carefully evaluated concerning thermal properties and cooling requirements.

2. Leakage current

One of the most critical issues is how to overcome ten times harsher radiation environment. Immediate concern in operating a silicon detector is an increase of the leakage current that is proportional to an accumulation of radiation [3]. The leakage current, which is estimated by taking a damage constant of 4×10^{-17} A/cm after annealing of 80 min at 60 °C or equivalently 14 days at 20 °C, is plotted Fig. 1 as a function of radiation fluence. The expected fluences in the inner tracker [4] are overlaid in the figure for the integrated luminosity of $3000\,fb^{-1}$ with a safety factor of 2. As the leakage current increases, a danger of starting a thermal runaway rises. The leakage

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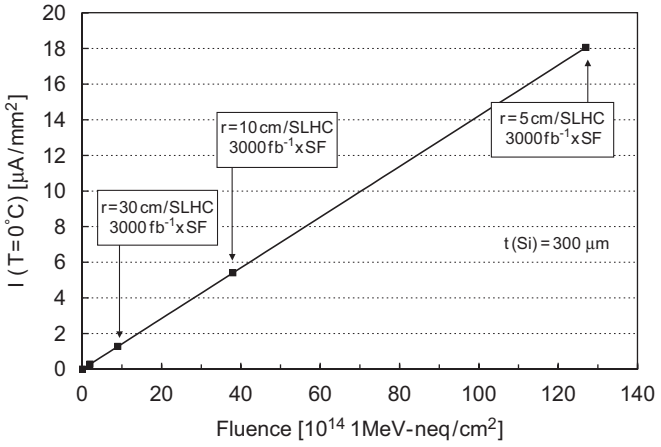

Fig. 1. Silicon sensor leakage current as a function of radiation fluence; the expected fluences with a safety factor (SF) of 2 are indicated in the figure for the integrated luminosity of 3000 fb^{-1} at various distances from the interaction point.

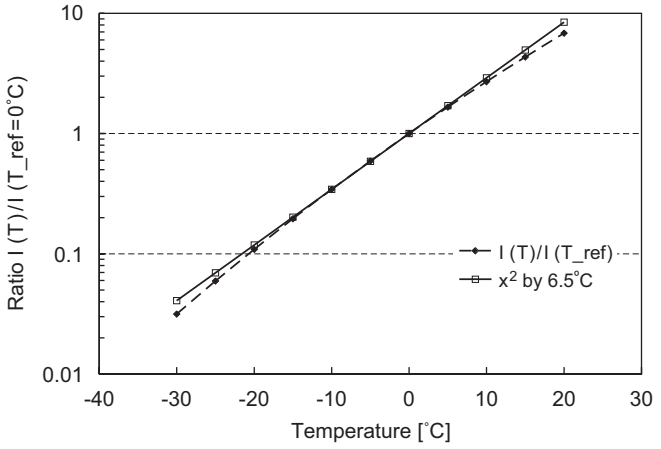

Fig. 2. Silicon sensor leakage current as a function of temperature: exponential dependence (filled diamond) and a simple exponent approximation (open square).

current also affects requirements to a HV power supply together with a front-end amplifier. At high fluence, in order to keep a good signal to noise ratio, the operating voltage may have to be raised as high as possible, e.g. 800 V, about twice that of LHC, requiring even more HV power capacity.

By lowering the temperature, however, the leakage current of the silicon detector can be rapidly reduced. The temperature dependence of the leakage current in silicon is formulated as in Eq. (1) in the next section [5] and is shown in Fig. 2, with a marker of $I(T)/I(T_{\mathrm{ref}}=0\,^{\circ}\mathrm{C})$. The leakage current changes by a factor of 2 as the temperature changes by 6.5 °C in the region around 0 °C. The silicon detectors for the super LHC need to be farther cooled by about 20 °C, $\Delta T=-20\,^{\circ}\mathrm{C}$, to keep the power in the silicon detectors at the same level of those for the LHC. Thus, by the leakage current requirement alone, the operating temperature for the super LHC becomes about −27 °C rather than −7 °C for the LHC.

3. Thermal runaway—simple model

An exponential rise of the leakage current as an increase of temperature invokes a catastrophic thermal behavior called thermal runaway, in which the module is heating up abruptly once it goes beyond some critical temperature. In a module design and its operation, an evaluation of this critical temperature is in prime importance.

Approximating the leakage current behavior,

$$I(T)=I(T_{\mathrm{ref}})(T/T_{\mathrm{ref}})^2\exp\{-E_{\mathrm{g}}/2k_{\mathrm{B}}(1/T-1/T_{\mathrm{ref}})\} \quad (1)$$

to a simple exponent function

$$\approx I(T_{\mathrm{ref}})2^{(T-T_{\mathrm{ref}})/T_{\mathrm{half}}} \quad (2)$$

where T_{ref} is an arbitrarily chosen reference temperature, we could easily deduce a thermal runaway condition and its scaling behavior. When the module is in operation at a bias voltage, V, it generates a heat, Q, caused by the leakage current, I,

$$Q=VI \quad (3)$$

the temperature of the module increases to T from the initial temperature T_0, with which the heat generation of the sensors is zero ($Q=0$). As illustrated in Fig. 3, this temperature rise,

$$\Delta T=T-T_0 \quad (4)$$

is proportional to the heat generation, Q, with the thermal resistance, R, as a coefficient. Therefore,

$$\begin{aligned}\Delta T &= RQ(T)\\ &= RVI(T)=RVI(T_{\mathrm{ref}})2^{(T-T_{\mathrm{ref}})/T_{\mathrm{half}}}\\ &= RVI(T_{\mathrm{ref}})2^{(\Delta T+T_0-T_{\mathrm{ref}})/T_{\mathrm{half}}}\\ &= RQ(T_{\mathrm{ref}})2^{(\Delta T+T_0-T_{\mathrm{ref}})/T_{\mathrm{half}}}\\ &= RQ(T_0)2^{\Delta T/T_{\mathrm{half}}} \quad (5)\end{aligned}$$

where we take $T_0=T_{\mathrm{ref}}$. Then,

$$\frac{RQ(T_0)}{T_{\mathrm{half}}}=\frac{\Delta T}{T_{\mathrm{half}}}2^{-\Delta T/T_{\mathrm{half}}}. \quad (6)$$

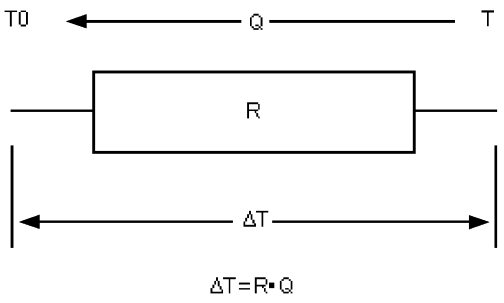

Fig. 3. Generated heat on the sensors, Q, introduces a temperature increase, ΔT, along the module which has a thermal resistance of R.

The function in R.H.S. has a single peak at

$$\Delta T = \frac{T_{\text{half}}}{\ln 2} \tag{7}$$

and the peak value is

$$\frac{T_{\text{half}}}{e \ln 2}. \tag{8}$$

Therefore, the thermal runaway condition is

$$Q(T_0)R \geqslant \frac{T_{\text{half}}}{e \ln 2}. \tag{9}$$

Using the T_{half} is 6.5 °C, numerically

$$\Delta T = 9.38\,^{\circ}\text{C} \tag{10}$$

and

$$Q(T_0)R = 3.45\,^{\circ}\text{C} \tag{11}$$

$$Q(T_{\text{ref}})R = 3.45 \times 2^{-(T_0 - T_{\text{ref}})/T_{\text{half}}}\,^{\circ}\text{C}. \tag{12}$$

From these we can immediately realize a kind of scaling behavior:

(1) Amount of temperature increase from the non-heating point to the runaway point is always the same as 9.38 °C, independent of the initial non-heating temperature.
(2) The tolerable heat can be doubled as the initial temperature is reduced by T_{half} of 6.5 °C. Fig. 4 demonstrates this scaling behavior. The top curve started at 0 °C and rose to the runaway point of 9.38 °C at $Q(T_{\text{ref}} = 0\,^{\circ}\text{C})R = 3.45\,^{\circ}\text{C}$, while the bottom one was able to tolerate up to twice $Q(T_{\text{ref}} = 0\,^{\circ}\text{C})R$ of 6.90 °C, as it started at the temperature which was lower by T_{half} of −6.5 °C.

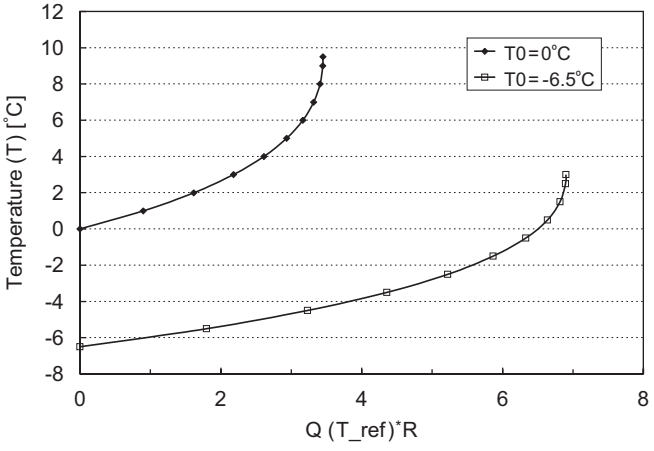

Fig. 4. Scaling behavior of the thermal runaway. The top curve (filled diamond) started at 0 °C and rose to the runaway point of 9.38 °C at $Q(T_{\text{ref}} = 0\,^{\circ}\text{C})R = 3.45\,^{\circ}\text{C}$, while the bottom one (open square) was extended up to twice $Q(T_{\text{ref}} = 0\,^{\circ}\text{C})R$ of 6.90 °C, since it started at the lower temperature by T_{half}: −6.5 °C.

4. Thermal analysis for SCT module

A FEA analysis can be used to understand a thermal behavior of the SCT module, thus deducing an average thermal resistance of the module. Once the thermal resistance is known, the simple runaway model can be utilized to look for an optimum condition, such as a cooling temperature and allowed heat generation, by making use of the scaling behavior.

The present SCT barrel module is made of four sensors, each of $64 \times 64 \times 0.3\,\text{mm}^3$. Shown in Fig. 5 is a drawing of the module. Pairs of the sensors are glued on the baseboard on the top and bottom surfaces. The baseboard (shaded area) is made from a highly thermal conductive TPG. One side of its extended ends is attached to a cooling pipe. The Cu/Polyimide flex-circuit-based hybrid with a pair of carbon-carbon plates for backing is wrapped around the sensor-baseboard sandwich. The hybrid populated with readout ASICs, which can be a potential heat source, is bridged over the silicon sensors and attached on the both ends of the baseboard.

A detailed three-dimensional FEA thermal analysis has been conducted with the ANSYS program [6] to the SCT barrel module. Results are plotted in Fig. 6 together with the simple runaway model calculations. The simple model calculations reproduce the thermal runaway quite well with somewhat conservative at the runaway point.

In order to develop a silicon tracker module for the super LHC, a two-dimensional model, which is a simple extension of the present SCT barrel module, is investigated by means of the ANSYS program. The module for the super LHC is expected to generate about 10 times more heat on the sensors, if operated at the same temperature. Furthermore, number of ASICs on the hybrid may become 48 (four rows of ASICs), rather than 12 (single row of ASICs) of the present module, resulting a heat generation of 24 W/module, 4 times larger than that of the present module, provided that the upgraded module has four sections of short strips (about 3 cm in length) on each side of the module for accommodating a super LHCs' high luminosity.

Relevant features and parameters used for the two-dimensional model analysis are summarized in the followings.

- Silicon sensor, width (w): 64 mm, thickness (t): 0.3 mm, thermal conductivity (k): 126 W/m/K.
- Baseboard (TPG1400), w: 88 mm, t: 0.4 mm, thermal conductivity in longitudinal ($k_{x,z}$): 1400 W/m/K, in transverse (k_y): 25 W/m/K.
- BeO facing, t: 0.25 mm, k: 280 W/m/K.
- Hybrid flexible circuit layer, t: 0.27 mm, $k_{x,z}$: 0.2 W/m/K, k_y: 1 W/m/K.
- Hybrid Carbon–Carbon backing, t: 0.3 mm, $k_{x,z}$: 650 W/m/K, k_y: 30 W/m/K.
- ASICs, area ($w \times t$): $6.55 \times 0.5\,\text{mm}^2$, 12/module with heat generation of 28 or 42 W/module.

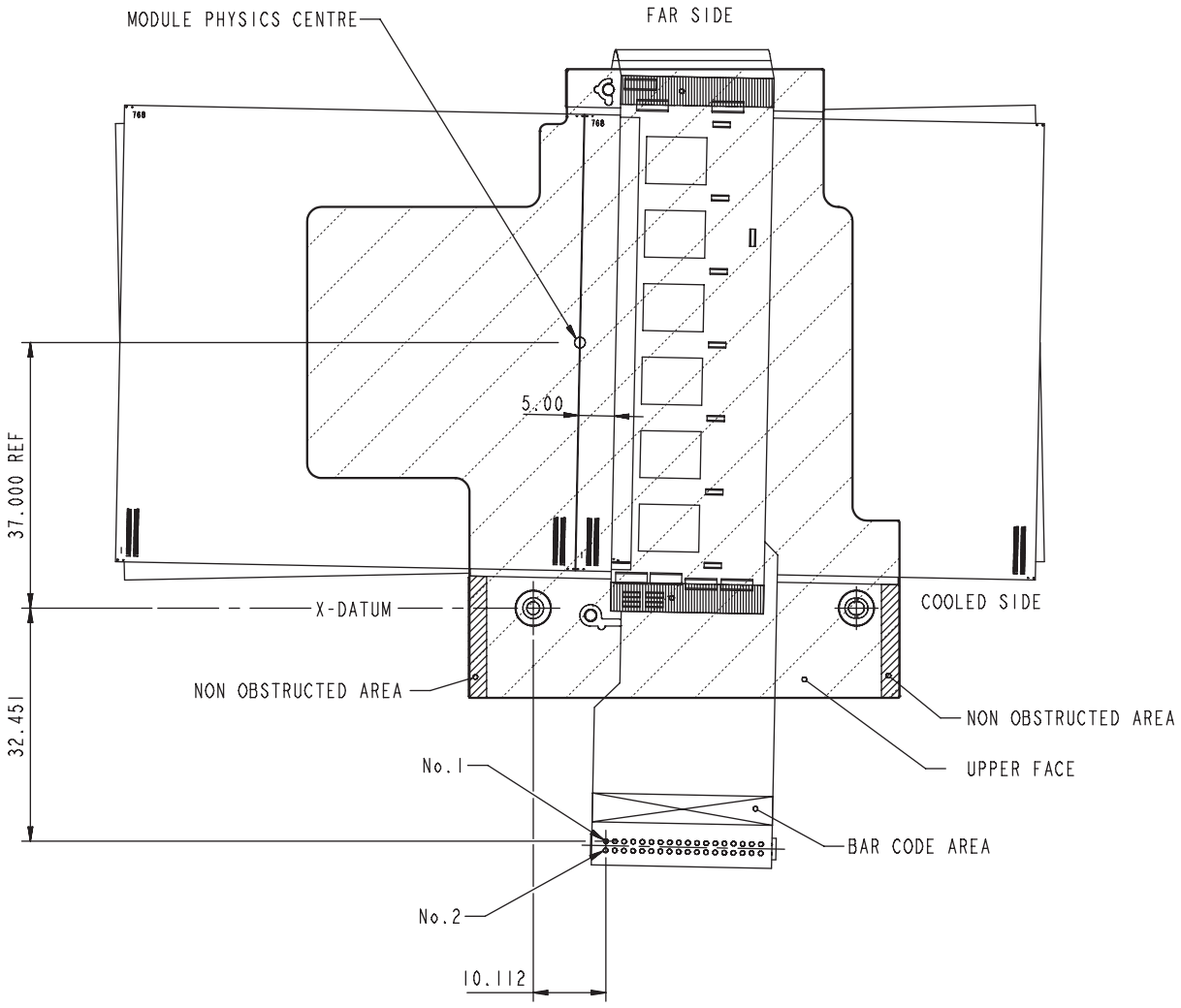

Fig. 5. Drawing of the present SCT barrel module.

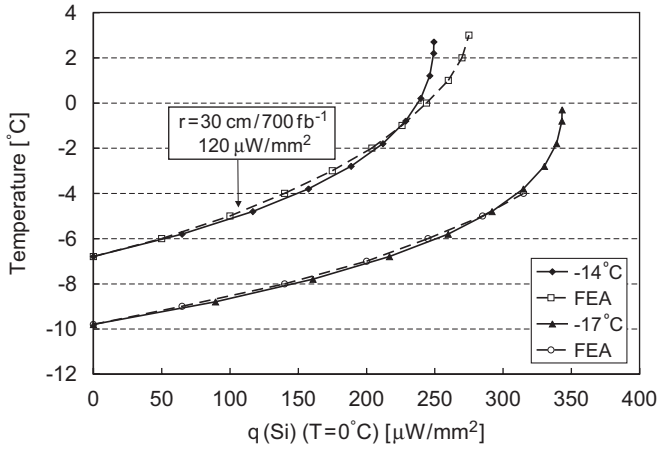

Fig. 6. Comparison of the detailed FEA analysis with the simple runaway model to the present SCT barrel module: cooling wall temperature at $-14\,^{\circ}C$ (FEA (open square), simple model (filled diamond)) and at $-17\,^{\circ}C$ (FEA (open circle), simple model (filled triangle)). Simple models are normalized to the temperatures at $q(\mathrm{Si}) = 0\,\mu W/mm^2$.

- Single end cooling using an aluminum conduit, 7 mm square with a 4 mm diameter hole for a coolant, k: 200 W/m/K.

Figs. 7 and 8 show results of the two dimensional ANSYS FEA analysis. Depicted in Fig. 7 is an isothermal contour of the module, while Fig. 8 shows a runaway behavior of the module in comparison with the simple runaway calculations. Three sets of curves (top, 2nd top and bottom) correspond to a different coolant temperature of -10 (open square), -15 (open circle) and $-30\,^{\circ}C$ (open triangle), with an ASIC heat of 28 W/module, respectively. An extreme case of six rows of ASICs, 42 W/module (third from top; filled diamond), is also shown in the figure. The simple model calculations (solid lines) agree quite well with the FEA analysis. Without sensor heat generation: $q(\mathrm{Si}) = 0$, module temperatures are already about $10\,^{\circ}C$ higher than the coolant temperature. This temperature offset is caused by the heat flux from the ASICs which

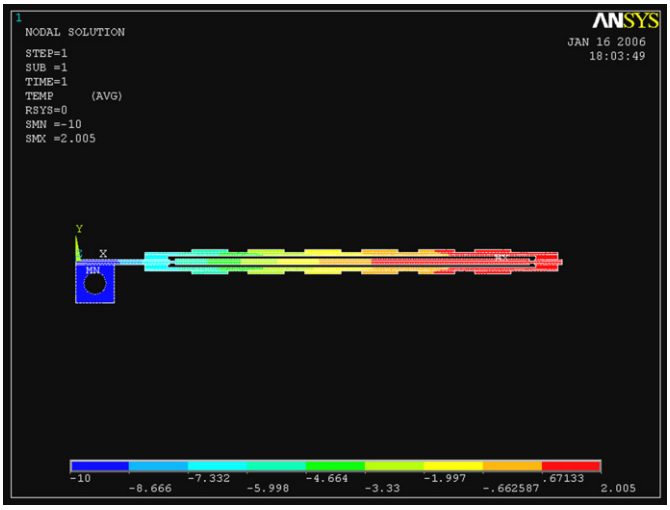

Fig. 7. Isothermal contour of the two-dimensional ANSYS FEA analysis.

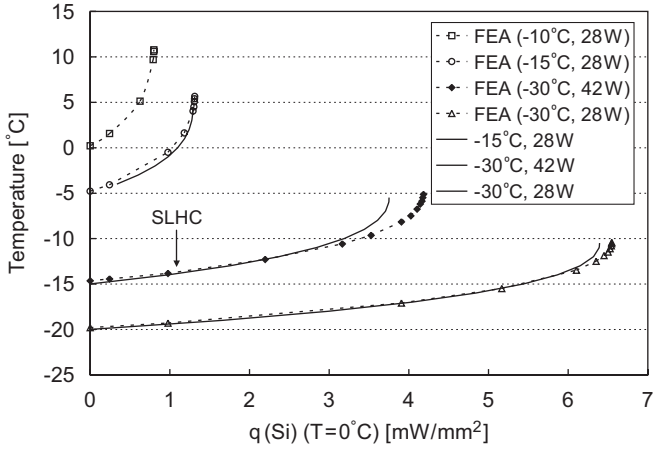

Fig. 8. Runaway behavior of the module analyzed with a two-dimensional ANSYS FEA in comparison with the simple runaway calculations: FEA analyses (dashed lines with markers) and simple calculations (solid lines). The nominal heat flux of the super LHC (1 mW/mm^2) is overlaid in the figure.

generate 28 W/module. After bearing a planned full term operation of 3000 fb^{-1} integrated luminosity, at 30 cm from the collision point in the super LHC, the silicon sensors' heat generation, with a contingency factor of two, reaches to 1000 μW/mm^2 at 0 °C, provided that the operating bias voltage is 800 V. The bottom curve in Fig. 8, which starts at −20 °C (coolant: −30 °C), shows the module is comfortably safe against the thermal runaway with a safety factor of more than 5. Concerning an actual operation, however, further requirement arises from the fact that the HV cables may not be upgradable, and we may need to keep the HV power as low as that of the present situation. This requires even lower operating temperature of about −27 °C to the sensor, therefore −37 °C to the coolant.

5. Short strip module

The silicon microstrip sensors for the ATLAS tracker at the super LHC can be fabricated from 6-in wafers. From a single 6-in wafer, one rectangular sensor of 12.47 × 6.37 cm^2 is laid out. Four sections of 3 cm strip elements are embedded in the single sensor. Two sensors are glued back-to-back on a thermo-mechanical baseboard, similar to the present SCT barrel modules.

A single wrap-around hybrid serves both the top and bottom sides. Since there are four sections of short strips in each sensor, the readout ASICs of four rows have to be populated on a single large area hybrid. The design of the hybrid with the four rows of ASICs is one of R&D issues, together with the engineering of cooling contacts, module fixation points, thermal managements with the baseboard design, and electrical connectivities.

Fig. 9 illustrates a basic concept of the four row ASICs hybrid with the wrap-around configuration. Although the available width for each row is narrower than the present one (also shown in Fig. 9), a redundancy scheme, which allows for skipping a failed chip and reading all healthy chips even with reduced number of master chips, should be accommodated. As illustrated in Fig. 10, the module is attached to the support

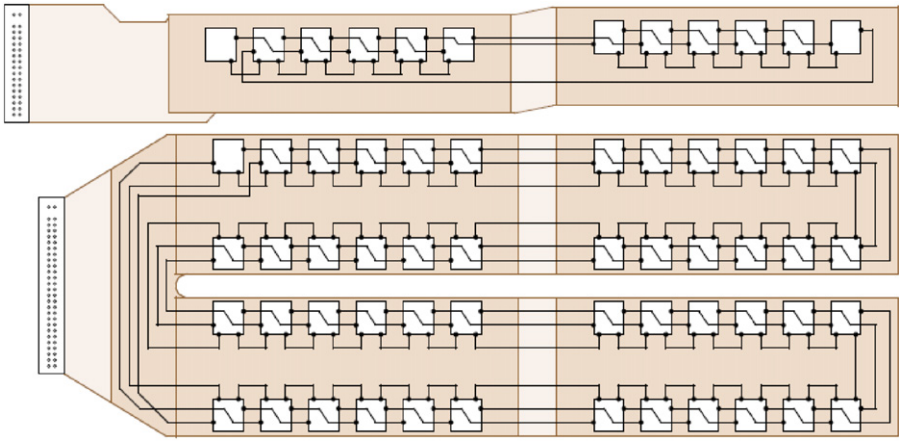

Fig. 9. Conceptual layout of the hybrid (bottom illust.) in comparison with the present one (top one).

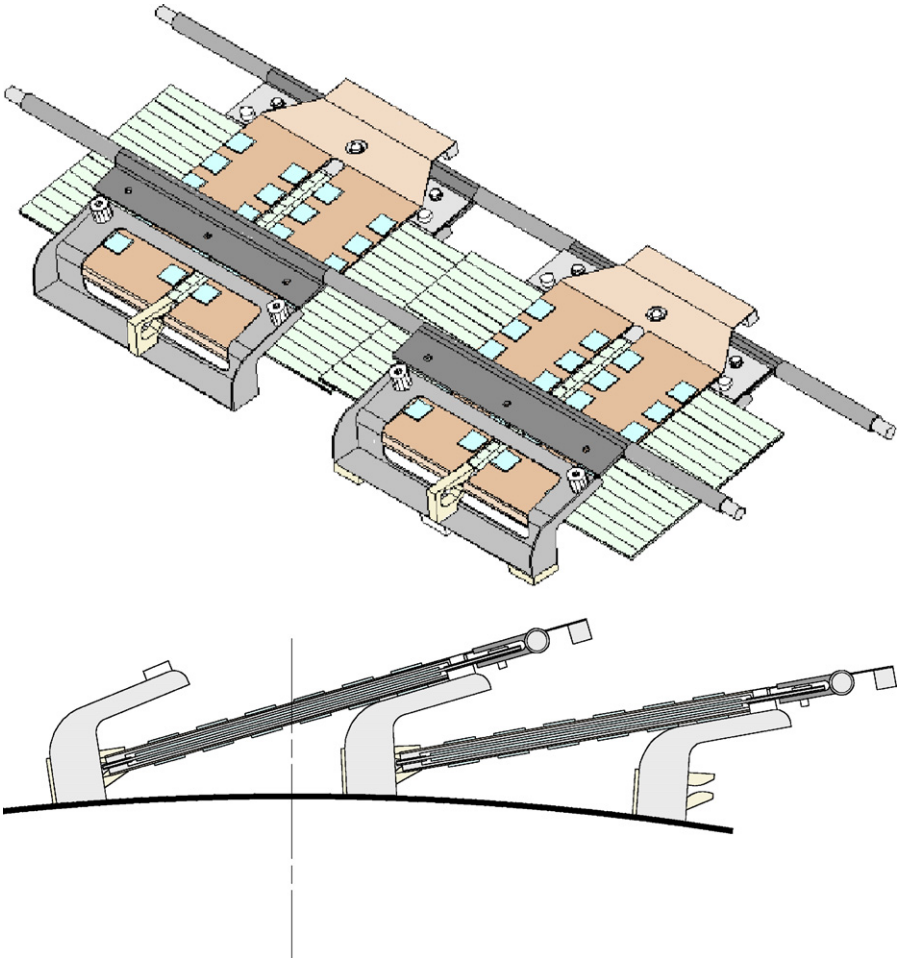

Fig. 10. Layout of the upgraded modules with a tilt angle of 16°.

cylinder by using a bracket with a tilt angle of 16° in order to match the Hall angle to gather electrons for the upgraded SCT, rather than holes for the present SCT.

6. Conclusions

We have proposed a silicon detector for the upgraded ATLAS central tracker for the super-LHC based on the present ATLAS SCT barrel module. While studying thermal properties of the module, we have come up with a simple runaway model which help us to understand thermal runaway, and thus to handle it rather conveniently. The two-dimensional ANSYS model, that represents a "full baseboard" module with a single-side cooling, shows a large safety margin against thermal runaway at a coolant temperature of −30 °C (sensor about −19 °C). It turns out, however, that the most imposing requirement to the module thermally is to keep the sensor power as low as the present SCT module. To this end, the temperature of the silicon sensors has to be kept at −27 °C or lower (coolant: less than −37 °C).

The size of $12.47 \times 6.37\,\mathrm{cm}^2$ sensor is obtained from a 6-in wafer. It can have four sections of 3 cm strips, about a quarter of the present SCT strip length. Such a short strips are needed to handle a high hit rate at the super LHC. Two sensors are glued back-to-back on a thermo-mechanical baseboard as just like the present SCT module. A large area hybrid with four rows of readout chips wraps around the sensor-baseboard sandwich. A single end cooling is sufficient with a comfortably large safety margin against thermal runaway.

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