Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research A 582 (2007) 861–865
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

R&D of a pixel sensor based on 0.15 μm fully depleted SOI technology

Toru Tsuboyama[a,*,1], Yasuo Arai[a], Koichi Fukuda[b], Kazuhiko Hara[c], Hirokazu Hayashi[b], Masashi Hazumi[a], Jiro Ida[b], Hirokazu Ikeda[d], Yoichi Ikegami[a], Hirokazu Ishino[e], Takeo Kawasaki[f], Takashi Kohriki[a], Hirotaka Komatsubara[b], Elena Martin[g], Hideki Miyake[h], Ai Mochizuki[c], Morifumi Ohno[b], Yuuji Saegusa[e], Hiro Tajima[i], Osamu Tajima[a], Tomiaki Takahashi[e], Susumu Terada[a], Yoshinobu Unno[a], Yutaka Ushiroda[a], Gary Varner[g]

[a]*KEK, High Energy Accelerator Research Organization, Japan*
[b]*OKI Electric Industry Co. Ltd., Japan*
[c]*University of Tsukuba, Japan*
[d]*JAXA, Japan Aerospace Exploration Agency, Japan*
[e]*Tokyo Institute of Technology, Japan*
[f]*Niigata University, Japan*
[g]*University of Hawaii, USA*
[h]*Osaka University, Japan*
[i]*Stanford Linear Accelerator Center, USA*

Available online 31 July 2007

Abstract

Development of a monolithic pixel detector based on SOI (silicon on insulator) technology was started at KEK in 2005. The substrate of the SOI wafer is used as a radiation sensor. At end of 2005, we submitted several test-structure group (TEG) chips for the 150 nm, fully depleted CMOS process. The TEG designs and preliminary results are presented.
© 2007 Elsevier B.V. All rights reserved.

PACS: 29.40.−n; 29.40.Gx; 29.40.Wk

Keywords: Monolithic pixel sensor; SOI CMOS technology

1. Introduction

SOI (silicon on insulator) is a process that fabricates CMOS circuitry atop a silicon-oxide layer (buried oxide, BOX) over a silicon wafer, as shown in Fig. 1. Since each transistor is isolated from the substrate and from each other, the circuit has smaller parasitic capacitance than a normal (bulk) CMOS LSI device, enabling faster and lower-power operation. For the same reason, such an SOI device shows much smaller susceptibility to single-event phenomena in high-energy physics or space applications. If we adopt a high-resistivity silicon wafer as the substrate and the signal induced in the substrate can be collected and processed by the CMOS circuit, SOI CMOS can be used as a radiation sensor. Pioneering work on this concept has been done by the SUCIMA [1] project, which successfully recorded minimum ionizing particle signals with such a device in a test beam. However, the process used is not compatible with sub-micron CMOS technology. The KEK Detector Technology Project [2] started its activity in 2005 and a monolithic-pixel detector subgroup, SOIPIX, has chosen the SOI technology of Oki Electric Co. Ltd., 150 nm fully depleted SOI CMOS process [3]. The merit of collaborating with a commercial LSI foundry is that the

*Corresponding author.
E-mail address: toru.tsuboyama@kek.jp (T. Tsuboyama).
[1]This research was partially supported by the Ministry of Education, Science, Sports and Culture, Grant-in-Aid for Scientific Research, 18204027, 2006.

0168-9002/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.nima.2007.07.111

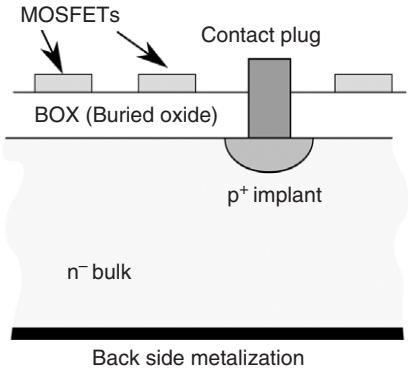

Fig. 1. Schematic view of an SOI CMOS device. p-type and n-type MOSFETs are fabricated on a buried oxide layer (BOX). The p^+ implant and contact plug is introduced in order to collect charge induced in the substrate.

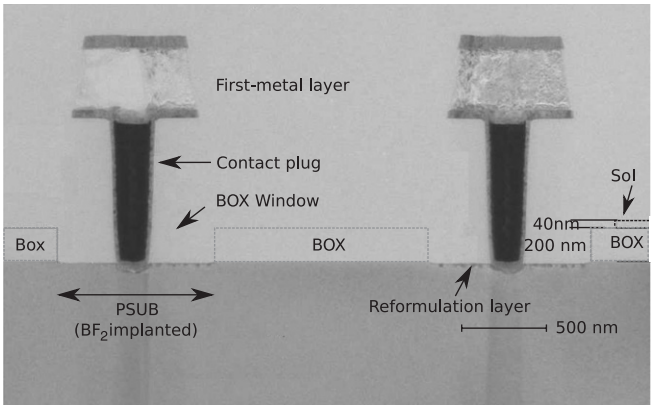

Fig. 2. Cross-section of the p^+ implant and the signal contact. A typical MOSFET is also shown. Borders of BOX and SOI are emphasized with dotted lines.

up-to-date technologies can be utilized in the device designs.

2. OKI FD SOI process

The SOI wafers are fabricated by SOITEC [4] by using their Smart-Cut technology [5]. The substrate is made from 650 μm thick, n-type FZ silicon. The resistivity of the substrate after silicon processing is measured to be about 700 Ω cm. The back side is thinned to 350 μm and sputtered with 200 nm thick aluminum. The thickness of the BOX layer is 200 nm. The CMOS transistor is made with 40-nm thick Cz crystal with a resistivity of 30 Ω cm. The thickness of the gate oxide is 2.5 nm. Five metal layers can be used in order to accommodate complex CMOS circuits. Because of the thin silicon layer, the FETs can be fully depleted at low gate voltage, which permits low-power operation. The nominal power supply voltage is 1 V. Fig. 2 is a SEM picture of the cross-section of the substrate contact. The area shown as 'BOX window' is etched out and ions are implanted through to the substrate. Then the area is filled with SiO_2 layer. The contact to the substrate is made later by the via holes and tungsten plugs.

3. Evaluation of test element group chips

Several test element group (TEG) designs were submitted to OKI in 2005. The designs and the results of subsequent evaluation are described in the following sections.

3.1. Strip-detector TEG

In order to measure the basic characteristics of the PIN diode in the SOI substrate, a strip-detector TEG was fabricated in a $2.5 \times 2.5\,mm^2$ chip. The chip is divided into eight regions. In each region, eight 460 μm long p-type

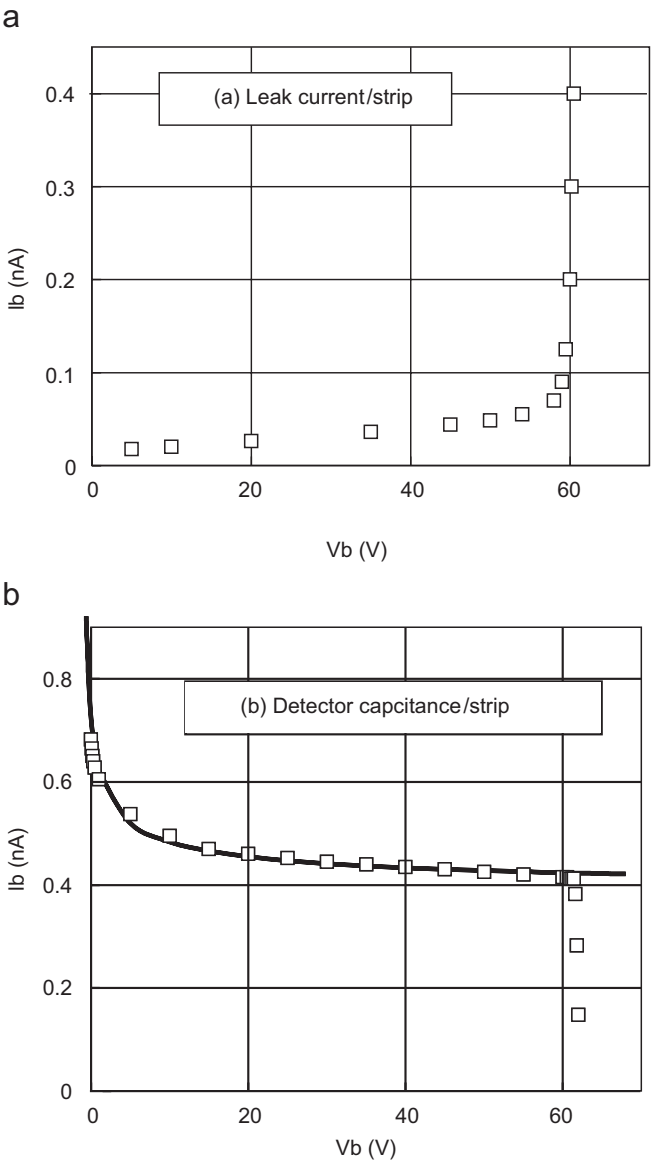

Fig. 3. The (a) *I–V* and (b) *C–V* characteristics of the strip-detector TEG. In (b) the measured data are plotted with white boxes. The solid line shows the result of fit.

implants are made in 50 μm pitch. There are regions with strip widths of 10, 20 and 40 μm. The I–V and C–V measurement is done for the 10 μm strip width (Figs. 3(a) and (b)). Four strips (every other strip) are connected parallel in the measurement. Value shown here is normalized for one strip. The breakdown voltage is found to be 60 V which is less than the expected full depletion voltage (~700 V). The observation with an infrared camera revealed the discharge takes place at the square corner of the strip implants. The solid line in Figs. 3(b) is fitted with $C = C_0 + \varepsilon S/W$, where C_0, ε, S and W represent offset capacitance, dielectric constant of silicon, area of strip coverage and depletion depth, respectively. If the resistivity of silicon is fixed to 700 Ω cm, the best fit is obtained with $S = 2 \times 50 \times 460\,\mu m^2$. This suggests the floating strips between measured strips fully contribute the C–V measurement through the inter-strip capacitance. The chip was then integrated into a readout system using an APV25 readout chip [6,7] and tested with a pulse laser. Every strip (50 μm pitch) is wire-bonded to an APV25 readout channel. The laser light ($\lambda = 890$ nm) is focused to diameter of σ~10 μm by a microscope and injected from top surface. The bias voltage dependence and laser position dependence of the observed charge are measured as follows. Charge collected by a strip is measured as a function of reverse bias voltage in Fig. 4(a). This charge is not saturated at the breakdown voltage of ~60 V, indicating the depletion region has not reached to the full substrate thickness.A laser spot is then scanned across several strips in 5 μm steps and the charge induced in the readout channels are recorded with the result shown in Fig. 4(b). The charge around the beam spot is reasonably distributed around the laser spot position. The dips around $x = 70$, 120 and 170 μm corresponds to the shadow of the readout metal traces. There are no strips for $x < 20$ μm.

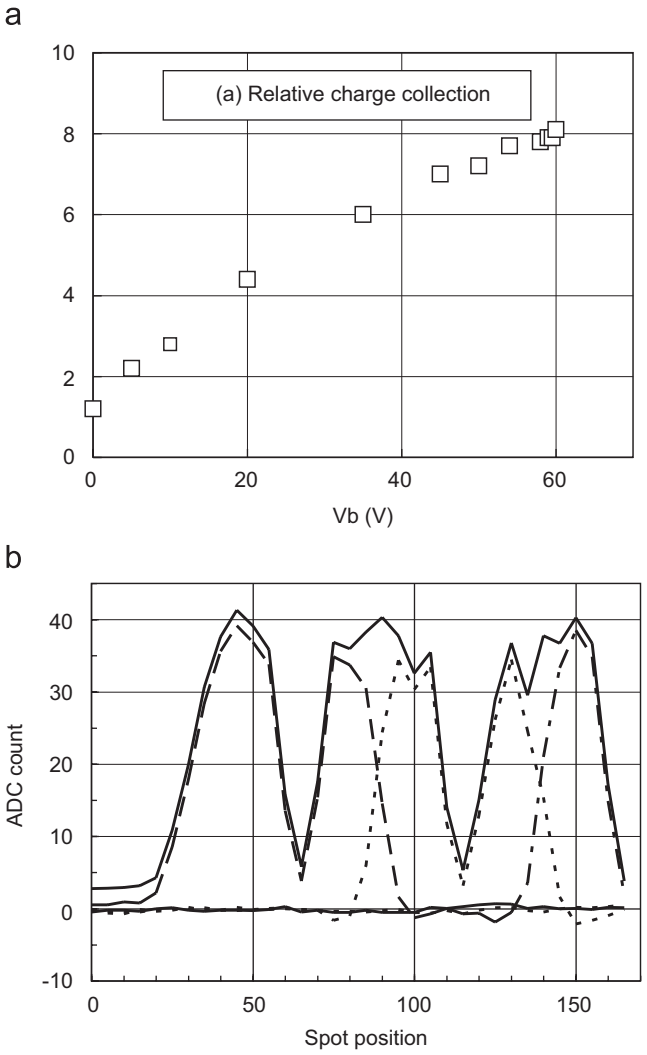

Fig. 4. Response of strip-detector TEG to a laser light ($\lambda = 890$ nm). (a) The output charge as a function of the detector bias voltage. (b) The result of a laser-position scan. The dashed, dotted and dot-dashed lines correspond to charge from the first three readout channels. The solid line shows the sum of the eight readout channels.

3.2. Pixel-type structure

A 32×32 matrix of $20 \times 20\,\mu m$ pixels is integrated on a $2.5 \times 2.5\,mm^2$ chip in order to examine the potential of the SOI as a radiation sensor [8]. Fig. 5(a) shows the magnified view of a pixel. Signal induced in the substrate is picked up with four octagonal shape $4 \times 4\,\mu m^2$ p-type implants. The aperture at the center is used for light illumination. Four implants are connected in parallel and read out with a front-end circuit as shown in Fig. 5(b). Charge induced in the p–n junction (D) is observed through source-follower by $M2$. $M1$ works as a protection diode for the gate of $M2$. Charge accumulated due to leakage current at the input is periodically reset by $M0$. $M4$ and C_s work as a track and hold circuit while $M3$ is used to discharge C_s. The analog output is multiplexed by $M5$ and $M6$ and recorded using an analog-to-digital converter. The breakdown voltage of the p–n junction is found to be about 100 V. However, because of the back-gate effects, explained later, the evaluation of the pixel TEG is done at 10 V bias voltage. Fig. 6(a) shows an image obtained with a 670 nm laser and a photomask. Several channels insensitive to light or saturated without light were identified in this laser light test. The mechanism of such a failure is under investigation. Fig. 6(b) shows the response of a pixel channel to a β-ray source (^{90}Sr) as a function of time. The channel is reset repeatedly and the analog output is observed with an oscilloscope. The size of the voltage step, corresponding to the charge induced by the β-ray deposition, is consistent with the expected depletion depth (44 μm) and the detector capacitance (8 fF).

3.3. Other test structures

In the circuit TEG, combinations of high-sensitivity preamplifiers and time-over-threshold circuits are

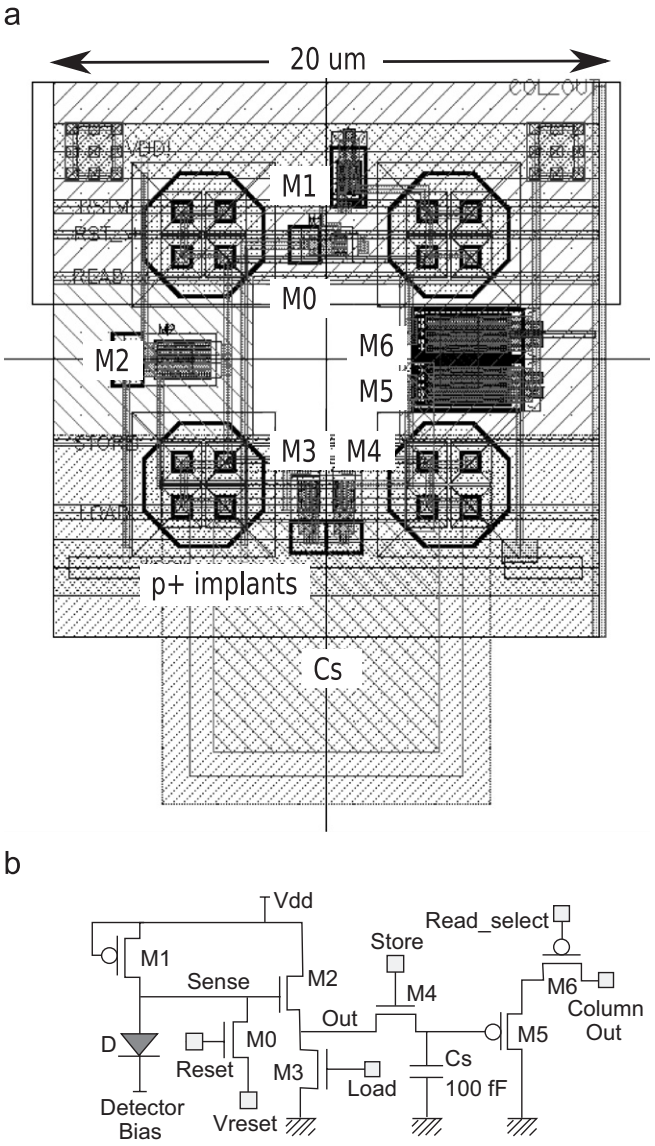

Fig. 5. (a) Detail view of a pixel. The 100 fF metal–insulator–metal capacitor overlaps to the neighbor cell. (b) Schematic of the front-end circuit within each pixel.

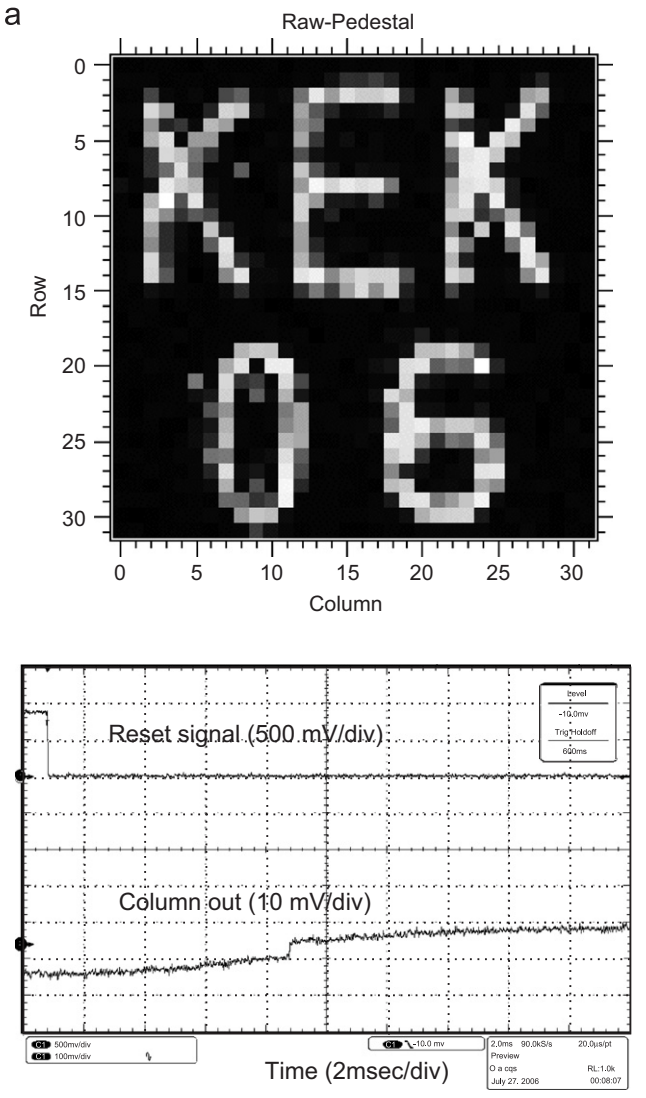

Fig. 6. (a) Image observed by PIXELTEG. The laser light ($\lambda = 670$ nm) is injected to the sensor through a photomask. (b) The response of a pixel to a β source. The full scale of the horizontal axis is 20 ms. The unit of vertical axis is 500 mV/div for "Reset" (upper curve) and 10 mV/div for "Column out" (lower curve). The lower curve shows non-linearity in time, this is because the integration time is much larger than the designed dynamic range of the front-end circuit shown in (b).

implemented. As a low-threshold, fully depleted CMOS circuit has not been widely used, this trial is important to develop analog circuits with large dynamic range [9]. The circuits work well. The minor errors in the circuit design are understood and will be fixed in the next submission. The radiation TEG is an array of MOSFET transistors with various design parameters. Several chips have been irradiated in a proton beam and radiation tolerance is measured [10]. Another type of pixel sensor is designed for use in an imaging hard X-ray Compton polarimeter in space [11].

4. Back-gate effect and TCAD simulation

In the SOI sensor, bias voltage is applied to the substrate in order to establish the necessary depletion layer. The potential induced in the substrate could affect the operation of the SOI MOS transistors through the BOX dielectric (back-gate effect). Due to lower resistivity than is usual for a detector-grade substrate, higher voltage is necessary to obtain the depleted thickness. The back-gate effect can be controlled with a ring-shaped p-type implant in the substrate (guard ring) around the MOSFET. In order to limit silicon processing iterations, a simulation study was done to optimize the guard-ring structure. Silicon-processing and device simulations have been performed using two TCAD (technology CAD) systems: ENEXSS [12], which is a newly developed TCAD system intended for 3-D simulations, and Silvaco [13]. In order to study the back-gate effect, the characteristics of an n-type

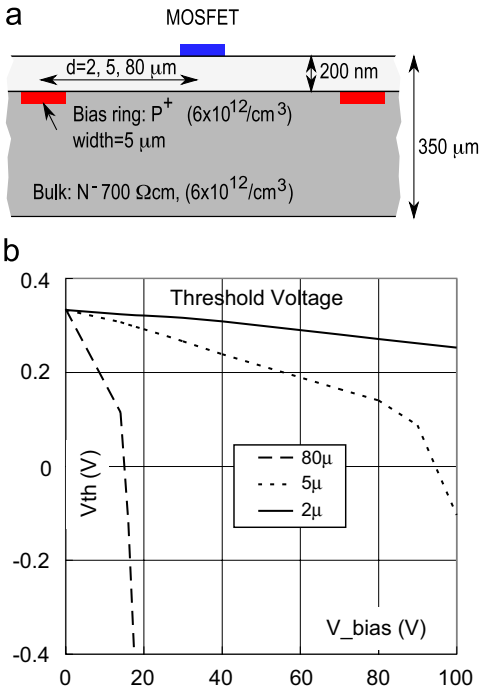

Fig. 7. (a) The simulation condition of TCAD. (b) Result of the device simulation. Solid, dotted and dashed curves correspond to the gate threshold voltage of the MOSFET for the case where the guard-ring implant is placed 2, 5 and 80 μm, respectively.

MOSFET are simulated with a bias voltage V_b in the substrate, as shown in Fig. 7(a) using ENEXSS in 2-D mode. Below the BOX, a p-type guard ring is implanted at a distance, d, whose potential is fixed to the voltage of the source of the MOSFET. The gate threshold voltage of the MOSFET is calculated for $0 < V_b < 100$ V and for distance d at 2, 5 and 80 μm. The result is shown in Fig. 7(b). If we allow a threshold voltage shift of 0.1 V, a bias voltage of 90, 15 and 1 V can be applied to the backside of the substrate for $d = 2, 5$ and 80 μm, respectively. We conclude the SoI pixel sensor works at 90 V bias voltage if proper guard rings are prepared around MOSFETs.

5. Summary

The R&D effort toward a pixel sensor based on 150-nm SOI CMOS technology started in 2005. Several TEG chips are processed and evaluated in 2006. With STRIPTEG, the characteristics of the SOI wafer as a radiation sensor is examined and it is confirmed that the substrate works as a position sensitive detector. Using the 32 × 32 array of 20 μm × 20 μm pixel sensor, we observe charge induced by laser light and by minimum ionizing particles. The TCAD simulation shows that, if proper guard rings are prepared around MOSFETs, the SOI circuit can be operated up to 90 V reverse bias voltage in the substrate. As we confirmed the possibility of the SOI technology as a radiation sensor, the R&D will be continued to achieve pixel sensor for real applications.

Acknowledgments

The authors wish to thank F. Takasaki, T. Kondo and J. Haba for their support to this project. We are also grateful to Y. Sugimoto and K. Hirose (JAXA) for their fruitful discussions.

References

[1] W. Kucewicz, et al., Nucl. Instr. and Meth. A 541 (2005) 172.
[2] ⟨http://rd.kek.jp/index.html⟩.
[3] A. Uchiyama, et al., IEEE Trans. on Electron Dev. 49 (2006) 2296.; K. Morikawa, Y. Kajita, M. Mitarashi, Oki Tech. Rev. 196 (2003) 61 ⟨http://www.oki.com/en/otr/196/downloads/otr-196-R15.pdf⟩.
[4] SOITEC, Silicon-On-Insulator Technologies, SA. ⟨http://www.soitec.com⟩.
[5] G.K. Celler, S. Cristoloveanu, J. Appl. Phys. 93 (2003) 4955.
[6] M.J. French, et al., Nucl. Instr. and Meth. A 466 (2001) 359.
[7] ⟨http://wwwhephy.oeaw.ac.at/u3w/f/friedl/www/belle/apvdaq_reference_v0.03.pdf⟩.
[8] Y. Arai, et al., IEEE Nuclear Science Symposium, Conference Record, N34-4, 2006.
[9] H. Ikeda, et al., Nucl. Instr. and Meth. A 579 (2007) 701.
[10] Y. Ikegami, et al., Nucl. Instr. and Meth. A 579 (2007) 706.
[11] H. Tajima, et al., IEEE Trans. Nucl. Sci. NS-52 (2005) 2749.
[12] ⟨http://www.tcad-international.com/ENEXSS_e.html⟩.
[13] ⟨http://www.silvaco.com/⟩.