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A silicon strip module for the ATLAS inner detector upgrade in the super LHC collider

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ABSTRACT

The ATLAS detector is a general purpose experiment designed to fully exploit the discovery potential of the Large Hadron Collider (LHC) at a nominal luminosity of $10^{34}\,cm^{-2}\,s^{-1}$. It is expected that after several years of successful data-taking, the LHC physics program will be extended by increasing the peak luminosity by one order of magnitude. For ATLAS, an upgrade scenario will imply the complete replacement of the Inner Detector (ID), since the current tracker will not provide the required performance due to cumulated radiation damage and a dramatic increase in the detector occupancy.

In this paper, a proposal of a double-sided silicon micro-strip module for the short-strip region of the future ATLAS ID is presented. The expected thermal performance based upon detailed FEA simulations is discussed. First electrical results from a prototype version of the next generation readout front-end chips are also shown.

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1. Introduction

A luminosity upgrade of the LHC (Super LHC or SLHC) up to $10^{35}\,cm^{-2}\,s^{-1}$ is planned for $\sim$2020. The expected integrated luminosity per experiment of $\sim 3000\,fb^{-1}$ will improve the precision in different measurements within the Standard Model; it will also enlarge the discovery region of particles predicted by some supersymmetric theories and enhance the sensitivity to low-rate phenomena inaccessible at the LHC energy scale [1].

The detectors will suffer of an increase in the number of proton–proton interactions per bunch-crossing to $\sim$400 (depending on the sLHC final bunch-spacing configuration). A completely new inner tracker for ATLAS is needed, with as basic requirements in terms of design being radiation hardness and efficient tracking capabilities with detector occupancies under control (few percent). Although the final layout has not been decided yet, most probably the tracker will be an all silicon-system with new detector technologies and increased granularity. The current design of the barrel region has four pixel layers at inner radii; five strip layers (three short and two long-strip layers) cover the outer radii. Detailed Monte Carlo simulations with signatures heavily dependent on the silicon tracker are currently under study to determine the layout for best performance.

For the strip region, the baseline layout relies in the so-called stave-concept, in which flex-hybrids holding the front-end electronics are directly glued to the silicon sensor. A bus tape underneath the detectors carries the required lines for control and readout of the digital signals [2].

Based on the experience of the current ATLAS Semiconductor Tracker (SCT), an alternative approach to that of the stave is being investigated. A double-sided silicon strip-module is proposed as the minimal modular unit to be assembled into larger structures. A local support structure for 12 modules enabling full coverage in both ϕ and Z for the barrel region is being developed.

2. Module design

The double-sided module proposed for the short-strip region of the upgraded ID is largely inspired in the current (barrel) SCT

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module. It consists of (see Fig. 1) two silicon microstrip sensors glued to a Thermo-Pyrolitical-Graphite (TPG) baseboard, four bridged-hybrids (each holding two rows of 10 front-end ASICS) located in pairs on both sides, four AlN facings and six washers (two for precision mounting and four screws). The prototype detectors [3,4] are $\sim 10 \times 10\,\text{cm}^2$ single-sided n-on-p detectors, with 1280 channels and 74.5 μm strip-pitch. The sensor integrates axial and stereo strips in the same wafer so that the 3D space-point (used during the pattern-recognition phase of track reconstruction) is naturally created by gluing identical but 180°-rotated wafers on the top and the bottom side.

2.1. Front-end electronics

The current prototype of the front-end chip for the short strip region (ATLAS Binary Chip Next or ABCN) has been produced in 0.250 μm IBM CMOS6 technology (so-called ABCN25) [5,6]. The ASIC implements a binary readout architecture for 128 channels and includes both analog and digital stages. Fig. 2 shows the block diagram of the chip.

On the analog side, it comprises preamplification, shaping and differential discrimination. A serial regulator can provide the analog voltage from a unique power source and two types of shunt-regulators allow to test different powering schemes. The ASIC has been designed to work with either positive or negative signal polarities decoupling the front-end (FE) from the chosen sensor technology.

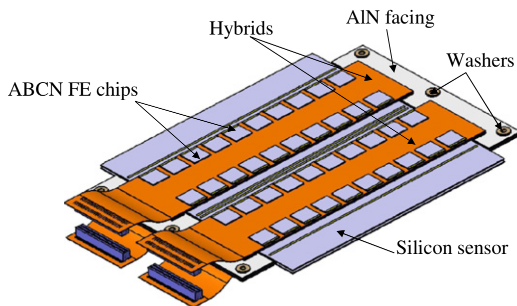

Fig. 1. Double-sided silicon micro-strip module concept.

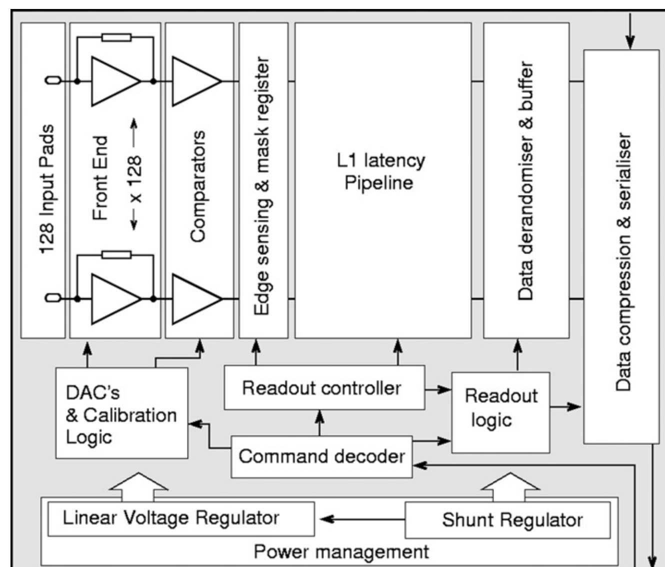

Fig. 2. Block diagram of the ABCN25 front-end chip.

The main digital blocks are input register, pipeline, derandomizer buffer, command decoder, readout buffer and data compression logic. The length of the digital pipeline is 256 bits or 6.4 μs latency time. A two-clock scheme allows to readout the chip at higher frequencies (80 MHz) than the main Bunch-Crossing (BC) clock. In the so-called *double-clock mode*, the output data rate is 80 Mbps. Additionally, the ABCN allows read/write operations in all registers, implements Single-Event-Upset (SEU) detection and token/data passing mechanism.

2.2. Hybrid development

Hybrids are kapton multi-layer flex circuits holding the FE ASICS. Two hybrid designs have been successfully developed by the University of Liverpool [3] and KEK [7]. In both cases, 20 ABCN25 chips are arranged in two columns of 10 (see Fig. 3).

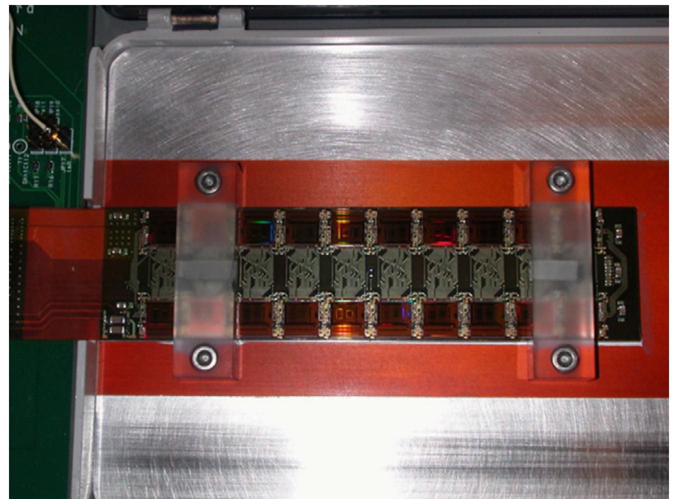

Fig. 3. Picture of a fully populated KEK hybrid.

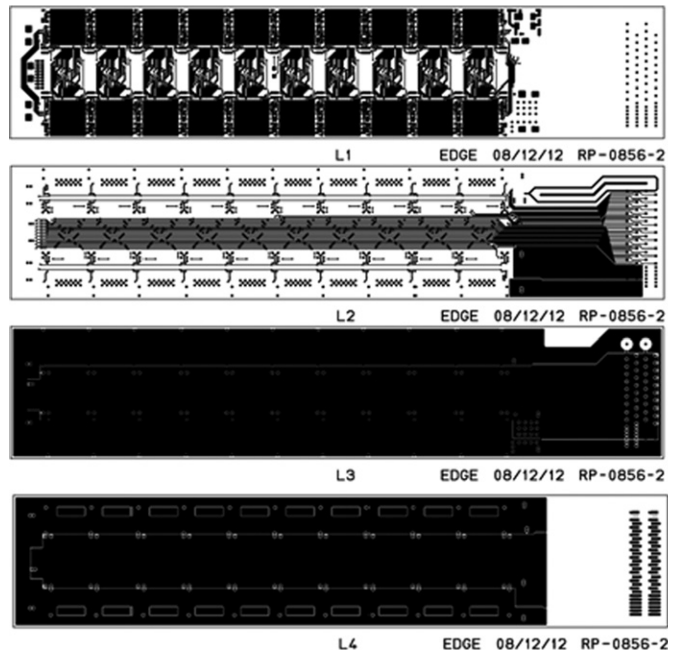

Fig. 4. Layout of the KEK hybrid. The four circuit layers are labelled L1 (top) to L4 (bottom).

In the case of the KEK design, the hybrid is composed of two double-sided flexible polyamide sheets with four circuit layers (see Fig. 4). Each polyamide sheet is 25 μm thick with a 12 μm thick laminated Cu layer on both surfaces. L1 includes the main circuit lines with redundancy lines incorporated in L2. L3 and L4 are intended for power distribution and grounding, respectively. A 0.8 mm pitch miniature connector is mounted at one end of the circuit layers for routing the LVDS signals.

A $400\times100\,\text{mm}^2$ carbon–carbon (CC) sheet underneath the flex circuit is designed to bridge over the silicon sensor avoiding any interference with the detector surface. The CC bridge, with a large thermal conductivity of 1400 W/m K, transfers the heat generated by the readout chips to the heat sink located at the bridge legs. The hybrid dimensions are 136 mm $\times$ 28.0 mm $\times$ 0.260 mm, with a total weight (excluding electrical components) of 4.25 g, equivalent to 0.00425 X_0 radiation lengths.

3. DAQ and first electrical results

The Data Acquisition (DAQ) system used in this paper is ABCNIDAQ [8], based on commercial components from National Instruments (NI) and specially developed for testing ABCN chips. The well-known SCTDAQ system [9], used for the characterization of SCT modules (equipped with the ABCD3TA chips [10]) was also adapted for ABCN and is being used by other groups [2].

ABCNIDAQ uses the high-speed (200/400 MHz in single/double data-rate mode) NI PCI/PXI 6562 card, with 16 digital channels for interfacing LVDS signals. The software has been written in LabVIEW, with an object-oriented design and chip configuration parameters stored in XML files. Scripted-generation and multi-record acquisition are used to speed-up the data transfer.

The ABCN ASIC has an internal calibration circuit which allows the simulation of a hit in a strip by the injection of test charges of selectable amplitude (up to 10.2 fC equivalent charge). An individual threshold correction per channel is implemented with a 5-bit DAC (TrimDAC) in order to compensate for possible deviations in the threshold offsets, optimizing the uniformity across the chip. The range of the TrimDAC is set by three bits in the configuration register, with 32 available steps within a given range value.

After setting the optimum value of the delay between the injection pulse with respect to the clock signal for each chip, a

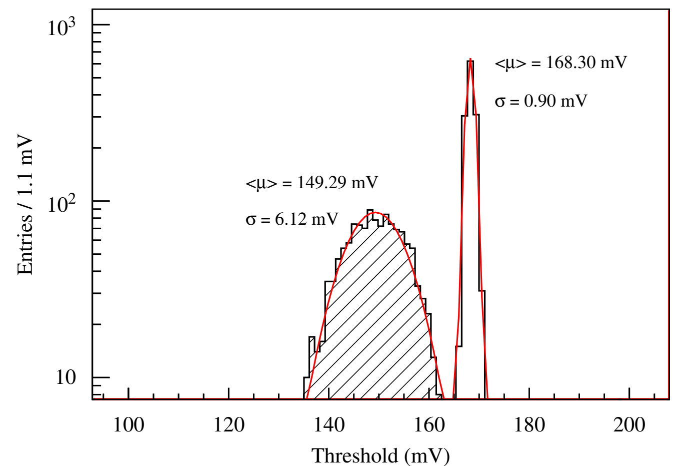

Fig. 6. Distribution of vt50 threshold points before trimming (dashed histogram) and after trimming (empty histogram) for all channels in one hybrid column. The mean $\langle\mu\rangle$ and sigma σ from a Gaussian fit to each distribution are also shown.

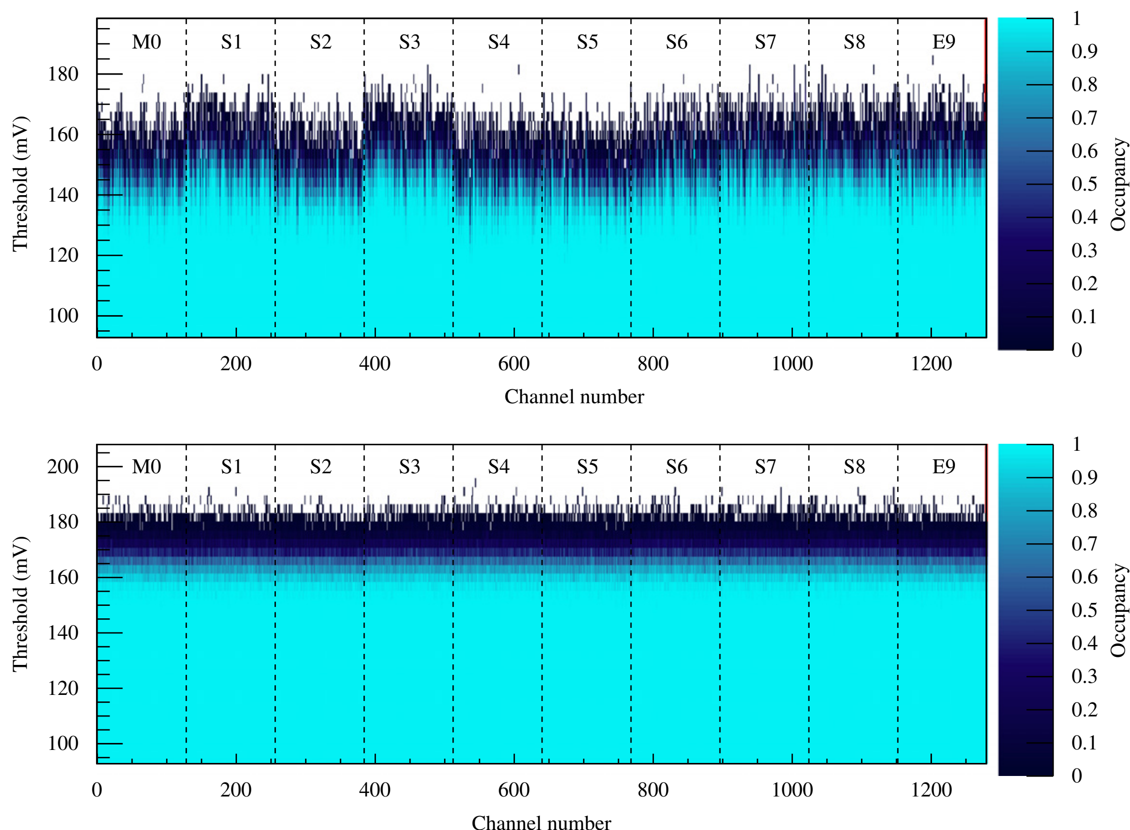

Fig. 5. Threshold scan for a 1.5 fC input charge before trimming (top) and after trimming (bottom). Only results from one column of 10 chips (see Fig. 3) are shown.

trimming procedure to correct the deviations of each channel threshold offset is performed. Fig. 5 shows the results of a threshold scan in a fully populated bare hybrid before and after trimming. For a given input charge (1.5 fC in this case), the differential threshold is varied, a certain number of triggers are sent and the occupancy in each channel is computed. All chips have been trimmed to the same range, resulting in a very uniform distribution across all channels.

From the projection of the occupancy plots to the threshold-axis, the threshold corresponding to 50% occupancy is obtained for each channel (so-called vt50 point). Fig. 6 shows the distribution of vt50 points for all channels of one column of bare hybrid before and after the trimming procedure. The threshold spread is reduced from $\sim$6.1 to $\sim$0.9 mV.

By performing threshold scans for several input charges, the gain and noise at the discrminator input can be determined (three-point gain scan). Fig. 7 shows the resulting distributions of gain (mV/fC), offset (mV), output noise (mV) and corresponding input noise (Equivalent Noise Charge or ENC) as a function of channel number. The results show an excellent agreement with the gain specification of 100 mV/fC and the estimated noise value of $\sim$400 ENC for the ABCN chip.

The hybrids have also been tested in double-clock mode, with the slow 40 MHz BC clock signal being generated on one of the output channels of the 6562 card. No significant differences in terms of analog performance have been observed.

4. Thermal simulations

Thermal performance is a key aspect of the module design since the silicon sensors are affected by radiation. Radiation

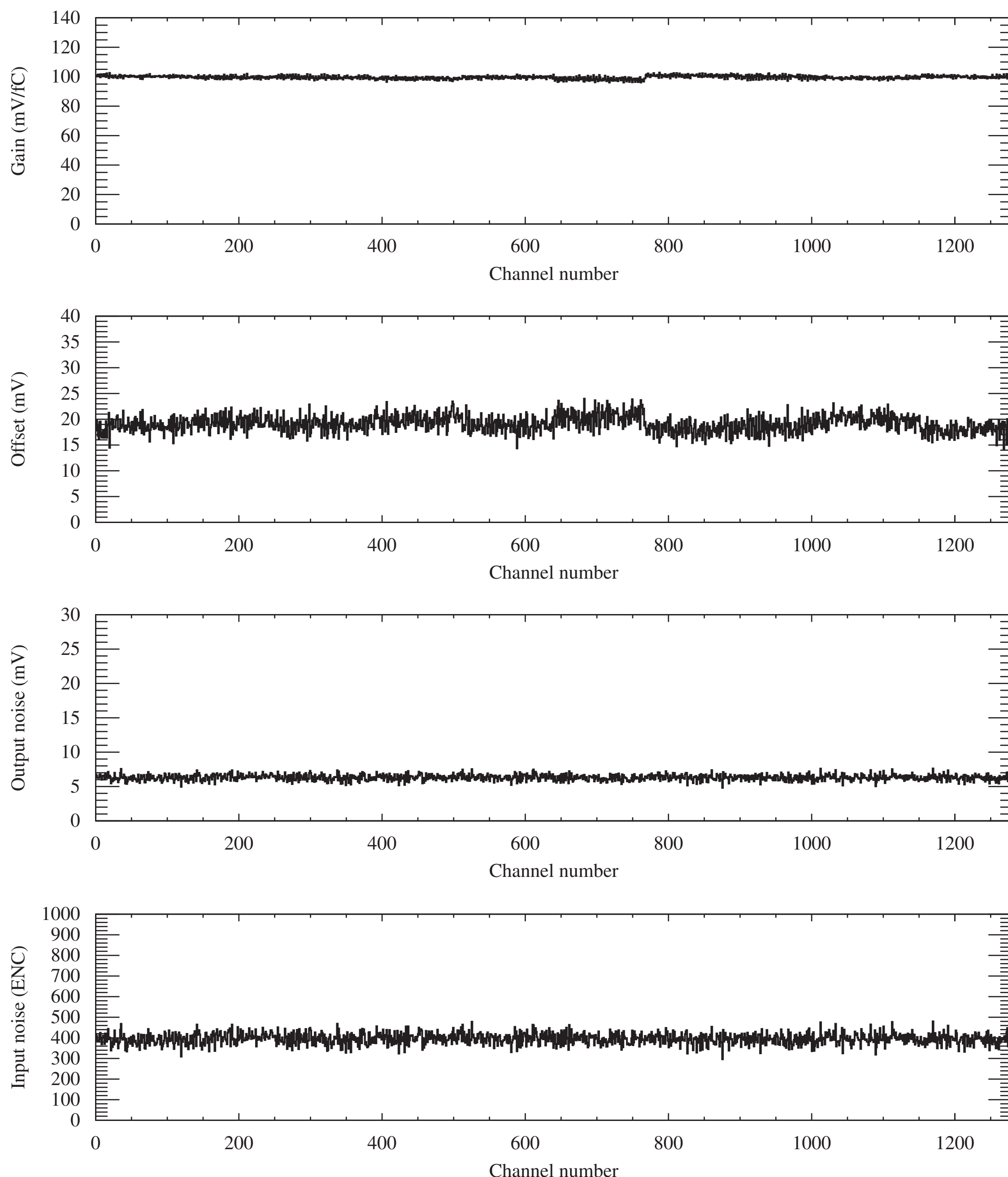

Fig. 7. From top to bottom, distribution of gain, threshold offset, output and input noise from a three-point gain scan for 1.0, 1.5 and 2.0 fC input charges.

damage in silicon detectors can be monitored by measuring the leakage current as it is linearly proportional to the fluence and is exponentially proportional to temperature [11]. If a power balance is not maintained between the active cooling and heating components, thermal runaway may occur. Detailed simulations based on Finite Element Analysis (FEA) were performed with ABAQUS [12] in order to study the thermal performance of the module design. Fig. 8 shows the predicted temperature distribution on a module for a chip power of 0.15 W and a cooling temperature of −30 °C The maximum unpowered silicon temperature would be in this case ~−22 °C.

The runaway is an analytic extrapolation of the maximum silicon temperature that is defined for the silicon power density at 0 °C. Fig. 9 shows the predicted runaway point as a function of the silicon sensor power density and different scenarios for the convection temperature. The detector power density expected at the sLHC fluence is also quoted. A thermal grease conductivity of 0.8 $W/m^2 K$ was taken into account in the simulation. This low mass module design is shown to be satisfactory, the safety margin is approximately a factor 4 to the runaway point.

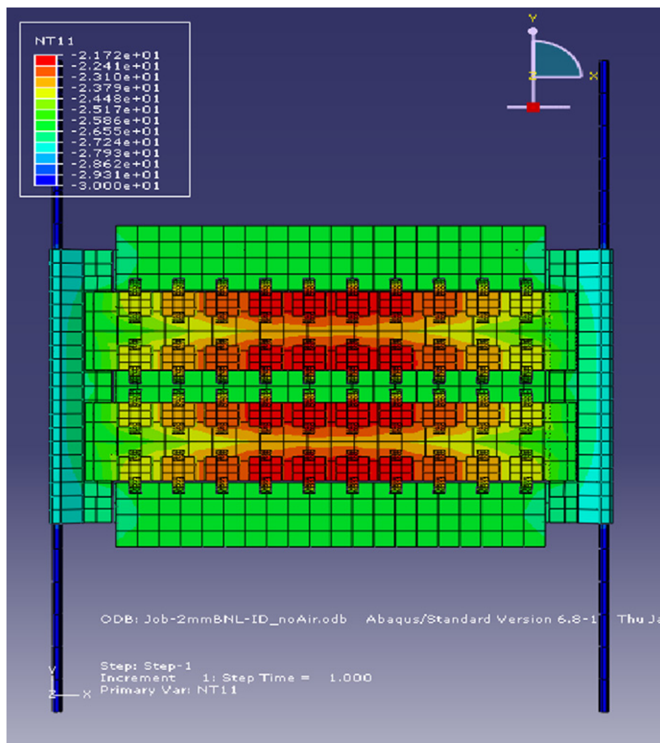

Fig. 8. Temperature distribution on the module based on FEA thermal simulations. The minimum and maximum values in the temperature scale are −30 and −21.7 °C, respectively.

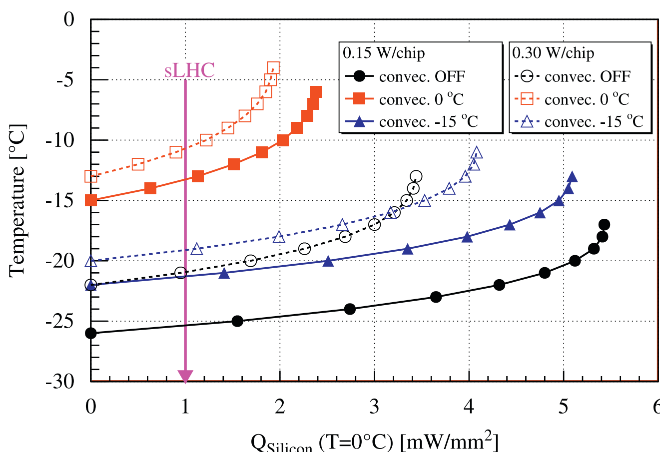

Fig. 9. Simulation results for the thermal runaway for the module concept.

5. Module assembly and testing

The assembly sequence of a single module can be splitted into four main stages:

- assembly of the TPG baseboard and AlN facings;
- assembly of sensors to baseboard and washers;
- assembly of top-side hybrids; and
- assembly of bottom-side hybrids.

Since the module program for KEK and Geneva is focusing on producing several module prototypes to prove their functionality and to study their electrical and thermal performances, the mechanical precision in the module assembly is not a primary target. At this stage, the sensors will be positioned from the detector edges to the jig alignment pins. Fig. 10 shows some of the jigs already produced for the module assembly. Once the glue is cured, the module is transferred for bonding.

A module interface board (MAB) has been designed and produced to allow the testing of a full module equipped with four hybrids (80 ABCN chips). The MAB holds several LVDS data/clock distributors to fanout clock and command signals to the FEs. Eight channels of the DAQ system are used for data acquisition (two lines per hybrid). Static signals are set by means of a DIP switch. The information from each of the four NTC thermistors is also available for temperature monitoring.

Fig. 11 shows a view of the four-module test box equipped with four double-sided silicon micro-strip modules and corresponding MAB cards. A common cooling pipe passing through the individual module cooling-plates will dissipate the heat generated. A flex-extender is used to surpass the aluminum frame to route the signals between the hybrids and the readout cards. A 4.2 mm stainless-steel pipe is intended to be used with C_3F_8 cooling, but can be adapted for other options (e.g. CO_2).

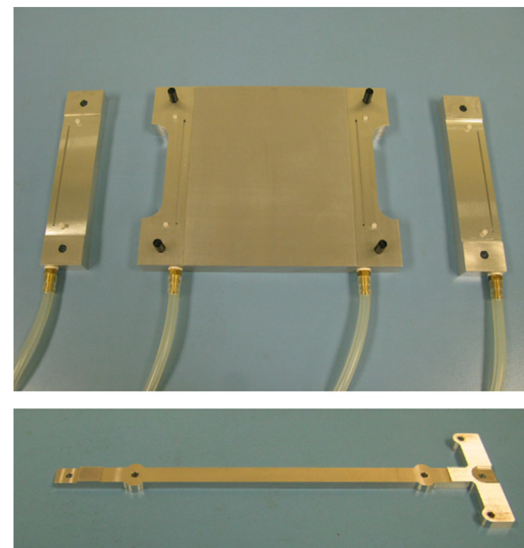

Fig. 10. Jigs for detector and AlN facings assembly (top) and hybrid positioning (bottom).

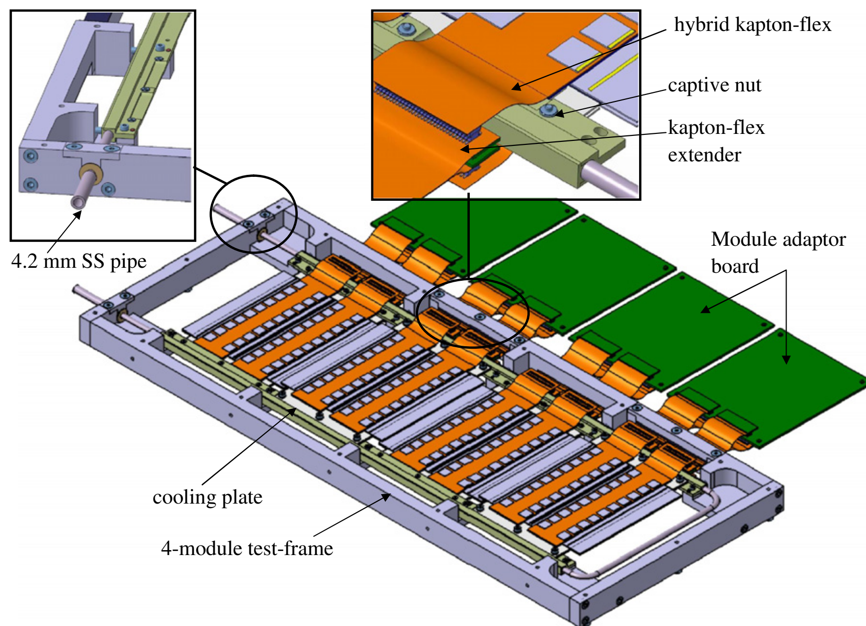

Fig. 11. View of the four-module test-box.

6. Local support structure

A local support (see Fig. 12) able to hold 12 modules has been developed. The local structure allows the end insertion of the support into the overall structure (e.g. barrel cylinders). The end insertion concept has been fully adopted for either stave of module concepts because of its flexibility for integration, commissioning and rework. A demonstrator of the support has been constructed, showing the feasibility of assembly, precision mounting and insertion/integration to the barrel structure.

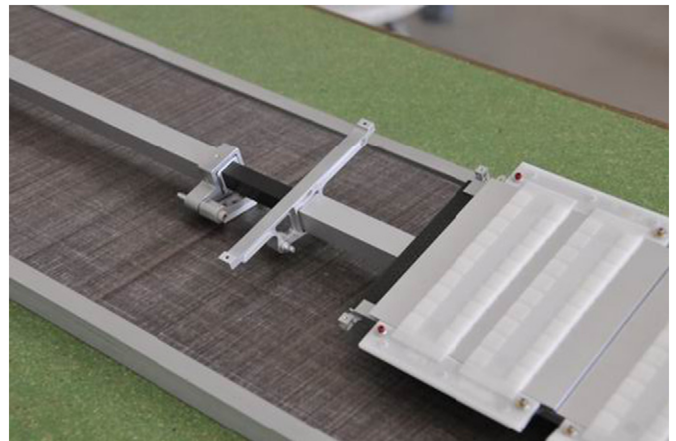

Fig. 12. Demonstrator with dummy modules for validation of the end-insertion concept.

7. Irradiations

As part of our R&D program, a module prototype has been built to be irradiated at the CERN-PS Irradiation facilities during the October/November 09 irradiation period. Due to limited availability of components for the prototype assembly, the module consists of one fully qualified sensor, one mechanical grade sensor, two fully populated hybrids on one side and two carbon-fibre bridges on the other side (for mechanical symmetry and stability). Fig. 13 shows a picture of the final assembled prototype module.

The total irradiation dose will be $\sim 4\times 10^{14}\,\mathrm{neq/cm^2}$. The beam profile has a size of $\sim 1\,\mathrm{cm^2}$, and with the detectors being almost parallel to the beam, 10 scan points will be needed to fully cover the sensing area. During the irradiation, the sensors will be biased and the front-end chips powered and clocked. The hybrid temperature and the sensor current will be monitored continuously.

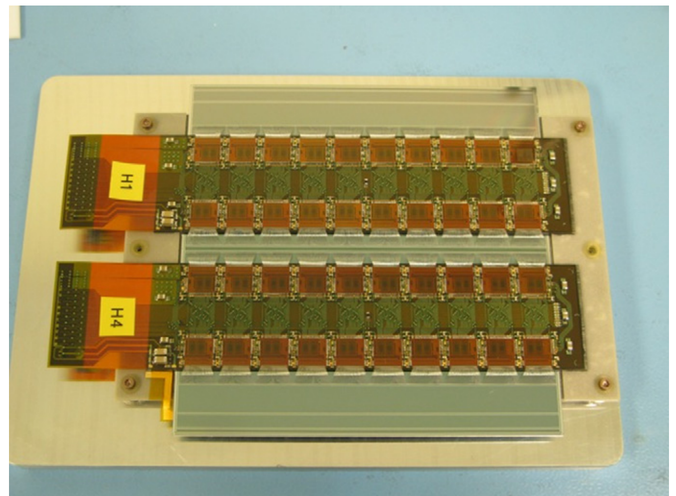

Fig. 13. Prototype module for irradiation.

8. Summary

A new design of a double-sided silicon micro-strip module for the short strip region of the upgraded ATLAS inner tracker has been presented. Preliminary results on bare hybrids show excellent performances of the first prototype readout ABCN25 ASIC. The R&D program shared between KEK and the University of Geneva is intended to demonstrate the competitiveness of the

proposed design through detailed evaluation of electrical and thermal performances of prototype modules.

Acknowledgments

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