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Development of novel n^+-in-p Silicon Planar Pixel Sensors for HL-LHC

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ABSTRACT

We have been developing highly radiation-tolerant n^+-in-p planar pixel sensors for use in the high-luminosity LHC. Novel n^+-in-p structures were made using various combinations of the bias structures (punch-through or polysilicon resistor), isolation structures (p-stop or p-spray), and thicknesses (320 μm or 150 μm). The 1-chip pixel modules with thin FE-I4 pixel sensors were evaluated using test beams, before and after 2×10^{15} n_{eq}/cm^2 irradiation. The full depletion voltages were estimated to be 44 ± 10 V and 380 ± 70 V, in the non-irradiated and the irradiated modules, respectively. A reduction of efficiency was observed in the vicinity of the four pixel corners and underneath the bias rail after the irradiation. The global efficiencies were $>99\%$ and $>95\%$ in the non-irradiated and the irradiated modules, respectively. The collected charges were uniform in the depth direction at bias voltages well above the full depletion voltages. The encapsulation of vulnerable edges with adhesive or parylene prevented HV sparking. Bump bonding with the SnAg solder bumps was performed at HPK with 150 μm- and 320 μm-thick sensors and chips. No disconnection of bumps was observed after 10 thermal cycles between -40 and $+50$ °C, with a temperature slew rate of >70 K/min.

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1. Introduction

Hybrid pixel detectors in which the sensor and read-out chip are separate entities and connected with bump bonding have been used in many applications [1,2]. We have been developing so-called n^+-in-p pixel sensors that are highly radiation-tolerant, have a "planar" electrode geometry, utilize p-type silicon wafers, and are read-out from highly doped n^+ implants, as shown in Fig. 1 [3]. We propose their use in, e.g., the high-luminosity large hadron collider (HL-LHC) where the particle fluence is expected to be in the range of 10^{15} to a few $\times10^{16}$ 1-MeV-neutron-equivalent $(n_{eq})/cm^2$.

The n^+-in-p silicon sensors have the following properties: the p-type silicon wafer does not change type after irradiation (no type-inversion); read-out is from the junction side (n^+) in all cases; and the collected carrier is the electron. These properties lead to a number of benefits: the lithographic processes are only required on a single side, which lead to lower production costs; partially depleted operation is allowed, which is crucial after heavy irradiation in which the full-depletion voltage becomes higher than the operation voltage; and stronger and faster signals are induced by the carrier in the higher electric field in the junction side, thus leading to less charge-trapping. We have previously reported the successful development and characterization of n^+-in-p silicon "strip" sensors [4–7].

A typical n^+-in-p planar pixel module is shown in Fig. 1. For the pixel sensors, the critical issues include operation at very high voltage, implementation of isolation and bias structures, and

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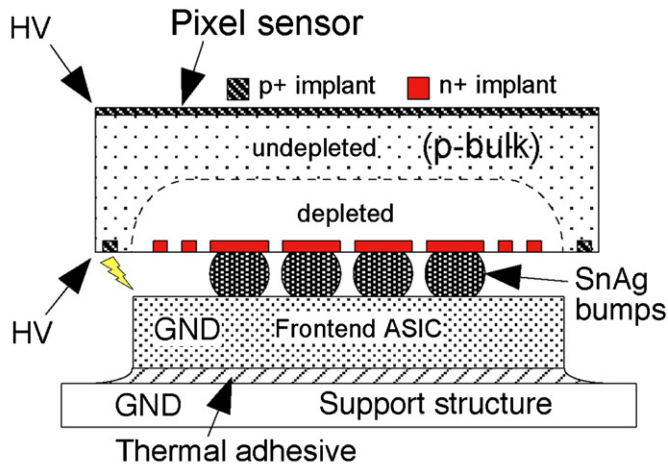

Fig. 1. Typical cross-section of an n^+-in-p hybrid pixel module.

reduction of material. For the pixel modules the critical issues include prevention of high voltage sparking and the need to bump bond with lead-free bumps. The R&D issues addressed in this paper cover the following areas:

1. The pixel sensor is required to be operated up to 1000 V, to cope with the increasing full-depletion voltage caused by radiation damage.
2. An isolation structure is required to isolate the n^+ pixels from being connected by the conductive layer of attracted electrons in the surface of silicon, caused by the built-in and radiation-induced positive charge-up in the interface of the silicon and the surface oxide. The isolation structure has to be robust, i.e. not to introduce breakdown in leakage current, against the high electric field caused by the high voltage operation.
3. A bias structure is required to provide a high voltage to all pixels for testing without connecting the pixels to the read-out chip. The insensitive area caused by the structures must be minimized.
4. The sensors must be made as thin as possible in order to be compatible with the performance requirements for detectors which are placed close to the interaction point. Thinning techniques must be developed.
5. The high voltage (HV) (edge of the sensor) and the ground (GND) (read-out chip) can, in the case of n^+-in-p devices, be as close as 20–30 μm. Techniques must be developed to prevent sparking between the HV and any GND point up to 1000 V.
6. Usage of lead-free Tin–Silver (SnAg) solder bumps has became the industry standard. We must demonstrate the quality and yield of the SnAg bump bonding to our application.

2. Novel n^+-in-p pixel sensors

A number of n^+-in-p pixel sensors were laid out on a 6-in. wafer [3], which was processed by Hamamatsu Photonics (HPK) [8]. A picture of the wafer is shown in Fig. 2. The pixel sensor, mated with the ATLAS FE-I3 [2] or the FE-I4 [9] pixel read-out chip, is called “FE-I3” or “FE-I4 pixel sensor”, respectively. The layout was made up of 1-chip and 4-chip tiles of the FE-I3 and 1-chip and 2-chip tiles of the FE-I4 pixel sensors as indicated in the figure. The typical parameters of the n^+-in-p KEK/HPK pixel sensors are summarized in Table 1.

The designs of the pixel structure in the vicinity of bias structure are shown in Fig. 3. Two types of resistive structure

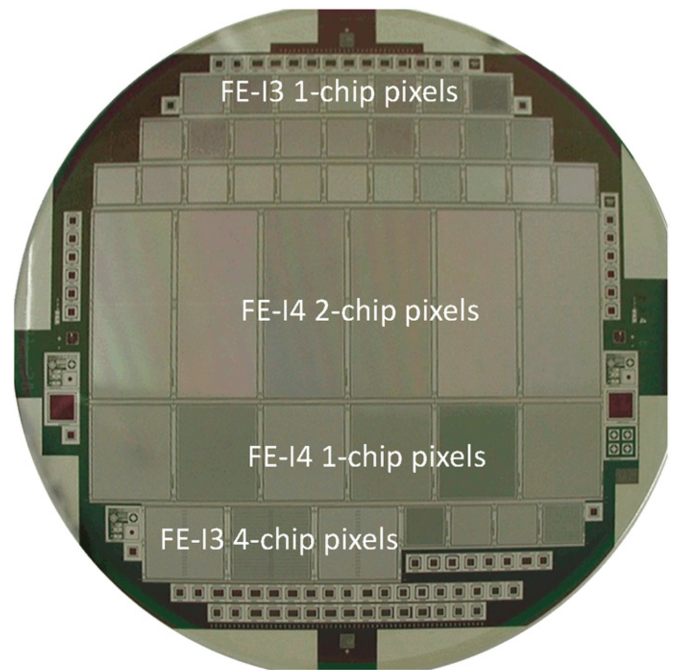

Fig. 2. Layout of pixel sensors on 6 in. wafer.

Table 1
Typical parameters of KEK/HPK n^+-in-p pixel sensors.

Silicon wafer	6 in. p-type FZ	
Crystal orientation	⟨100⟩	
Resistivity	4–7 kΩ cm	
Thickness	320 μm	
FE-I4 pixel sensor	1-chip	2-chip
Pixel size	$50 \times 250\ \mu m^2$	
Bias structure	PTLA (four pixel corner)	
	PolySi (~2.7 MΩ)	
Dimension	18.7 × 20.9	$18.7 \times 41.3\ mm^2$
Number of pixels	336 × 80 = 26 880	336 × 160 = 53 760
FE-I3 pixel sensor	1-chip	4-chip
Pixel size	$50 \times 400\ \mu m^2$	
Bias structure	PolySi (~1 MΩ)	
Dimension	10.5 × 10.0	$18.7 \times 17.2\ mm^2$
Number of pixels	164 × 18 = 2952	328 × 36 = 11 808
Isolation (density)	p-stop ($\sim 4 \times 10^{12}$ ions/cm^2)	
	p-spray ($\sim 2 \times 10^{12}$ ions/cm^2)	
Thickness after thinning	150 μm	

were formed from the bias rail: (1) a punch-through structure with an implant dot at the four pixel corners, called “PTLA” (Fig. 3(a)–(c)) and (2) a long trace of polysilicon resistor, “PolySi” (Fig. 3(d)–(f)). The PTLA dots were placed at all four pixel corners by mistake, whereas it had been intended to place them only at alternate four pixel corners. The three isolation structure conditions were (1) common p-stop (Fig. 3(a) and (d)), (2) individual p-stop (Fig. 3(b) and (e)), and (3) p-spray (Fig. 3(c) and (f)). The p-stop structure uses a lightly doped p-implantation in a masked area. The p-spray method, at HPK, uses a wafer with a lightly doped p-implantation over the full surface. The bias rail is a metal trace placed over the insulator with no implantation in the silicon underneath.

The potential to the bias rail was provided from the bias ring at the edge of the sensor. The bias ring was surrounded by one guard ring, floating in potential. The sensors were diced at 450 μm from the end of pixel implants in the long pixel direction. In the short

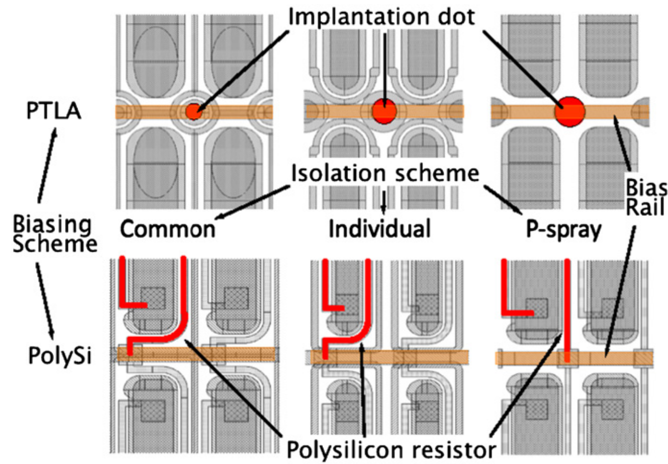

Fig. 3. Pixel structures in the vicinity of bias structures: punch-through type (PTLA: (a)–(c)) and polysilicon type (PolySi: (d)–(f)), combined with the isolation structures of common p-stop ((a), (d)), individual p-stop ((b), (e)), and p-spray ((c), (f)).

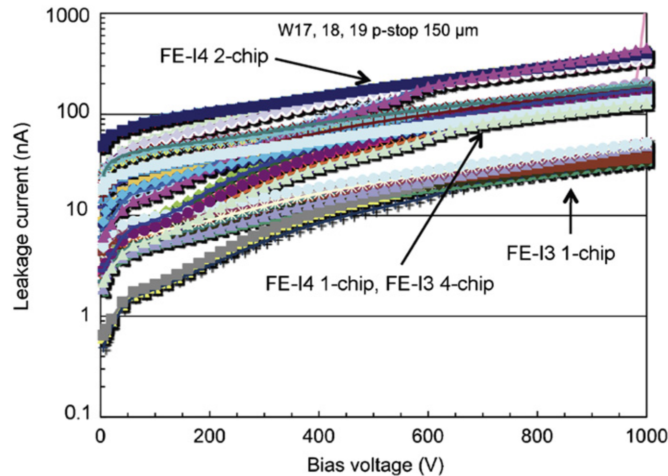

Fig. 4. Leakage currents of thin pixel sensors with p-stop isolation in wafers.

pixel direction, at 1175 µm as the requirement for narrowness was modest in this direction.

Thin pixel sensors (150 µm in thickness) were fabricated, aiming for reducing the amount of material. The thin sensors were made in two steps: completing the n^+ pixel side in the normal wafers of 320 µm in thickness, then thinning and completing the back-side. The leakage currents of the thin pixel sensors are shown in Fig. 4, as measured in the wafers, before dicing. There were 21 FE-I3 1-chip, 9 FE-I3 4-chip, 18 FE-I4 1-chip, and 18 FE-I4 2-chip pixel sensors. No sudden increase of leakage current was observed up to 1000 V. There were four groups of the leakage currents: ~40 nA for FE-I3 1-chip, ~150 nA for FE-I3 4-chip, ~200 nA for FE-I4 1-chip, and ~400 nA for FE-I4 2-chip pixel sensors, at a bias voltage of 1000 V. The linearity of the leakage currents as a function of sensor area was an indication of the correct functionality of the PTLA and the PolySi bias structures. The p-spray sensors showed lower breakdown voltages at approximately 900 V.

Out of four thinned wafers containing the pixel sensors, four of the thin FE-I4 1-chip pixel sensors were diced and bump bonded, at IZM [10]. The four pixel sensors after bump bonding still had no breakdown in the leakage current up to 1000 V. The properties of the thin FE-I4 1-chip pixel modules are summarized in Table 2.

3. Evaluation of 1-chip modules before and after irradiation

We evaluated the FE-I4 1-chip modules in two beam tests at CERN, using 120 GeV π^+ particles [11], and in the laboratory, using a ^{90}Sr β-source. The modules that had not been irradiated (non-irradiated (NR)) were tested in the first beam test. The modules (KEK3, KEK5, KEK6) were then irradiated using 23 MeV protons at Karlsruhe [12] to a fluence of 2×10^{15} n_{eq}/cm^2 . The second beam test was performed with non-irradiated KEK4 and the irradiated modules (irradiated (IR)). The results are presented in detail in Ref. [13].

The signal pulse height distributions as a function of the bias voltage of the FE-I4 1-chip modules (KEK4 and KEK5) are shown in Fig. 5. The pulse heights, measured with the time-over-threshold (TOT), included non-linearity of the amplifiers. The pulse heights were then normalized to unity, for NR modules at 150 V and for IR modules at 1000 V, respectively. The normalized pulse heights were well aligned with each other, including the laboratory measurements (lab) using a β-source. The full-depletion voltage was approximately 50 V and 400 V in the NR and IR modules, respectively. The charge collection was still efficient at partial-depletion voltages. The pulse heights in the IR modules increased gradually by 10% when going from 400 V to 1000 V, which implied smallness of the influence of, e.g., the charge multiplication [14].

The collected charge is known to increase in proportion to the square-root of the applied voltage, at least in the non-irradiated silicon crystals [15]. The full depletion voltages were estimated by fitting a function, $f(x)=\sqrt{(x-a)/(b-a)}$, where a represents any offset effects and b represents the full depletion voltage at which the function reached unity at $x=b$. Fits were made to two cases for the NR modules: 15 V to 25 V and 15 V to 50 V; three cases in the IR modules: 50 V to 200 V, 50 V to 300 V, and 50 V to 400 V. The average and the standard deviation of the full depletion voltage, V_{FD}, were 44 ± 10 V and 380 ± 70 V, in the NR and IR modules, respectively. The solid curves in Fig. 5 show the fit functions with the full depletion voltage reference and the unity. The effective doping concentration, N_{eff}, is related to the full depletion voltage, V_{FD} as $N_{eff}=2\epsilon(V_{FD}+V_{bi})/eW^2$, where ϵ is the dielectric constant of silicon, ~ 1.05 pF/cm, e is the electronic charge, 1.6×10^{-19} C, V_{bi} is the built-in voltage, ~0.5 V, and W is the thickness of the silicon, 150 µm in these sensors. The N_{eff}'s were, then, derived to be $(2.6\pm0.6)\times10^{12}$ and $(2.2\pm0.4)\times10^{13}$ cm^3, before and after the irradiation, respectively.

The effect of the bias and the isolation structures is shown in Fig. 6; the local efficiency maps where the pixels in a chip were folded into a pixel (at the center and parts of the adjacent pixels). The NR module ((a) KEK4, PolySi-common p-stop, at 200 V) was highly efficient. Irradiation decreased the efficiencies of the IR modules ((b) KEK5, PolySi-common p-stop, (c) KEK6, PTLA-individual p-stop, both at 1000 V), at the four pixel corners ((125, 25), (125, 75), (275, 25) and (275, 75)), an effect which was much more noticeable under the bias rail and at the PTLA dot, than for the NR module. The PTLA-individual p-stop module was less efficient than the PolySi-common p-stop module, although some efficiency can be recovered by correct design of the alternate PTLA structure. The global efficiencies are summarized in Table 2 for the modules in the first and the second beam test.

The pulse height distribution, Q (TOT), in the depth direction is shown in Fig. 7. This data was collected using shallow angle incident beams at 4°. The pulse heights in the first and the last bin were less because the particles passed the pixels partially depending on the entrance or exit location. In other cases, the pulse heights were essentially uniform over depth both in the NR (at 200 V) and IR (at 1000 V) modules, which implies that the influence of charge trapping was small along the drift path from the back-side to the

Table 2
Properties of FE-I4 1-chip pixel modules.

ID	SCC no.	Bias st.	Isolation st.	Eff. 1st	Eff. 2nd
KEK3	SCC93	PolySi	Individual p-stop	$99.7 \pm 0.02\%$ (NR)	N/A
KEK4	SCC94	PolySi	Common p-stop	$98.7 \pm 0.17\%$ (NR)	$99.8 \pm 0.02\%$ (NR)
KEK5	SCC95	PolySi	Common p-stop	$99.7 \pm 0.02\%$ (NR)	$95.6 \pm 0.15\%$ (IR)
KEK6	SCC96	PTLA	Individual p-stop	$94.2 \pm 0.04\%$ (NR)	$94.9 \pm 0.14\%$ (IR)

SCC, single chip card; st., structure; eff., efficiency; N/A, not available; NR, non-irradiated; IR, irradiated to 2×10^{15} n_{eq}/cm^2.

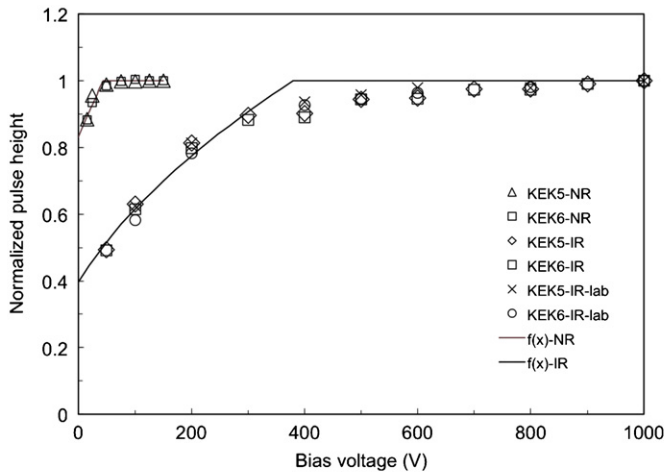

Fig. 5. Normalized pulse height distributions as a function of the bias voltage of FE-I4 1-chip modules (KEK4 and KEK5). The pulse heights of non-irradiated and irradiated (2×10^{15} n_{eq}/cm^2) cases are normalized to unity at 150 V and at 1000 V, respectively. Solid curves are fit functions with the full depletion voltages of 44 V and 380 V for the NR and IR modules, and the unity pulse height reference.

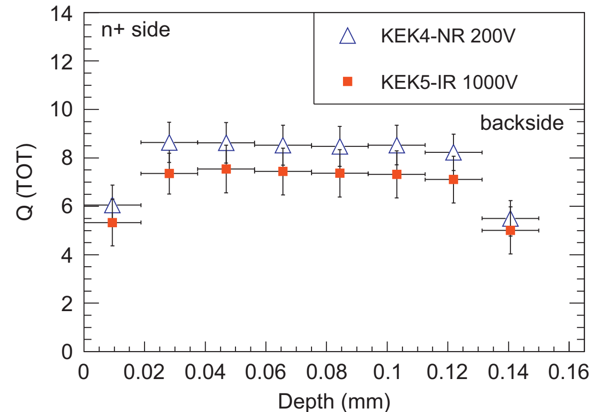

Fig. 7. Pulse height distribution in the depth direction, using shallow incident-angle beam.

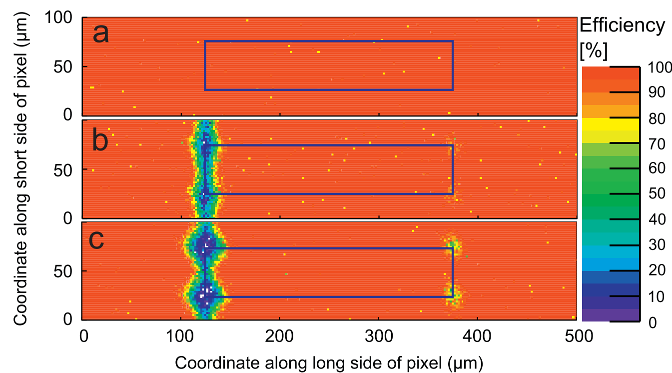

Fig. 6. Local efficiency map of a pixel: (a) non-irradiated PolySi-common p-stop (KEK4) and irradiated (2×10^{15} n_{eq}/cm^2), (b) PolySi-common p-stop (KEK5) and (c) PTLA-individual p-stop (KEK6) for FE-I4 1-chip modules.

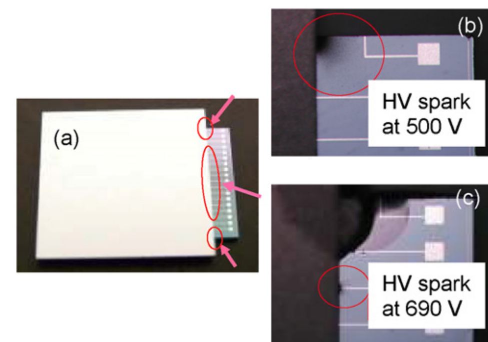

Fig. 8. HV protection test: (a) pixel module with FE-I3 real pixel sensor and aluminum-trace dummy read-out chip, (b) HV spark mark at cross-corner of edges at 500 V, and (c) HV spark mark on aluminum trace that occurred at 690 V. The gap between sensor and chip was 20–30 μm.

(charge-collecting) n^+ side. The observation was consistent with the charge trapping distance for the fluence of 2×10^{15} n_{eq}/cm^2 of order of 150 μm [13].

4. Prevention of high-voltage sparking using post-process application

4.1. Encapsulation

The HV-protection test samples were made of real FE-I3 pixel sensors and dummy read-out chips that had been bump bonded. A sample in which the top chip is the pixel sensor is shown in Fig. 8(a). The dummy chips were made with aluminum patterns to make a daisy-chain connection. The aluminum patterns were passivated with silicon oxide of ~ 1 μm in thickness, except for the bump bonding pads and the probing pads at the end of the traces. The gap between the chips was 20–30 μm. Three areas were of interest: the two cross-corner of the pixel sensor and the read-out chip, and the one side-edge facing the aluminum traces. Three types of encapsulation were applied with a silicone adhesive: encapsulating (1) no area (sample #1), the cross-corners (sample #2), and both the cross-corners and the full length of the facing edge (sample #3). When applying high voltage to the back-side of the pixel sensor and keeping the pixels on the front side and the read-out chip grounded, sparks occurred at 500 V at the cross-corners of sample #1, Fig. 8(b), and at 690 V at the aluminum trace facing the edge in sample #2, Fig. 8(c). No spark was observed up to 1000 V for the fully encapsulated sample (#3).

The HV protection of the FE-I4 1-chip pixel modules in Section 3 was applied over the full length with a silicone adhesive, as shown in Fig. 9. All non-irradiated and irradiated modules operated successfully up to 1000 V both in the laboratory and in the beam tests.

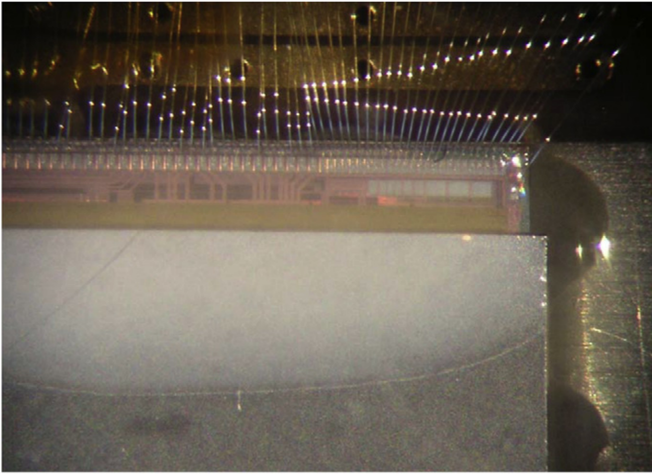

Fig. 9. HV encapsulation of FE-I4 module for use with test beam.

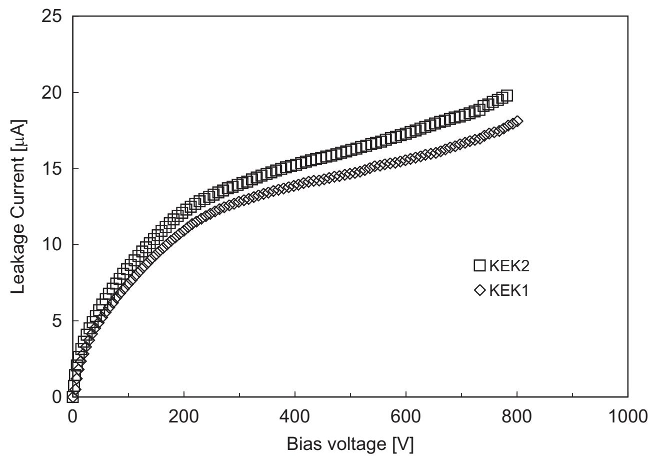

Fig. 10. Leakage current as a function of the bias voltage of FE-I3 module after Parylene-C (~3 μm) coating.

4.2. Parylene coating

Two FE-I3 1-chip pixel modules, KEK1 and KEK2, were assembled on FE-I3 single chip cards (SCCs) [3]. The vicinities of the pixel modules in the SCC's were conformally coated with Parylene-C of ~3 μm in thickness [16], for which the breakdown voltage is expected to be >1000 V [17]. These Parylene-coated SCC's were irradiated using 70 MeV protons to 1.1×10^{15} n_{eq}/cm^2 [18]; no damage to the parylene was observed. The leakage currents as a function of the bias voltage are shown in Fig. 10; the breakdown was observed at approximately 700 V, which was consistent with the known breakdown voltage of the card. These FE-I3 1-chip modules were in the test beams at CERN in 2010 and 2011 [11]. In retrospect, the softer Parylene-N might be better suited for our application than the harder Parylene-C, as the Parylene-N produces a highly conformal thin coating.

5. Bump-bonding at HPK

5.1. SnAg bump-bonding

We have been developing bump-bonding technology at HPK. The FE-I3 1-chip pixel modules in Section 4.2 were bump-bonded at HPK, using the pixel sensors applied with electroless under-bump-metallization (UBM) at HPK and FE-I3 read-out chips applied with electro-plating UBM and lead–tin (PbSn) solder bumps at IZM.

Because industrial bump bonding has begun shifting towards lead-free materials, we performed tin–silver (SnAg) solder bump bonding with the FE-I3 and the FE-I4 dummy sensors and the dummy read-out chips with daisy-chain patterns. The FE-I4 1-chip and the 4-chip bump-bonded modules are shown in Fig. 11, (left) 1-chip with 150 μm-thick chips and (right) 4-chip with 320 μm-thick chips. The UBM of one side was electroless and the other side of the SnAg bumps was electroplated. We have previously reported a high resistance per (SnAg) bump, likely because of the (possible) existence of a thin insulating layer [3]. The issue has been resolved by including a plasma-etching process. The resistances of the daisy chains of the new FE-I4 1-chip dummy module are shown in Fig. 12. The resistance per bump was ~0.28 Ω, comparable to the resistance of PbSn of ~0.14 Ω reported in Ref. [3].

5.2. Thermal cycling

The pixel modules are to be cooled to, e.g., −40 °C to reduce the leakage current after heavy irradiation. Thermo-mechanical resistance to the thermal cycling is an issue in bump-bonded modules. To achieve a high cool-down/warm-up slew rate, a simple setup consisting of climate chambers was prepared: one chamber with a low (−40 °C) and the other with a high (+50 °C) temperature; each condition included a large aluminum block placed inside the chamber to act as a heat capacitor. Six FE-I4 1-chip dummy modules were subjected to 10 thermal cycles. The samples were placed in an aluminum box. The aluminum box was

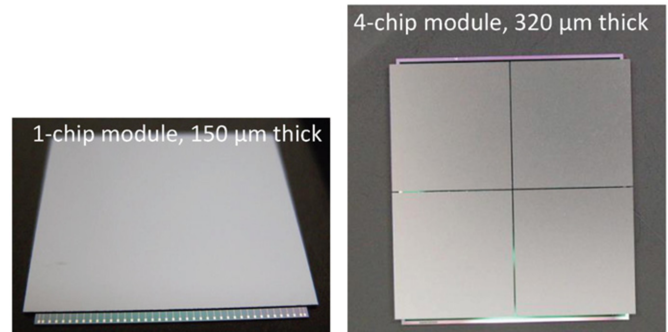

Fig. 11. FE-I4 1-chip and 4-chip dummy modules.

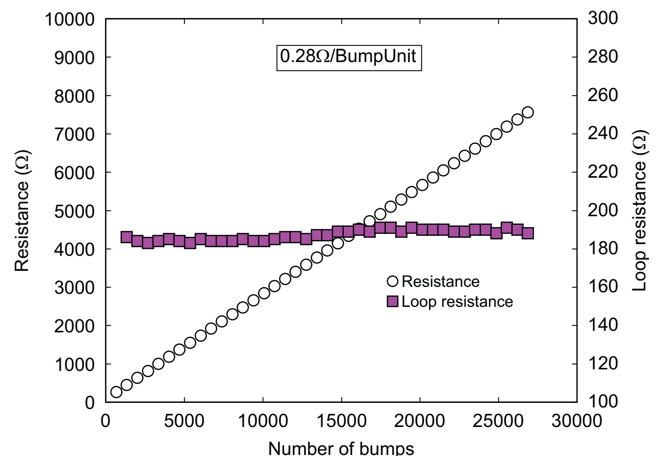

Fig. 12. Resistances of SnAg solder bumps of FE-I4 1-chip dummy module.

placed on the aluminum block for 30 min in one climate chamber, and then transferred by hand to the other for another 30 min, to make one thermal cycle. A platinum resistor (PT100) was attached to a piece of silicon and placed in the box to measure the temperature. The temperature slew rate upward was 108.2 K/min for the first 30 s and 73.4 K/min in 1 min. The rate downward was -115.4 K/min in the first 30 s and -71.6 K/min in 1 min. With one climate chamber to cool down or warm up, the temperature slew rate was approximately 3–5 K/min.

After 10 thermal cycles between $-40\,^{\circ}$C and $+50\,^{\circ}$C, none of the six samples had developed any disconnection. The average resistance of a daisy chain though full bumps was $5083 \pm 1374\,\Omega$ and $5110 \pm 1370\,\Omega$, and the difference in resistance was $27 \pm 31\,\Omega$, before and after the thermal cycling, respectively.

6. Summary

We have been developing highly radiation-tolerant n^{+}-in-p planar pixel sensors for the fluence of 10^{15} to a few $\times 10^{16}$ n_{eq}/cm^2 expected in the HL-LHC, and we have addressed the issues associated with the n^{+}-in-p hybrid pixel modules. Novel n^{+}-in-p pixel sensors were fabricated with a bias structure of the punch-through dot at the four pixel corners or of the polysilicon resistor, combined with an isolation structure of common or individual p-stop, or p-spray. The pixel sensors of 150 μm in thickness were fabricated by thinning the back side of the wafers of 320 μm in thickness, after completing the frontside process. Little leakage current breakdown was observed up to a bias voltage of 1000 V.

The thin FE-I4 1-chip pixel sensors, bump bonded with FE-I4 read-out chips, were evaluated both in test beams and in the laboratory, both before and after 2×10^{15} n_{eq}/cm^2 irradiation. The full depletion voltage was estimated (from the charge collection data) to be 44 ± 10 V and 380 ± 70 V, and then the effective doping concentration to be $(2.6 \pm 0.6) \times 10^{12}$ and $(2.2 \pm 0.4) \times 10^{13}$ cm^3, in the non-irradiated and the irradiated sensor, respectively.

The effect of the bias and the isolation structures was compared based on the local efficiency map of a pixel. A reduction of efficiency was observed in the vicinity of four pixel corners and especially underneath the bias rail, after the irradiation. Efficiency in average was $>99\%$ and $>95\%$ in the non-irradiated and irradiated modules, respectively. The charge collection in the depth direction was studied by using the shallow angle incident beams at 4°. The collected charges were uniform in the depth direction at bias voltages well above the full depletion voltages, and consistent with the charge trapping distance of order of 150 μm for the fluence of 2×10^{15} n_{eq}/cm^2.

HV sparking was confirmed with the dummy modules made up of real pixel sensors and dummy read-out chips. Sparking occurred at 500 V at the cross-corners of edges, and at 690 V at the trace on the chip and sensor edge. Prevention of HV sparking was achieved either by encapsulating the vulnerable edges in a silicone adhesive or by applying Parylene coating. The FE-I4 1-chip pixel modules encapsulated with a silicone adhesive operated successfully up to 1000 V in test beams and the laboratory.

Bump bonding with SnAg solder bumps was performed at HPK, with dummy FE-I4 sensors and chips of 150 μm and 320 μm in thickness. Six dummy modules were subjected to 10 thermal cycles between -40 and $+50\,^{\circ}$C, with temperature slew rates of >70 K/min. No disconnection of bumps was observed.

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