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Radiation effects in silicon-on-insulator transistors with back-gate control method fabricated with OKI Semiconductor 0.20 μm FD-SOI technology

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ABSTRACT

Bonded silicon-on-insulator (SOI) wafers have the capability of realizing monolithic pixel devices, where the silicon resistivity is optimized separately for the electronics and detector parts. Using UNIBOND wafers, we are developing monolithic pixel devices fabricated with OKI Semiconductor 0.20 μm FD-SOI technology. A set of PMOS and NMOS transistors were irradiated with protons in order to investigate the total ionization dose effect in transistor operation. We evaluated also the devices with a back-gate control electrode added underneath the buried oxide layer. Primary radiation effect appears in transistor threshold shifts, which can be explained by charge traps in the oxide layers and charge states created at the silicon–oxide boundaries. We discuss the possibility of TCAD simulation for evaluation of the charge densities.

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1. Introduction

Monolithic devices, where the sensor and readout electronics are integrated on one chip are the ideal type of radiation detectors for the user. Such a technology is of prime importance for fabrication of devices with large number of readout channels with fine segmentation though at a small cost. The pixel devices at the Large Hadron Collider (LHC) experiments, for example, consist of nearly 100 million channels with pixel sizes of 400×50 (ATLAS [1]) and $100 \times 150\ \mu m^2$ (CMS [2]). They rely on bump bonding for integration of pixels to their readout electronics. This procedure becomes delicate with increasing number of pixels and for the devices with finer pixel size. Smaller pixel size provides improved performance in various applications such as medical, biometrics and high-speed. Reliable and low cost monolithic devices are, of course, interesting even for smaller systems.

We are investigating UNIBOND™ [3] silicon-on-insulator (SOI) wafers for the fabrication of monolithic pixel devices. With such bonded wafers, the silicon resistivity can be optimized separately for the readout electronics and SOI “handle wafer” which we adopt as the sensitive part. The original idea of SOI monolithic pixel sensor can be found in Ref. [4]. SOI pixel devices were also fabricated using non-commercial processes utilizing low resistivity separation by implantation of oxygen (SIMOX) [5,6] and low doping UNIBOND wafers [7]. We are developing pixel devices SOIPIX [8–11] using 0.15–0.20 μm fully depleted SOI (FD-SOI) CMOS processes commercially provided by OKI Semiconductor Co. Ltd.

The pixel device structure is illustrated in Fig. 1. Table 1 summarizes the SOIPIX parameters fabricated with OKI Semiconductor 0.2 μm process.

The readout electronics is fabricated in 40 nm thick SOI silicon. The pixel electrodes penetrate through the 200 nm thick buried oxide (BOX) layer into the handle wafer, which is high resistive silicon adopted as a sensitive volume. After the top side process was completed, the device was thinned to 260 μm and the backside was Al sputtered for biasing.

Several sensor types have been fabricated successfully [12] showing ingenious features of the SOI monolithic devices. Radiation damage in 0.15 μm devices has also been evaluated [13]. The irradiated pixel device was sensitive to red light; although the electronics performance was degraded due to changes in the transistor operation condition. However, electronics operation is substantially affected through the BOX layer by the bias applied to the backside—the back-gate effect. A bias of 10 V maximum was typically applicable, which was not sufficient to detect hard X-rays and minimum ionizing particles for limited depletion thickness. A novel method (BPW—buried P-well) to control the back-gate effect was developed recently, which is shown to solve the problem [14]. The BPW is a p^+ layer implanted

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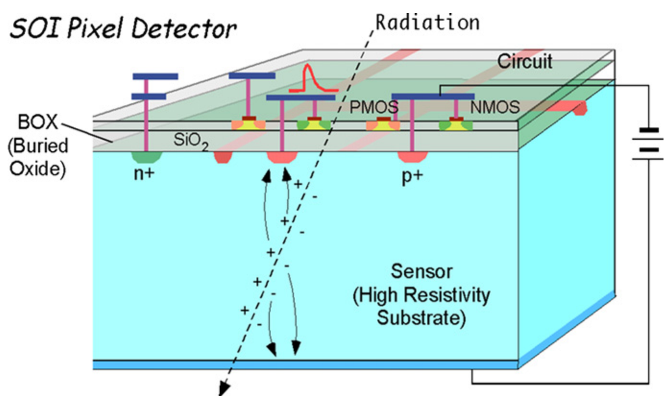

Fig. 1. Monolithic pixel device realized in bonded SOI wafer. The BOX layer separates the high resistivity detector part (n-type) and the readout electronics part. Two pixel electrodes (p^+) are drawn schematically, together with a peripheral n^+ ring for biasing from the top side.

Table 1
Main SOIPIX parameters.

process	0.20 μm Low-leakage fully depleted SOI CMOS: 1 poly Si, 4 metal layers, MIM capacitors
SOI wafer	(Top) 40 nm thick p-type of 18 Ω cm; (BOX) 200 nm; (handle) 650 μm thick n-type of 700 Ω cm
backside	Thinned to 260 μm, 200 nm Al sputtered

underneath the BOX layer, which reduces the electric field in the BOX layer by utilizing the p^+–n junction. The potential of the BPW layer is designed to be externally adjustable.

The radiation effects in the SOI devices with and without BPW were investigated by irradiating Transistor Test Element Group (TrTEG) chips, where a set of basic PMOS and NMOS transistors is implemented. Four chips were irradiated with 70 MeV protons up to a fluence of 1.2×10^{15} 1-MeV $n_{eq}\,cm^{-2}$ scaled by NIEL [15] in silicon. This fluence corresponds to the ionization dose of 0.4 MGy (SiO_2).

The transistor parameters such as threshold voltage and transconductance were characterized. Characteristic radiation effect appears in the threshold voltage shifts due, presumably, to the accumulated holes in the BOX and gate oxide (GOX) layers and to the charge states created at the silicon–oxide interfaces. A TCAD simulation [16] is employed to evaluate contributions of those charges to the measured threshold shifts. The samples and irradiation are described in Section 2, followed by the TrTEG characterization results in Section 3 and TCAD simulation in Section 4.

2. TrTEG samples and irradiation

A schematic diagram of one PMOS transistor group is shown in Fig. 2. There are similar groups of 7 NMOS or 6 PMOS transistors, each group having a common source terminal. The transistors are described briefly in Table 2. Tr7 is a depletion mode transistor having a smaller W/L ratio than others is not considered in this paper. We prepared samples with two GOX thicknesses, 4.5 (Type1) and 7.0 nm (Type2), in order to investigate the effects of radiation induced hole traps. The minimum gate length is 0.20 and 0.35 μm. In each group, there are three for each type with different thresholds and body controls. The source of Tr5 is tied to the body externally at one of the metal layers on top of the SOI device. The body of Tr6 extracted outside the chip was grounded in the measurements.

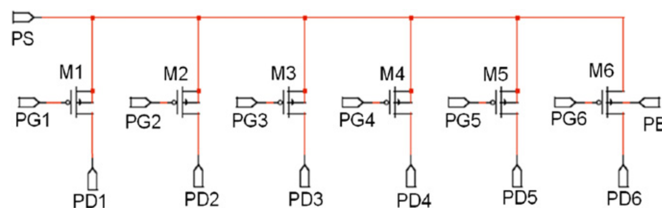

Fig. 2. One group in TrTEG consisting of six PMOS transistors.

Table 2
List of transistors in TrTEG. Type refers to the gate thicknesses.

Tr number	W/L (μm)	Type	Threshold, body control
Tr1 (NMOS)	100/0.2	1	Normal VT; floating body
Tr2 (NMOS)	100/0.2	1	Low VT; floating body
Tr3 (N/PMOS)	175/0.35	2	High VT; floating body
Tr4 (N/PMOS)	175/0.35	2	Normal VT; floating body
Tr5 (N/PMOS)	175/1.00	2	Normal VT; source tie
Tr6 (N/PMOS)	100/0.2	1	Normal VT; body control
Tr7 (NMOS)	100/10	2	Depletion mode

There are two copies of groups, one having the BPW underneath the BOX layer. Individual transistor was characterized with a HP4145A analyzer, where the four inputs were a pair of drain and gate terminals, the common source and the back-gate bias V_{BG}. The potential of the BPW was controlled externally. Terminal selection was computer controlled through a dedicated switch board consisting of miniature relays.

The proton irradiation was performed at the Cyclotron Radio Isotope Center (CYRIC) of Tohoku University. Details of the irradiation facility and methods are described elsewhere [17]. The samples were uniformly irradiated with 70-MeV protons. The evaluated NIEL fluence for the four chips were 1.3×10^{12}, 1.2×10^{13}, 6.0×10^{14}, and 1.1×10^{15} 1-MeV $n_{eq}\,cm^{-2}$. The irradiation times were between 42 and 62 min and were set by adjusting the beam current. During the irradiation, all terminals were set to the same potential but left floating. The devices were kept cooled at $-7\,^{\circ}C$ during irradiation and the irradiated samples were immediately stored in a refrigerator to suppress any post-irradiation annealing.

3. Transistor characteristics

The transistors were characterized before and after annealing, where the devices were kept for 80 min at 60 °C [18] in order to suppress short-term annealing effects after proton irradiation. We report post annealing results of PMOS Tr3–Tr6 and NMOS Tr1–Tr6 (a mistake was found in PMOS Tr1 and Tr2 circuits).

The transistor characterization was made for positive supply voltages. For NMOS (PMOS), with setting the source (drain) at 0 V, the drain current I_d was measured as a function of the gate voltage V_{gs} for two drain (source) voltage settings 0.1 and 1.8 V (1.7 and 0 V). The back bias V_{BG} was varied to 0, 5, 10, 50, and 100 V. The BPW potential was set to 0, 1.8 V, or at floating.

3.1. Threshold voltage shift by back-gate bias

The threshold voltage is defined as V_{gs}, where the I_d reaches $(W/L)\times100$ nA. The effects of back-gate bias V_{BG} on the threshold voltage are shown in Fig. 3 for non-irradiated NMOS and PMOS transistors. The data are shown for the groups without BPW and with BPW set at 0 V. The applied back-gate bias V_{BG} was positive since the sensor part is an n-type silicon. The back-gate effects to

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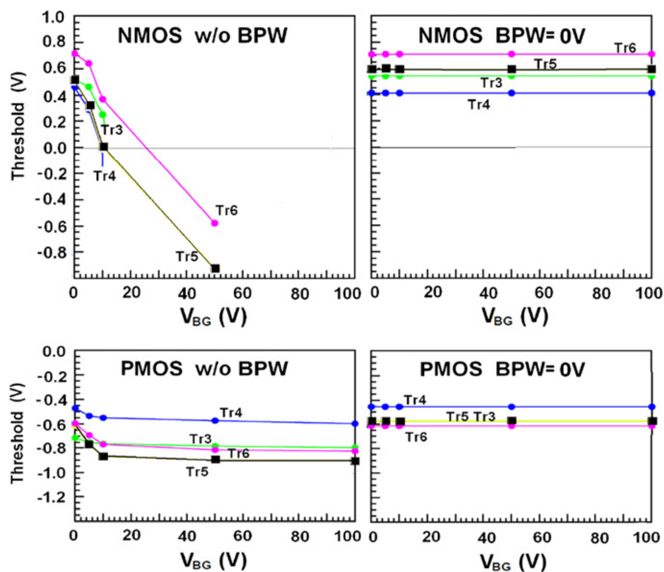

Fig. 3. Threshold voltage of non-irradiated NMOS and PMOS transistors vs. the back-gate bias V_{BG}, without and with BPW = 0 V. NMOS Tr3 and Tr4 w/o BPW showed a threshold below −0.9 V at V_{BG} = 50 V and are not shown in the figure. The transistors were characterized for a source–drain voltage difference of 1.8 V.

the NMOS transistors without BPW are larger than to PMOS. The positive bias from the backside turns on the NMOS transistors in similar way as the front gate voltage does, while for the PMOS it reduces the effective channel thickness, thus the effect is limited for PMOS. The effectiveness of the BPW is evident, as the threshold voltage is not at all affected up to 100 V bias. Note that the device can be biased up to 130 V, above which the leakage current starts to increase steeply.

3.2. Threshold voltage shift by irradiation

The radiation induced threshold voltage shifts are plotted in Fig. 4 for NMOS and PMOS transistors for groups without BPW and with BPW set at 0 V. The back-gate bias V_{BG} is 0 V. The presence of the BPW does not cause significant difference. The difference is also small for the other BPW potential settings. This is understood because the voltage shift is caused by charge traps, which is inherent irrespective of the BPW existence. We conclude that the voltage shift is not degraded by addition of the BPW.

Characteristics difference in radiation response is observed between the NMOS and PMOS transistors: the shift decreases monotonically for PMOS while it rebounds for NMOS. The threshold rebound [19] in NMOS devices is explained by excess negative interface-trap charge over the positive oxide-trap charge. The trapped holes in oxide have a faster dynamic, namely, they prevail and thermally anneal quicker compared to the interface states. Therefore, the rebound effect is technology dependent as well as radiation rate dependent. For the PMOS transistors, both trapped holes and interface states are positive and no rebound is observed.

3.3. Transconductance

Fig. 5 shows the transconductance of NMOS and PMOS Tr4–Tr6 transistors as a function of the fluence, compared between without and with BPW at 0 V. The back-gate was grounded. The transconductance of PMOS transistors Tr4 and Tr6 tend to decrease with fluence. This can be explained by the holes trapped in the BOX deplete the n channel partially, reducing the effective channel thickness. The source tied PMOS Tr5 shows better stability against radiation than the other devices.

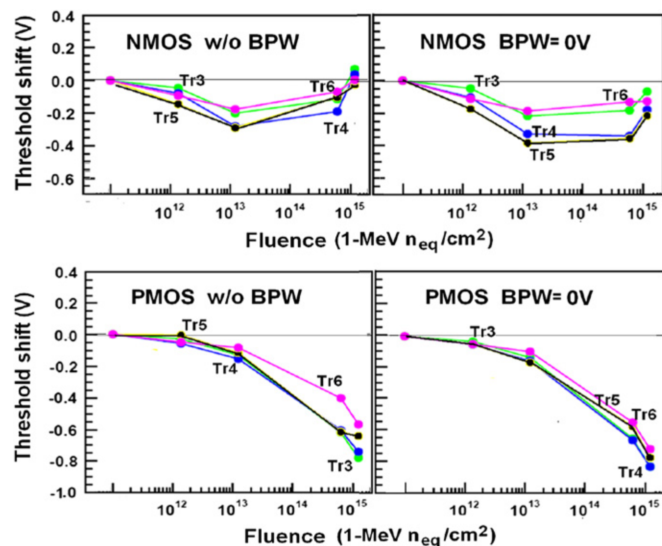

Fig. 4. Radiation induced threshold shifts for NMOS and PMOS transistors vs. radiation fluence, without and BPW = 0 V. V_{BG} = 0 V. The first points refer to the pre-irradiation values.

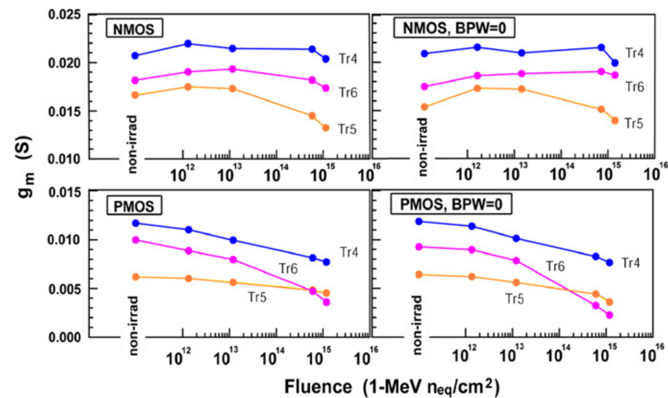

Fig. 5. Transconductance of NMOS and PMOS transistors Tr4–Tr6 as a function of fluence. The back-gate bias V_{BG} = 0.

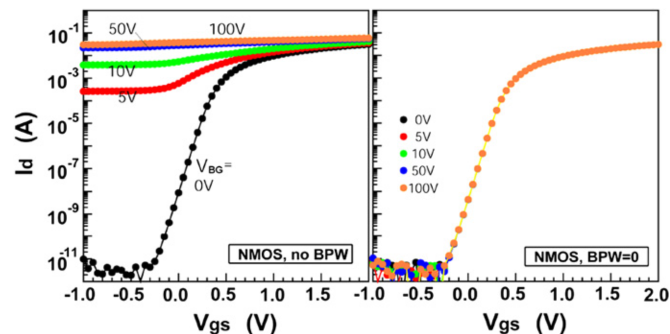

Fig. 6. The I_d–V_{gs} curves of NMOS transistor Tr4 irradiated to 1.3×10^{12} 1-MeV $n_{eq}\,cm^{-2}$ for (left) without BPW and (right) with BPW grounded. Curves are for different back-gate bias V_{BG}. V_{ds} = 2 V.

3.4. Effectiveness of BPW after irradiation

Figs. 6 and 7 show the I_d–V_{gs} curves of NMOS and PMOS Tr4 transistors irradiated to 1.3×10^{12} 1-MeV $n_{eq}\,cm^{-2}$ for varied

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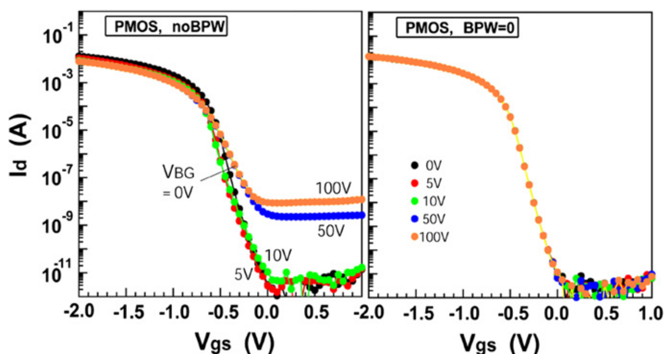

Fig. 7. The I_d–V_{gs} curves of PMOS transistor Tr4 irradiated to 1.3×10^{12} 1-MeV $n_{eq}\,cm^{-2}$ for (left) without BPW and (right) with BPW grounded. Curves are for different back-gate bias V_{BG}. V_{ds}=2 V.

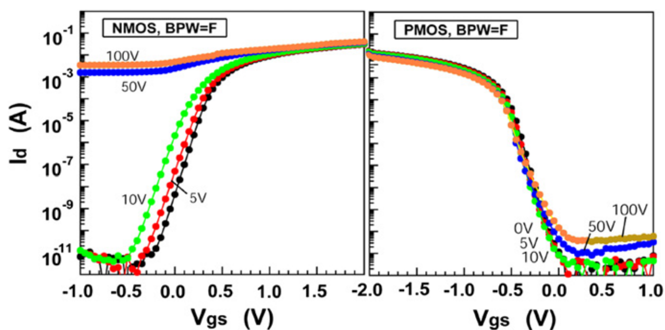

Fig. 8. The I_d–V_{gs} curves at different V_{BG} for Tr4 transistors irradiated to 1.3×10^{12} 1-MeV $n_{eq}\,cm^{-2}$ for (left) NMOS and (right) PMOS. The BPW is floating. V_{ds}=2 V.

back-gate voltage V_{BG}. With increasing the back-gate bias, curves are distorted significantly for the samples without BPW, while curves are identical with BPW set at ground and at 1.8 V. We observed also the distorted curves when the BPW was floating (see Fig. 8), which was not the case in the non-irradiated sample.

Substantial radiation-induced charge up in or around the BPW may explain the difference between BPW=0/1.8 V and at floating. The transistors irradiated to $1.2\times10^{13}\,n_{eq}\,cm^{-2}$ (4 kGy) and above did not suppress the back-gate effect even with the BPW set at ground. We continue to investigate this issue such as increasing the BPW doping density and irradiation in a condition, where the BPW potential is tied to the ground.

4. TCAD simulation of threshold shift

4.1. Contributions of charge traps to the threshold

Technology Computer Aided Design (CAD) is intensively used for modeling semiconductor fabrication and device operation. We employed TiSSiEN program of TCAD International, Inc. [16,20].

The transistors are first modelled in "Device simulation" part of TCAD to reproduce the non-irradiated transistor characteristics. As discussed in Section 3.2, the difference in radiation induced threshold shifts is not significant between transistors with and without BPW. In the following, we simulate transistors with no BPW and no back-gate bias applied. Radiation induced threshold shifts were realized by positive charges uniformly added in the GOX and BOX layers, and by charge states at the GOX–body and body–BOX as well as BOX–substrate interfaces. The interface states can be negative for NMOS and positive for PMOS transistors.

Fig. 9 illustrates the individual contributions of the interface charges to the threshold shift, evaluated in the modelled NMOS Tr4 (normal threshold Type2). The charge densities other than under consideration are zero in this plot. Simulation results are similar in shape for other types of transistors, including PMOS.

The radiation induced interface charge density should be scaled in terms of sheet density in the first order approximation, although the different oxide forming technologies make this assumption less reliable. As shown in Fig. 9, the BOX–substrate interface charge state contribution is negligible, and GOX–body and body–BOX contributions are similar up to $5\times10^{11}\,cm^{-2}$. We have checked that the latter two interface contributions are additive to the threshold shift. This leads to a conclusion that describing sheet densities at both GOX–body and body–BOX interfaces with single parameter is effective up to $5\times10^{11}\,cm^{-2}$, the density being regarded as the average at the two interfaces.

The individual contributions of the hole densities in the oxide layers are dependent on the transistor type. Fig. 10 shows examples for PMOS Tr4 and Tr6. In general, the BOX contribution is dominant at small hole densities. The magnitude of the BOX contribution is dependent on the channel impurity concentration, the larger the concentration the smaller the magnitude of ΔVth. Among these, Tr6, normal Vth transistor with thinner GOX, has the largest concentration. The threshold shift due to the BOX seems to saturate above a few $\times10^{17}\,cm^{-3}$. The BOX contribution is surpassed by the GOX at higher densities. The magnitude of the GOX contribution is smaller for Tr6 since the GOX is thinner for Tr6.

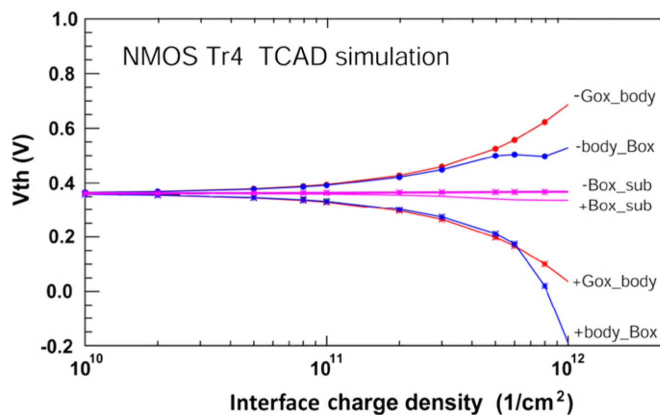

Fig. 9. Interface charge contributions to the threshold voltage. Curves labeled-Gox–body, -body–Box and -Box–sub are for the cases negatively charged.

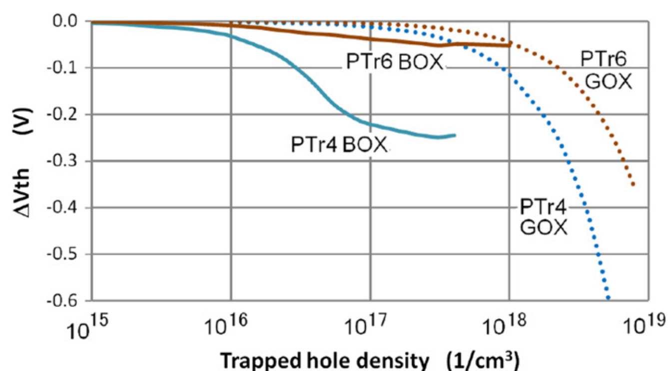

Fig. 10. Threshold shifts due to oxide trapped hole density in the GOX and BOX layers, shown for PMOS Tr4 and Tr6.

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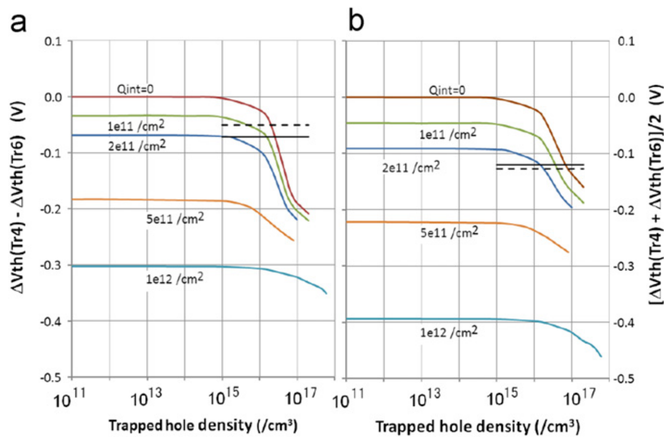

Fig. 11. Difference (a) and average (b) of the threshold shifts for PMOS Tr4 and Tr6, as a function of the hole density trapped in the oxide layers simulated for several interface charge densities. The data at fluence of $1.2 \times 10^{13}\ n_{eq}\ cm^{-2}$ are shown as horizontal bars for the transistors with (dashed) and without (solid) BPW.

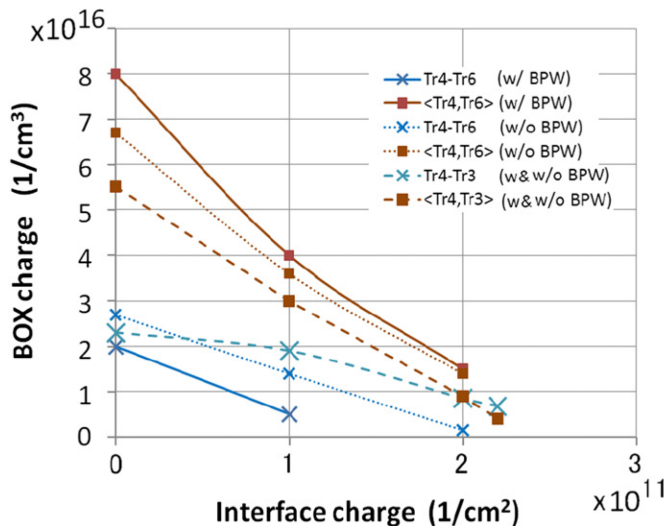

Fig. 12. Candidate interface and BOX charge densities at $1.2 \times 10^{13}\ n_{eq}\ cm^{-2}$ irradiation. Evaluations are made based on PMOS Tr4 and Tr6, and Tr3 and Tr4 pairs.

The radiation induced GOX and BOX hole densities should be scaled in terms of volume density, while effects such as hole tunneling and recombination may contribute differently. Fig. 10 describes that the BOX or GOX contribution is dominating in different hole density ranges, providing a conclusion that the threshold shift to ~0.2 V (~0.03 V) is due to the BOX charge and beyond is due to GOX for PMOS Tr4 (Tr6).

4.2. Comparison with the data

The difference and average of the PMOS Tr4 and Tr6 threshold shifts are simulated at the same GOX/BOX charge densities for several interface charge state densities. The results are shown in Fig. 11. Note that the horizontal axis is essentially due to the BOX hole density at a shown concentration range. Also shown in the figure are the corresponding measurement data, providing candidate combinations of the interface and BOX charge densities.

The candidate combinations are given in Fig. 12. The data both with and without BPW at $1.2 \times 10^{13}\ n_{eq}\ cm^{-2}$ irradiation are used, in addition to the combinations obtained from the Tr3 and Tr4 pairs (the shifts are identical for these samples with and without BPW). This fluence is chosen because the BOX contribution should be dominant in the measured threshold shift range, as shown in Fig. 10. Since the BOX layer is identical, all curves are expected to have a common point within uncertainty. The best estimate seems to be located at around the effective interface charge of $2 \times 10^{11}\ cm^{-2}$ and the BOX trap density $< 2 \times 10^{16}\ cm^{-3}$.

The threshold shifts at the fluence of $6 \times 10^{14}\ n_{eq}\ cm^{-2}$ and above should be explained mainly by the GOX hole density with a saturated BOX contribution, together with the interface charge contributions. The evaluation is in progress, including combinations of other transistor data and sub-threshold swing values, which are expected to provide more reliable and precise determination of the different charge layers and densities contributing to the threshold voltage shift.

5. Summary

We are evaluating radiation effects in OKI 0.20 μm FD-SOI devices caused by proton irradiation. The BPW suppresses the back-gate effect completely for non-irradiated samples and samples irradiated to $1.3 \times 10^{12}\ n_{eq}\ cm^{-2}$. The threshold shifts in NMOS are shown to rebound above $10^{13}\ n_{eq}\ cm^{-2}$ and become nearly zero around $10^{15}\ n_{eq}\ cm^{-2}$ (0.4 MGy in SiO_2), while those for PMOS decrease monotonically. The BPW is found not to induce extra radiation damage in the transistor performance, threshold voltage shifts and transconductance when the samples were irradiated with no back biasing. With a bias it is expected that the BPW which reduces the electric field in the BOX layer should increase the probability of recombination of holes before they are trapped, thus reducing the radiation effect.

The measured threshold shifts are expected to be explained by the hole density trapped in the oxide layers and the density of charge states at the silicon–oxide interfaces. We described a method of evaluation of these effects with the help of a TCAD simulation.

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