Total Ionization Damage Effects in Double Silicon-on-Insulator Devices

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***Abstract*– We are developing monolithic pixel sensors based on a 0.2 µm fully-depleted silicon-on-Insulator (SOI) technology. The major issue in applications them in high-radiation environments is the total ionization damage (TID) effects. The effects are rather substantial in the SOI devices since the transistors are enclosed in the oxide layers where generated holes are trapped and affect the operation of the near-by transistors. The double SOI sensors that provide an independent electrode underneath the buried oxide layer have been developed. We have irradiated transistor test elements and pixel sensors with γ-rays. By adjusting the potential of this electrode, the TID effects are shown to be compensated. The pixel sensor irradiated to 20 kGy recovered its functionality by applying a bias to the electrode. The radiation tolerance of the SOI devices has been substantially improved by the double SOI.**

I. Introduction

THE potentiality of novel monolithic pixel devices utilizing the 0.2-µm fully depleted silicon-on-insulator (FD-SOI) technology provided by Lapis Semiconductor [1] has been intensively explored for various applications including space, γ/X-ray imaging, high-energy, and other applications [2][3][4][5]. Our technology characteristics, in addition to utilization of the commercial reliable process, is adaption of bonded wafers provided by SOITEC Co.[6] We adopt high resistive silicon as the SOI handle wafer to use it as the sensing part. A schematic diagram of typical SOI pixel device is illustrated in Fig. 1. Nominally the top is 40-nm thick silicon of 18 Ωcm, separated by a 200-nm thick buried oxide (BOX) layer with the handle wafer. Table 1 summarizes the Lapis FD-SOI process, where the silicon types and resistivity values adopted so far are also shown. Thicker devices (up to 700 µm thickness) are of particular useful for X-ray detectors while thin devices (down to 50 µm) for high-energy physics applications, both being able to be fully depleted.

There are a couple of issues to solve, though, have become obvious. The back-gate effect where the voltage applied to the back as the detector bias affects the operation of top-side circuit. This has been diminished by applying BPW (buried p-well) for p-type pixel nodes (BNW for n-type pixel nodes), as also illustrated in the figure. The potential of such electrodes is stabilized externally or by the pixel node.

Another issue is that the total ionization damage (TID) effect [7] is rather substantial since each SOI transistor is fully enclosed in oxide and the holes trapped in the oxide layers shift negatively the transistor threshold [8][9][10]. The operation of the transistors, e.g., threshold voltages, should be restorable by applying negative voltage to the positively

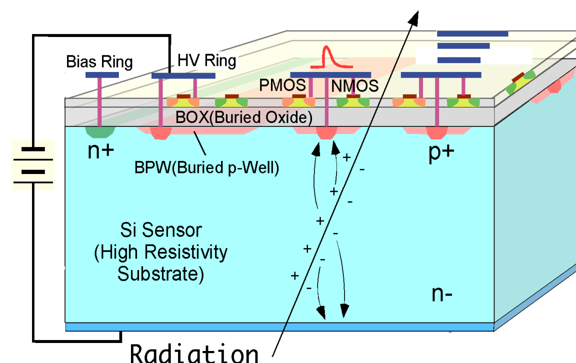

Fig. 1. Schematics of SOI monolithic pixel device. The pixel electrodes, fabricated through the BOX layer, and SOI MOS transistor terminals are interconnected via metal layers on top of the device. The device is biased from the back or from the front n^+ contact (Bias Ring).

Table 1. Main Process Parameters

Process	0.2µm low leakage fully-depleted SOI CMOS 1 poly+5 metal layers, MIM (1.5 µF/µm^2), DMOS Core (I/O) voltage=1.8 (3.3)V
SOI wafer	Diameter : 200 mmϕ Top Si : Cz ~18Ωcm (p-type) ,40 nm thick Buried oxide: 200 nm thick Handle wafer: Cz(n, 0.7kΩcm), FZ(n,7k),FZ(p,25k) Double SOI available
Backside	Mechanical grind (down to 200 µm), chemical etching, implant, laser annealing, Al plating Further thinning to (50,100 µm) available

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charged area. The developed BPW is not suitable for this purpose because of the potential configurations among the pixel node, BPW, and the back. The BNW with n-type pixel nodes may be effective provided that the sheet resistance is low enough. The additional BPW/BNW electrodes, though, modify the detector capacitance, hence the response shape, and tend to increase the coupling noise among the circuitry through this common electrode.

Recently double SOI wafers were fabricated by SOITEC per our request. Their patented SmartCut^{TM} process was repeated twice to form two sets of silicon and BOX pair layer. Usual electronics part is processed on the top silicon, whereas the second silicon layer is used as an individual electrode that can control the potential to suppress the TID effect. Also the same layer should be effective to suppress the back-gate effect and the noise coupling.

We have fabricated transistor test element groups (TrTEG) and conducted Co γ irradiation to investigate the effectiveness of the double SOI in TID suppression. The functionality of a whole pixel device was examined by irradiating integration type pixel sensors INTPIXh2.

II. Double SOI Process and Tested Samples

The double SOI wafers provided by SOITEX employ p-type Cz silicon (10-18 Ωcm) for top and second (middle) layers of about 80 nm thickness each, and a handle wafer of n-type Cz 700 Ωcm. The top two layers are interleaved with a SiO_2 layer (BOX2) of 150 nm thickness, and the middle layer and the handle wafer with BOX1 of another 150 nm thickness. (The values are typical.) Fig. 2 is a TEM image showing one set of transistor at left and a pixel node reaching through to the handle wafer. Connections to the gate and to the middle layer are provided in a different slice cross-section. The sheet resistance of the middle layer is 170 kΩ/sq with $CoSi_2$ layer fabricated on top and 1 MΩ/sq without.

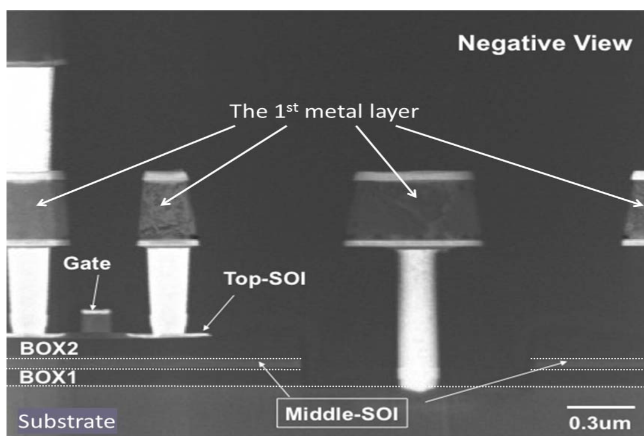

Fig. 2. TEM image of a double SOI transistor and a pixel node.

Table IIA. Characterisitics of 11 Transistors in TrTEG_o. L and W are in microns; M shows the number of transisitors tied in series to effectively lengthen W. LV T: low-voltage threshold, NVT: normal-voltage threshold, HVT: high-voltage threshold. There are two types of source-tie (tie and tie2).

TR	L	W	M	Comment
0	0.20	5	1	LVT
1	0.20	5	1	NVT
2	0.40	5	1	NVT_S-TIE2
3	0.35	5	1	NVT_S-TEI2
4	0.20	5	1	NVT_S-TIE
5	0.35	5	1	IOHVT
6	0.35	5	1	IONVT
7	0.40	5	1	IOHVT_S-TIE2
8	0.35	5	1	IONVT_S-TIE2
9	0.35	5	1	IONVT_S-TIE
10	0.40	2.5	2	NVT_S-TIE2

Table IIB. Charatceristics of 18 transistors in TrTEG6. MULT_B-TIE : multiple body tie. The effective W/L is 100 for all.

TR	L	W	M	Comment
0	0.20	5	4	NVT
1	0.50	5	10	NVT
2	1.00	5	20	NVT
3	0.20	5	4	LVT
4	0.50	5	10	LVT
5	1.00	5	20	LVT
6	0.35	5	7	IOHVT
7	0.35	5	7	IOHVT
8	0.20	5	4	LVT_S-TIE
9	0.50	5	10	LVT_S-TIE
10	1.00	5	20	LVT_S-TIE
11	0.40	10	4	NVT_S-TIE2
12	0.60	6	10	NVT_S-TIE2
13	1.00	5	20	NVT_S-TIE2
14	0.20	5	4	NVT_MULT_B-TIE
15	0.50	5	10	NVT_MULT_B-TIE
16	1.00	5	20	NVT_MULT_B-TIE
17	1.00	5	20	IONVT_S-TIE

We evaluated the radiation damage using two versions of TrTEG, TrTEG_o and TrTEG6, where various transistors were fabricated as listed in Tables IIA and IIB. There are in total 29 transistor types each for PMOS and NMOS. The W/L ratios range from 25 to 100. The core transistors (t_{OX}=4 nm)

include low (LVT) and normal (NVT) threshold types, and IO (t_{OX}=7 nm) include normal (IONVT) and high (IOHVT) threshold types. We examined source-tie schema with two versions for both core and IO, and multiple body ties for the core.

The INTPIXh2 sensor is composed of pixels of 18 μm square, which has an on-pixel circuit as shown in Fig. 3. The pixel outputs in the same column are sent out one after the other to a 12-bit ADC located outside the chip. Since the irradiation was performed on a chip basis, the functionality of the on-pixel circuits and a common on-chip peripheral circuit including output buffers and switching logics was examined.

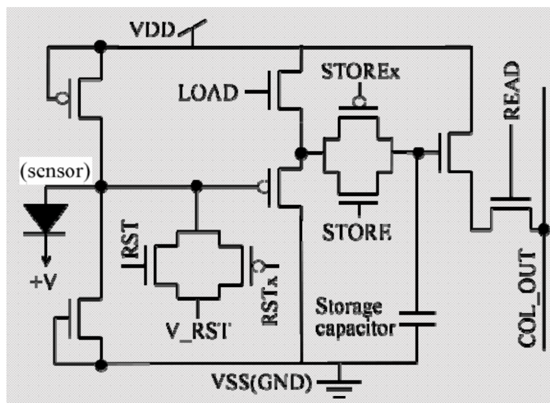

Fig. 3. On-pixel circuit employed in INTPIXh2. Analog data is extracted to an off-chip 12-bit ADC through COL_OUT via buffer amplifier.

III. COBALT IRRADIATION AND EXAMPLE CHARACTERISTICS

The ^{60}Co γ irradiation was performed at Takasaki Advanced Radiation Research Institute, JAEA. The total dose ranged from 500 Gy up to 200 kGy for TrTEG samples and up to 20 kGy for INTPIXh2. Most of the samples were irradiated with all the terminals grounded. Some TrTEG6 samples for 20 kGy irradiation were examined in other biasing conditions, which is detailed in later section. The irradiation was performed at room temperature. The samples, each received the target dose for a time span of typically 20 h, were brought to University of Tsukuba in four hours and then kept refrigerated at −20°C except during the characterization measurements.

Fig. 4 shows a typical example (TrTEG6 no.14) of I_D-V_G curves measured at pre-irradiation and at different doses with the middle SOI voltage V_{SOI2}=0 V. The curves were obtained at V_D=1.8 V and V_S=0 V for NMOS, and V_D= −1.8 V and V_S=0 V for PMOS. For both NMOS and PMOS, the curve shifts negatively as accumulating the dose, as expected that the holes trapped in the oxide effectively reduce the required transistor threshold voltage. The transistor performance was characterized by three quantities:

(1) threshold voltage (V_{th}), defined as V_G at I_D=100 W/L [nA]
(2) trans-conductance (g_m), g_m in [S]
(3) sub-threshold swing (S), S in [V/dec]

The threshold voltages for a typical sample are shown in Fig. 5 as a function of the dose for different V_{SOI2} settings. By properly adjusting V_{SOI2}, the threshold voltage can be restored to the original value. Similar plots for the trans-conductance and swing compensations are shown in Fig. 6. In the following, the curves are used to determine the V_{SOI2} voltage per dose to restore each of the three transistor quantities to the pre-irradiation value measured at V_{SOI2}=0; we call the voltage as optimum V_{SOI2}.

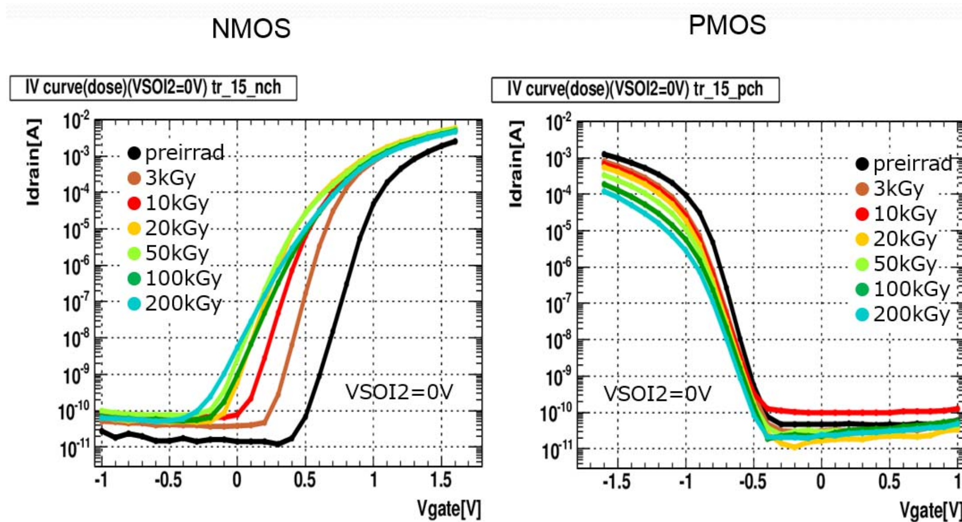

Fig. 4. I_D-V_G curves for typical (left) NMOS and (right) PMOS transistors, measured at V_{SOI2}=0 V. The curve shifts negatively with accumulating the dose.

IV. Compensation by SOI2

A. Compensating threshold voltage shift

The optimum V_{SOI2} voltages are plotted in Fig. 7 to compensate the threshold voltage shifts. The data are shown separately for core and IO transistors, and for NMOS and PMOS. While the PMOS shows a monotonic decrease with the dose, there are two groups for the NMOS, clearly separated by either body-floating or source-tied. The trend of body-floating transistors is illustrated by the phenomenon called ``rebound'' [11]. The Si-SiO_2 interface traps generated by irradiation are negatively charged for NMOS, which partially compensate the effects caused by hole traps in the oxide. The interface traps are dependent on oxide processing and conditions such as applied voltage at irradiation. Source-tied NMOS transistors manifest smaller compensating effects, hence larger V_{SOI2} is required. No noticeable difference is observed between core and IO transistors.

B. Compensating g_m and S shifts

Fig. 8 shows the optimum V_{SOI2} to compensate the trans-conductance and sub-threshold shifts. Since g_m variation with dose is moderate for NMOS, the optimum voltages apparently differ between NMOS and PMOS.

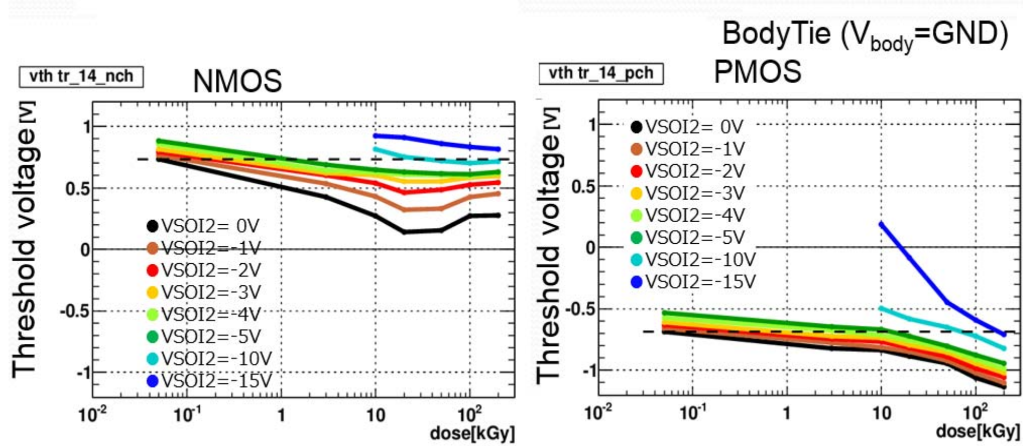

Fig. 5. Threshold voltages as function of dose for (left) NMOS and (right) PMOS. Different curves are for V_{SOI2} varied from 0 to -15 V. The dashed lines indicate the threshold voltage of the pre-irradiation sample measured at V_{SOI2}=0 V.

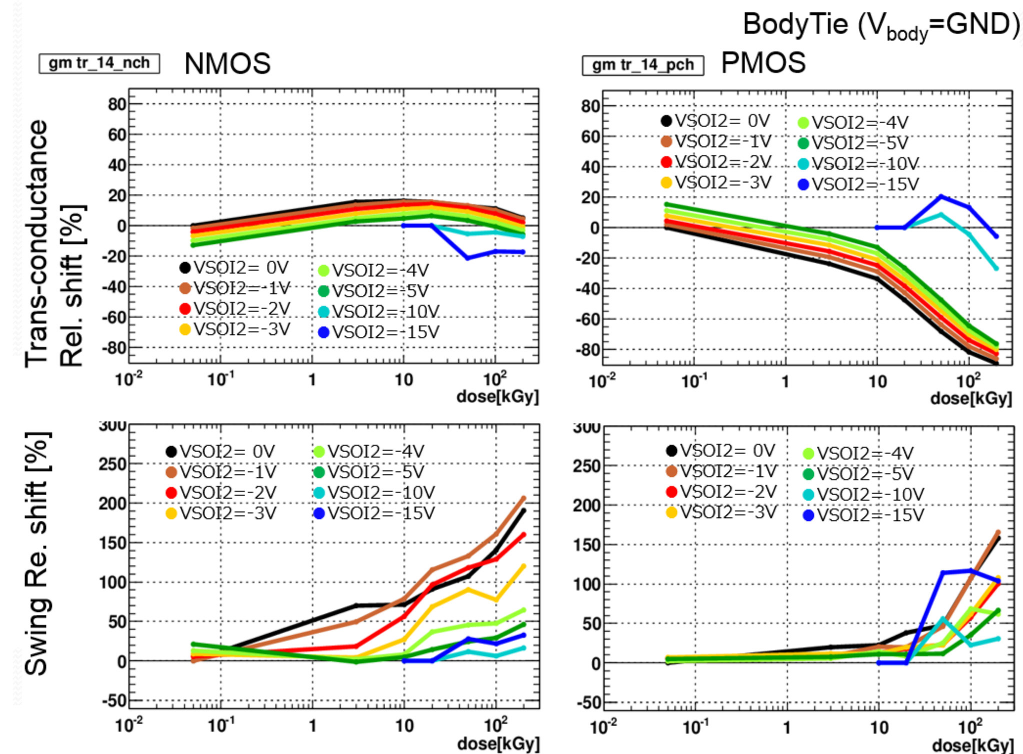

Fig. 6. (Top) Trans-conductance shifts and (above) swing shifts in percentage as function of the dose. Left: NMOS and Right: PMOS. Different curves are for V_{SOI2} varied from 0 to -15 V

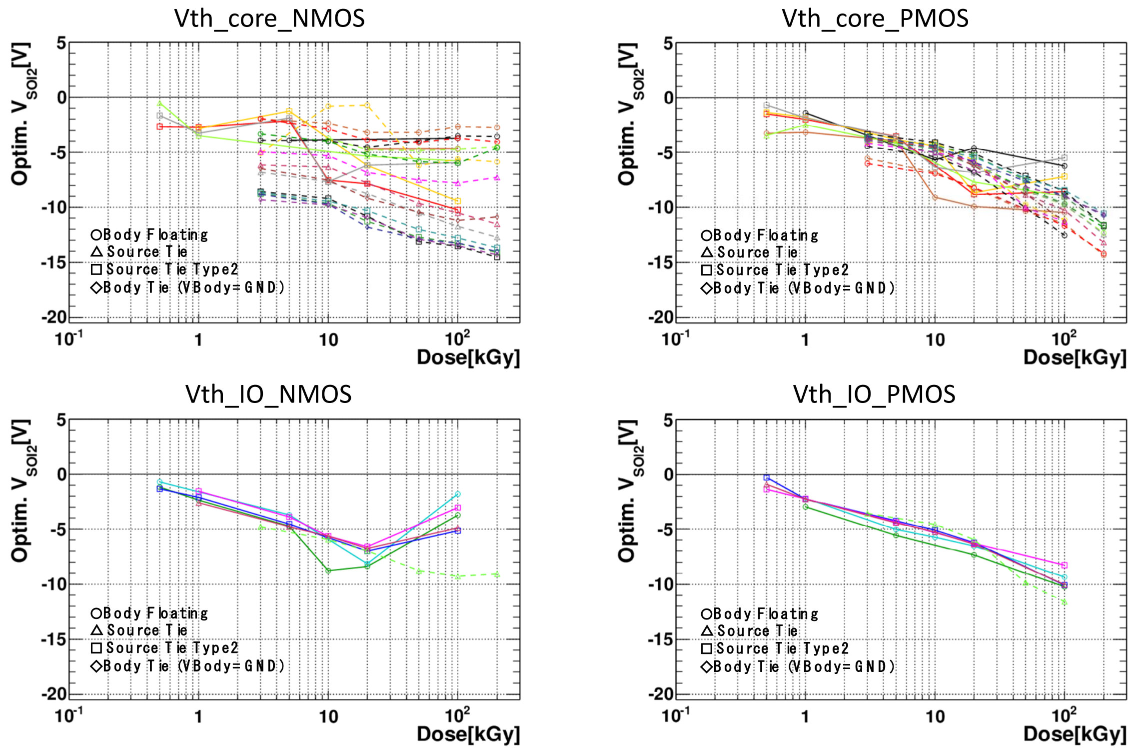

Fig. 7. Optimum V_{SOI2} voltages as function of dose to compensate the threshold voltage shifts. The data are shown for all the tested transistors separately for the core (top) and IO (above) transistors, and for (left) NMOS and (right) PMOS.

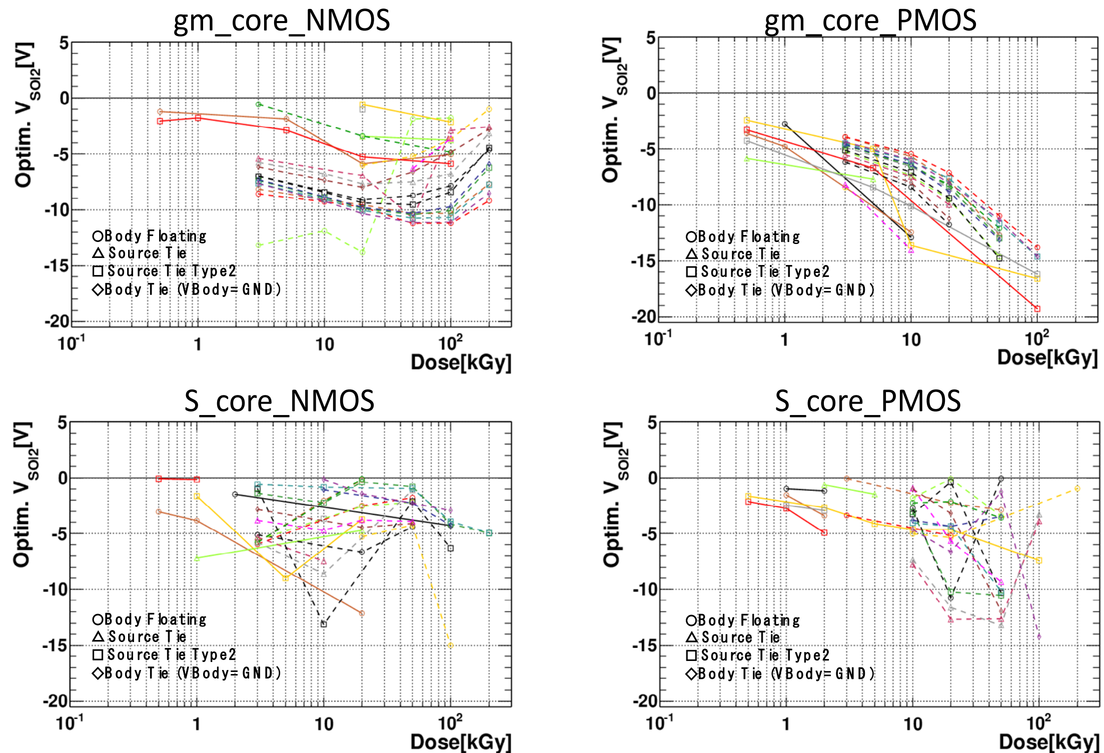

Fig. 8. Optimum V_{SOI2} voltages as function of dose to compensate (top) the trans-conductance shifts and (above) sub-threshold shifts. The data are shown for all the tested transistors separately for (left) NMOS and (right) PMOS.

C. Dependence on biasing

The effect of biasing configuration during irradiation was evaluated at one irradiation point of 20 kGy. The threshold voltages for a typical sample are summarized in Fig. 9. With the condition V_{DS}=1.8 V and V_G=0 V (V_S=0 V for NMOS and V_D=0 V for PMOS), the threshold shift becomes larger for NMOS while it becomes smaller for PMOS. This is understandable since the potential of gate is lower (higher) in NMOS (PMOS) than the body potential, demoting (promoting) holes in the gate oxide to recombine. This mechanism is diminished when V_{SOI2} is set negative.

V. PIXEL RESPONSE

The functionality of the pixel sensor as a whole was examined by irradiating four pixel sensors to the dose from 1 kGy to 20 kGy. The electronics functionality evaluated as the response to reset voltages RSTV (see Fig. 3) is presented in Fig. 10. The output pulse height increases with the dose for the same RSTV, reaching the ADCs full count range. The response curve is mostly restored by applying V_{SOI2}. At V_{SOI2}= −7 V, the threshold voltage of the main PMOS transistor, shown in Fig. 3, is expected to be compensated at 20 kGy (see Fig. 7). Since multiple and various transistors are

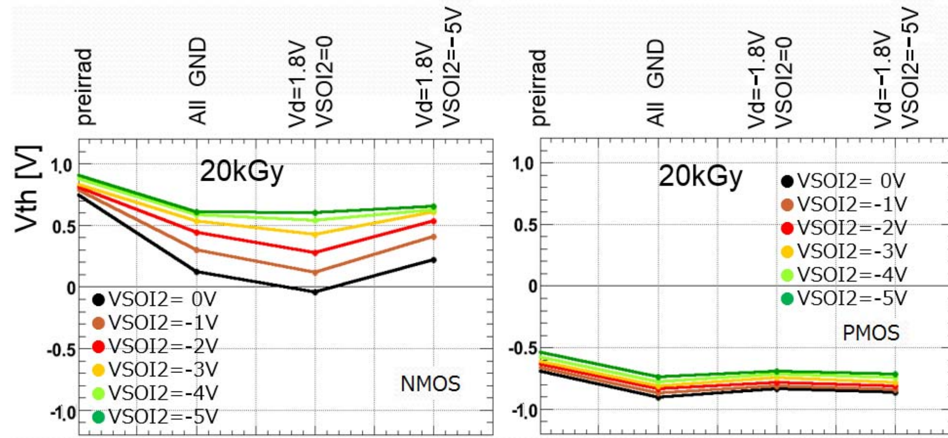

Fig. 9. Threshold voltages for samples irradiated to 20 kGy for (left) NMOS and (right) PMOS. The data are compared among different biasing conditions during irradiation: all terminals were grounded; V_{DS}=1.8 V and V_{SOI2}=0 V; V_{DS} =1.8 V and V_{SOI2}= −5 V. TR6 of TrTEG6.

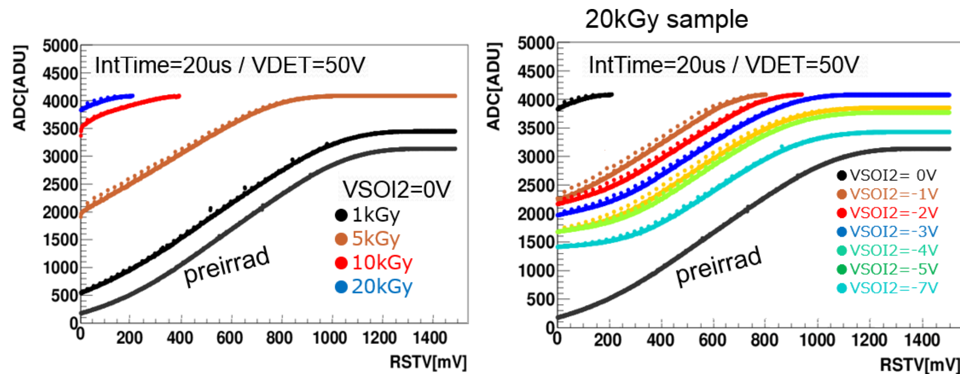

Fig. 10. Response measured with varying RESET Voltage (RSTV). (Left) Samples irradiated to 1 kGy to 20 kGy and measured at V_{SOI2}=0 are compared with pre-irradiation sample. (Right) Sample irradiated to 20 kGy is measured with varying V_{SOI2} voltage. In both measurements the sensors were biased at 50 V. The ADC is 12 bits.

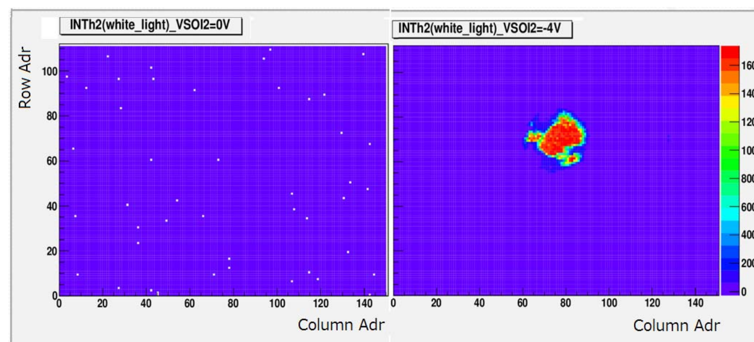

Fig. 11. Response to white light of the sample irradiated to 20 kGy are measured at (left) V_{SOI2}=0 V and (right) V_{SOI2}= −4 V.

involved in the circuit, the response curve is not completely back to the original curve, yet the functionality as a pixel device is recovered.

The recovery is clearly seen in the pixel response to white light spotted around the chip center, as shown in Fig. 11. While the response is almost saturated at V_{SOI2}= 0 V, showing small signal ADC counts, the spot image is obtained by setting V_{SOI2} at –4 V.

VI. Summary

We have evaluated the TID effects in the newly developed double SOI devices, demonstrating that the TID effects in the SOI transistors are mostly compensable by V_{SOI2} adjustment in the dose range up to 200 kGy. The pixel devices irradiated up to 20 kGy showed substantial recovery in response, although periodical calibration should be required to maintain the original performance.

The optimum V_{SOI2} is found to show some modest differences among the samples, NMOS and PMOS, source-tied and body floating, depending on the transistor characteristics values (threshold voltage, trans-conductance, sub-threshold swing) to compensate. Differences depending on the biasing condition during irradiation are observed.

In summary, the radiation tolerance has been enhanced substantially by employing the innovative double SOI. Under consideration of the observed differences and the impact factors of the individual transistors in view of the required pixel performance, it should be possible to design radiation tolerant devices. The present study encourages us and designing SOI pixel sensors for future collider experiments is set forward.

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References

[1] Lapis Semiconductor Co., Ltd.: http://www.lapis-semi.com/en/.

[2] T. Tanaka et al., “Development of SOI Pixel Sensors for X-Ray Astronomy”, presented at this symposium, N1-4; A. Takeda et al., “Development of New Circuit for X-ray Astronomical SOI Pixel Detector”, presented at this symposium, NPO2-124.

[3] T. Hatsui et al., “Line-Spread Function and Noise Spectrum Analysis of a Direct-Detection X-Ray CMOS Image Sensor with 500 µm Thick High Resistivity Silicon”, presented at this symposium, M14-4; S. Ono et al., “Noise Analysis of a Silicon-on-Insulator (SOI) Pixel Sensor with 500 µm Thick High Resistivity Silicon for X-Ray Free-Electron Laser Experiments”, presented at this symposium, NPO1-11.

[4] T. Miyoshi et al., “Evaluation Test of SOI Monolithic Pixel Detectors with High-Speed Readout Electronics”, presented at this symposium, NPO1-3; K. Hara et al., “Development of FD-SOI Monolithic Pixel Devices for High-Energy Charged Particle Detection”, IEEE NSS, 23 Oct-29 Oct 2011, Valencia, CR-N21-1.

[5] D. Nio et al., “Investigation of Geiger-Mode APD Using SOI Technology”, presented at this symposium, NPO1-86; Y. Sekiguchi et al., “Basic Performance of SOI Pixel Detectors for Radiation Monitor”, presented at this symposium, NPO1-184.

[6] SOITEC: http://www.soitec.com/en/technologies/smart-cut/

[7] J. R. Schwank, M. R Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, “Radiation Effects in MOS Oxides,” *IEEE Trans. Nucl. Sci.*, vol. 55-4, p. 1833, 2008.

[8] K. Hara et al., ”Radiation Resistance of SOI Pixel Devices fabricated with OKI 0.15um FD-SOI Technology.” IEEE *IEEE Trans. Nucl. Sci.*, vol. 56-5, October 2009, pp. 2896-2904.

[9] K. Hara et al., "Development of INTPIX and CNTPIX Silicon-On-Insulator Monolithic Pixel Devices", PoS (Vertex2010) 033.

[10] M. Kochiyama et al., “Radiation effects in silicon-on-insulator transistors with back-gate control method fabricated with OKI Semiconductor 0.20 µm FD-SOI technology”, Nucl. Instr Meth A636 (2011) S62.

[11] J. R. Schwank, P. S. Winokur, P. J. McWhorter, F. W. Sexton, P. V. Dressendorfer, and D. C. Turpin, “Physical mechanisms contributing to device “Rebound,” *IEEE Trans. Nucl. Sci.*, vol. NS-31, p. 1434, 1984.