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# Nuclear Instruments and Methods in Physics Research A

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## Silicon strip detectors for ATLAS at the HL-LHC upgrade

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### For the ATLAS Upgrade Silicon Strip Community

#### ARTICLE INFO

##### Keywords:

Silicon strip detector  
HL-LHC  
ATLAS

#### ABSTRACT

The present ATLAS silicon strip tracker (SCT) and transition radiation tracker (TRT) are to be replaced with new silicon strip detectors as part of the inner tracker system (ITK) for the Phase-II upgrade of the Large Hadron Collider, HL-LHC. We have carried out intensive R&D programs based on n<sup>+</sup>-on-p microstrip detectors to fabricate improved radiation hard strip detectors that can survive the radiation levels corresponding to the integrated luminosity of up to 3000 fb<sup>-1</sup>. We describe the main specifications for this year's sensor fabrication and the related R&D results, followed by a description of the candidate schema for module integration.

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## 1. Introduction

Silicon microstrip detectors have been playing essential roles in high-energy physics experiments for their excellent precision tracking capability and robust operation even at locations close to the interaction region. The ATLAS experiment at the Large Hadron Collider (LHC) is due to undergo phased detector upgrades [1,2] in tandem with the planned accelerator upgrades. The beam luminosity after the Phase-II upgrade of the LHC, termed the HL-LHC (high luminosity LHC), is expected to reach  $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  instantaneously. The ATLAS experiment is set to accumulate 3000 fb<sup>-1</sup> of proton–proton collisions at a center-of-mass energy of 14 TeV.

For the HL-LHC, the present ATLAS inner detector will be replaced with an all-silicon tracker composed of pixel layers and strip layers. We are carrying out intensive R&D studies to construct a detector that can achieve physics goals of the HL-LHC. The studies are currently under review and are to be summarized in a Letter of Intent (LoI). We describe the latest evaluation of the strip detectors that are to be constructed for the HL-LHC.

## 2. Inner detector layout

The baseline layout of the new inner tracker ITK is shown in Fig. 1. The barrel part is composed of four layers of pixels and five layers of strips with additional rings. The rings are to be used to

recover the reduction in the number of hits in the barrel-to-end-cap transition region. Each strip layer should provide space points from pairs of small stereo readout strips. The layout aims to have at least 14 silicon hits everywhere down to  $\eta = 2.5$ . Our experience with the current detector indicates that we need at least 11 hits on a track to avoid the creation of fake tracks in the foreseen high pile-up environment. The designed configuration should ensure robust tracking at the HL-LHC, thereby allowing a few dead modules and holes in coverage to be present.

In order to cope with the expected five-fold increase in luminosity to  $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ , the barrel strips at the three radii close to the interaction region are 2.4 cm long while the other layers are 4.8 cm long (current SCT strips are 12 cm long), and both having a pitch of 74.5  $\mu\text{m}$  (the current pitch is 80  $\mu\text{m}$ ). As per the proposed layout, the barrel and end-cap strip detectors have respectively 122 and 70 m<sup>2</sup> area and 47 M and 27 M readout channels.

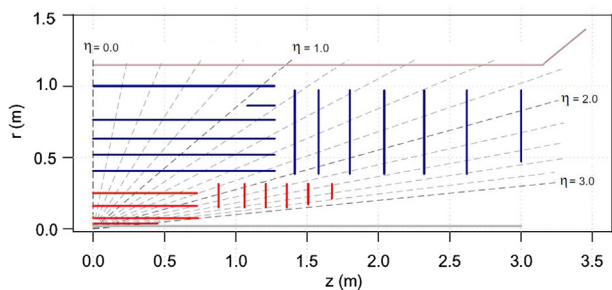
The fluence, which is evaluated from a simulation, is found to be in agreement within 20% of the measurement values [3]. The lifetime fluence calculation is available for the previous detector configuration. The fluence values are up to  $1.2 \times 10^{15} \text{ 1-MeV n}^{\text{eq}}/\text{cm}^2$  for the short barrel strips and up to  $0.56 \times 10^{15} \text{ 1-MeV n}^{\text{eq}}/\text{cm}^2$  for the long barrel strips, after including a safety factor of 2 [4]. The revised estimations in the proposed detector configuration are in progress [3].

Fig. 2 shows the expected momentum resolutions at 1, 10 and 100 GeV/c, obtained from an analytical calculation. Further, the current inner detector resolutions are indicated by broken-line curves. The outer radii strips are designed to be set at large radii while accommodating the neutron poly-moderator, and the positions of the end-cap discs are optimized to minimize the  $\eta$  variation

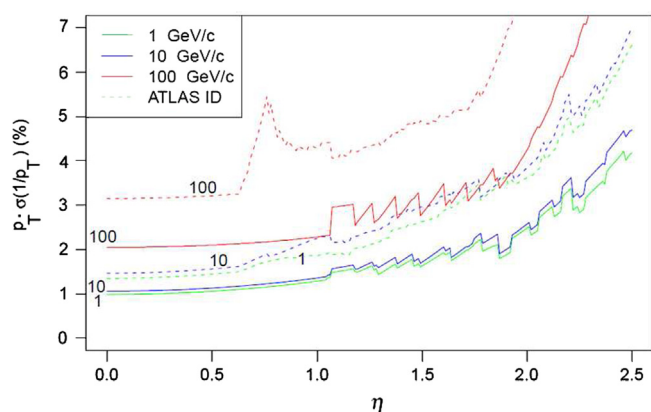
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in resolution; these design changes are estimated to improve the resolution of the new ITK over that of the current inner detector.



**Fig. 1.** Baseline quarter  $r$ - $z$  longitudinal view (LoI layout) of new ATLAS inner tracker (active areas) for HL-LHC.



**Fig. 2.** Estimated  $p_T$  resolution for different momenta. Dashed curves indicate resolutions for the current version of ATLAS. Resolutions were obtained using an analytical calculation.

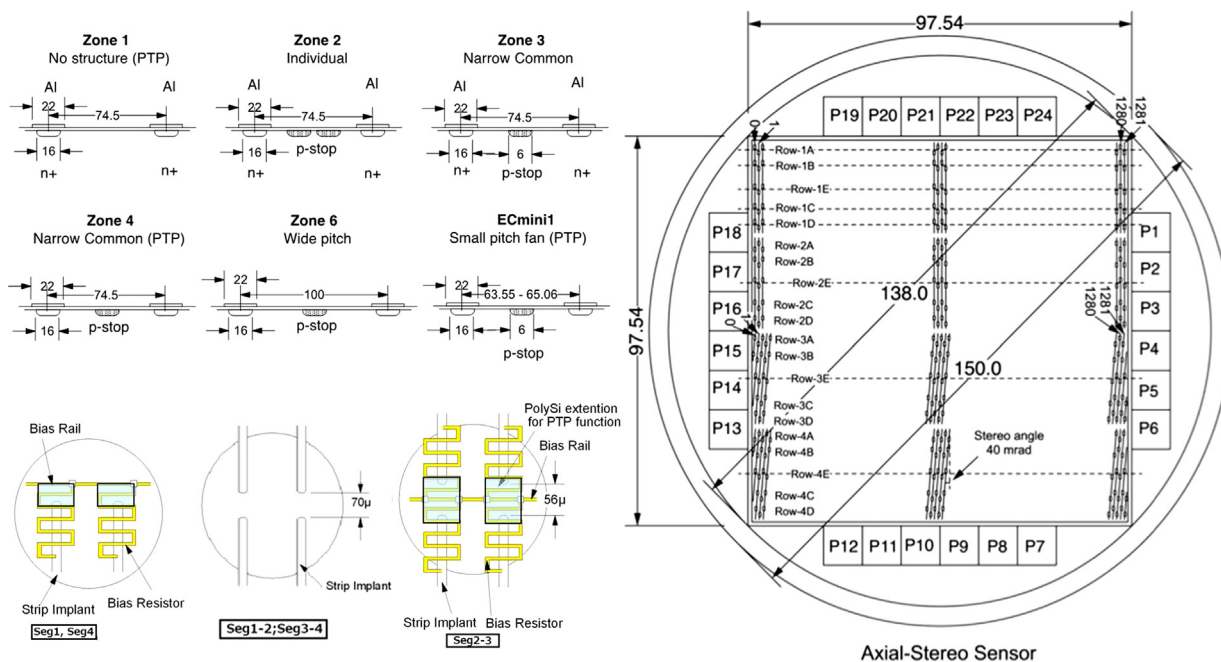
### 3. Sensor design

The strip sensors are composed of AC-coupled n-type implants placed in p-type ( $n^+$ -on-p) float zone (FZ) silicon. This type of sensor is not subject to radiation induced type inversion, thereby allowing sensor operation under partial depletion in the case where the increased full depletion voltage exceeds the maximum allowed value of the system. The radiation damage is shown to be moderate because the sensor collects faster electrons and the strip-related larger weighting fields in the Shockley-Ramo theorem are favored in view of charge collection [5]. The fully irradiated sensors provide a signal of 7.5–12.5  $ke^-$  at 500 V [6] for various irradiation sources. Since the electronics noise is found to be less than 700  $e^-$  [7,8], the signal-to-noise ratio will remain above 10.

#### 3.1. ATLAS12

A new sensor design study, named ATLAS12, is programmed in 2012 to address the above issues. The main specifications for the ATLAS12 sensor are summarized below.

- The baseline wafer is a p-type FZ of  $> 4 \text{ k}\Omega \text{ cm}$  resistivity to realize the initial full depletion of  $< 300 \text{ V}$  for a wafer thickness of  $320 \mu\text{m}$ .
- Isolation between strips is achieved by use of a common p-stop structure with doping concentration of approximately  $4 \times 10^{12} \text{ ions/cm}^2$ .
- The maximum operation voltage is set at 600 V, suitable for 500 V rating of the existing ATLAS cables.
- No micro-discharge should occur below 600 V. However, the sensors will be subjected to test voltage of up to 1 kV to investigate stable operation at higher biases.
- The interstrip capacitance to the nearest-neighbor on both sides should be 0.8 pF/cm at a 300 V bias with  $f_{\text{TEST}} = 100 \text{ kHz}$ .
- The allowed strip failure rate is less than 2%.



**Fig. 3.** ATLAS12 wafer layout for short barrel strip sensor prototypes. (Right) The sensitive area (electrodes running vertically) is segmented into four short strip regions with the strips in lower two regions tilted with respect to those in upper regions. (Left) Detailed drawings of different zones implemented in the test structures (P1–P24) and of biasing schema for each segment.

The ATLAS12, see Fig. 3 (right), is composed of short strips with the main sensor which has an area of  $97.54 \text{ mm}^2$  being segmented into four segments over the strip length. The strips are biased, see Fig. 3 (left), from one end via the use of poly-silicon resistors: the strips in Seg2 and Seg3 share a common bias rail. The strips in the lower two segments are tilted by 40 Mrad, thereby providing the possibility of stereo readout when the sensors are assembled back-to-back to match the axial and tilted strips. In addition to the main sensor, miniature sensors with an area of  $1 \text{ cm}^2$  are manufactured, and different p-stop structures and strip pitches are examined, see Fig. 3 (left). The main sensor has a structure denoted as Z4 where PTP (punch-through protection) is realized by extending the implant ends closer ( $20 \mu\text{m}$ ) to the bias rail.

Most of the above mentioned requirements have been already met in previous production runs [9]. We continue to monitor the performance of the new prototypes in the light of deeper understanding of the sensor fabrication.

Apart from the more precise values given in the specifications, which are based on the studies made on the last prototyping ATLAS07 [10], we remark on two modifications in the mask design: (1) A second scribe line that provides possibility of reducing the sensor width (slim edge) and (2) the complete coverage of the ends of the implants by poly-Si tied to the bias rails. The second modification enables the stabilization of the function of PTP of the sensor. The PTP should be designed to sink as swiftly as possible the large current and to protect the strip insulator against being damaged by induced large voltage across, while such large current generation may originate from situations such as beam splash due to possible accelerator accidents.

### 3.2. Slim edge

In our design of the sensors, we have set the canonical distance between the active area to the edge for n-bulk sensors to three times the sensor thickness to withstand the bias voltage exceeding the full depletion. We have carried out a systematic measurement of this distance for Hamamatsu p-bulk sensors with a sensor area of  $4 \text{ mm}^2$  [11]. Fig. 4 shows the plot of the field width which can withstand a 1000 V bias as a function of the fluence when the sensor is irradiated with 70-MeV protons. The field width is defined as the distance from the bias ring to the edge while excluding the implantation. The implantation electrodes are composed of a guard ring of the opposite dopant type as the bulk and a p-type edge ring. We examined two different sensor thicknesses of  $320 \mu\text{m}$  and  $150 \mu\text{m}$  for both p-bulk and n-bulk sensors.

From the figure, it can be observed that the minimum field width for a 1000 V bias decreases with the fluence and the difference in

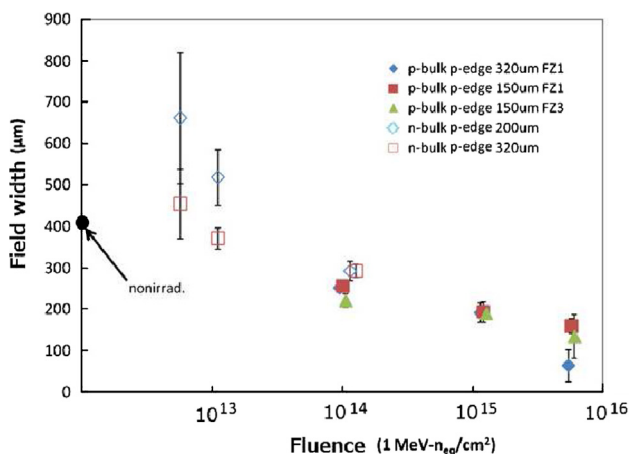


Fig. 4. Fluence dependence of field width for bias up to 1000 V.

field width between p-bulk and n-bulk diminishes as the sample accumulates the fluence. This is because the initial n-bulk has mutated into p-bulk in the dose range of the investigation. The p-bulk (and n-bulk) sensors may require a field width of  $450 \mu\text{m}$  to withstand the 1000 V bias. These results lead us to introduce a second scribe line with the width of  $450 \mu\text{m}$  alongside the strips. Reducing the width of the sensors reduces the material, although the decision to adopt the second scribe line requires further evaluation.

### 3.3. PTP structure

The optimum PTP structure has been investigated using ATLAS07 miniature sensors [12] with emphasis on the structure

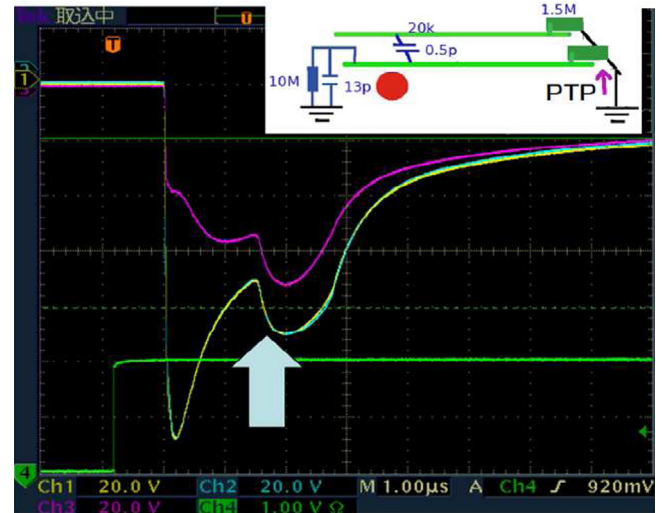


Fig. 5. Typical oscilloscope traces when intense laser is spotted near strip end opposite to PTP structure end while three nearby implant voltages are read out from end from which laser is spotted. The inset drawing illustrates the test configuration where the red circle indicates the laser spot, whereas the PTP occurs at opposite end indicated by arrow. CH1 and CH2 traces are for the two strips between which the laser was spotted, CH3 is for the strip at neighbor. The laser trigger pulse is shown in CH4. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

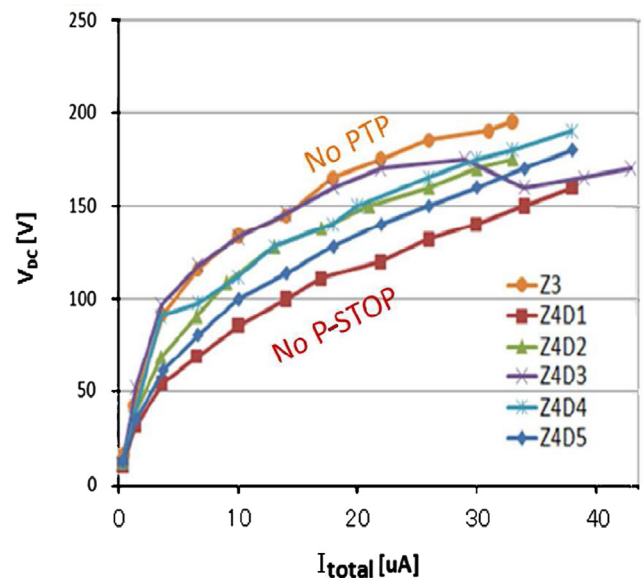


Fig. 6. Maximum voltage of implant as function of generated current. The curves are shown for different gate coverage fractions over the PTP region; D1 minimum coverage while D5 indicates full coverage. Samples: test structures with area of  $1 \text{ cm}^2$ .

around the strip end. In general, the distance between the strip end and the bias ring is a key parameter for punch through (PT) to occur. However, the p-stop adopted to utilize the p-bulk substrate acts as "PT protector", thereby complicating the investigation of the optimum PTP structure [7,8]. Further, our investigation revealed that another key parameter towards PTP optimization is the gate structure above the PT region.

The dynamic properties of PTP were studied by injecting an intense laser beam [13] (1064 nm wavelength with 10 ns duration, focused in an area  $10 \mu\text{m}^2$ ) at the strip end while measuring the implant voltage via oscilloscope probes. Typical oscilloscope traces are shown in Fig. 5 where three neighboring implant voltages were read out while one laser pulse with the generated charge corresponding to passage of  $10^6$  charged particles was injected between two of the strips. The impedance characteristics of the probes can mimic the existence of the readout ASIC, and hence, the measured voltages can be regarded as real voltages of the implant when ASICs are connected. However,

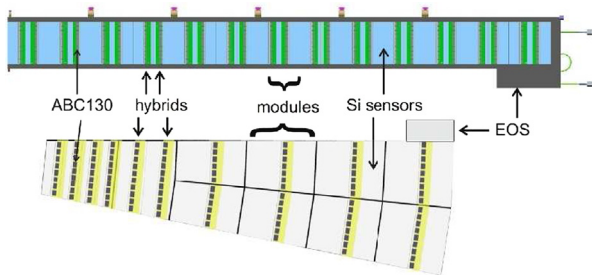


Fig. 7. Concept of end-cap module in comparison with the barrel stave.

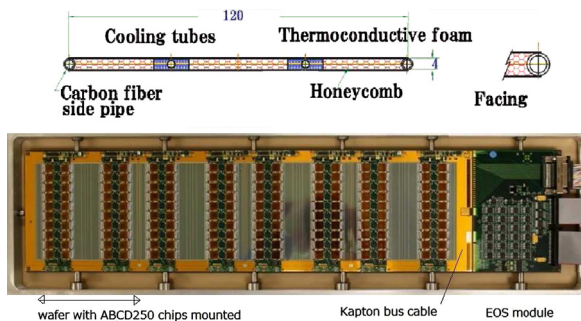


Fig. 8. Shortened version of full stave, "stavelet". The stavelet width is 12 cm.

this is applicable only when the PT is on, i.e., while the impedance between the strip to the bias ring is small enough. The implant voltages increase initially due to the charge generated by the laser absorption, and subsequently the voltages are dumped due to PTP. After an interval of about  $1.5 \mu\text{s}$  at the position indicated by the arrow in the plot, the voltages increase because the PT disappears. The increase is due to the impedance changes between the strip end and the bias ring, and the voltages shown cannot be regarded as true implant voltages.

In fact the PTP characteristics are dependent on the positions of laser injection and the signal readout. The worst case scenario, which is illustrated in the figure, occurs when both the laser spot and readout are at the other end of the PTP structure due to the existence of a finite implant resistance. The maximum voltages in this configuration are plotted in Fig. 6 as a function of the laser intensity. The abscissa represents the current generated by the laser, with a current of  $40 \mu\text{A}$  corresponding to  $10^6$  mips. The various curves are obtained for different gate coverage fractions over the PT area, with the gate being controlled via the bias ring voltage. For the uncovered PTP sample (D1) for which the distance of strip end and the bias ring is  $20 \mu\text{m}$ , the voltage becomes as high as that obtained in the absence of a PTP sample for which the strip-end-to-bias-ring distance is  $60 \mu\text{m}$ . The optimum PTP characteristics are obtained for the gate coverage corresponding to D5 where the PT region is fully covered. In the ATLAS12, the PT regions are covered by poly-silicon tied to the bias rail.

#### 4. Module design and integration

The barrel strip detector consists of 512 ladder structures (LS), as shown in Fig. 7. Each LS has 13 silicon wafers on each side providing stereo space point reconstruction, where hybrids equipped with ABC130 ASICs [14], a common interface (EOS) to the outside and a cooling system are integrated. For 256 channels per ABC130, 10 chips are lined on a hybrid, collecting signals alternately from two adjacent sensor rows. Therefore, two (one) hybrids are required for each wafer comprising short (long) strips. For the end-caps, the technologies are identical but the sensor shapes are trapezoidal with six different sensor types being used. The shortest strips are 2.3 cm long and the longest strips are 6 cm, with the strip pitch varying from 60 to  $110 \mu\text{m}$ .

The EOS has a gigabit transceiver to interface with the hybrids along with a fiber optic driver. LV and HV power supplies that

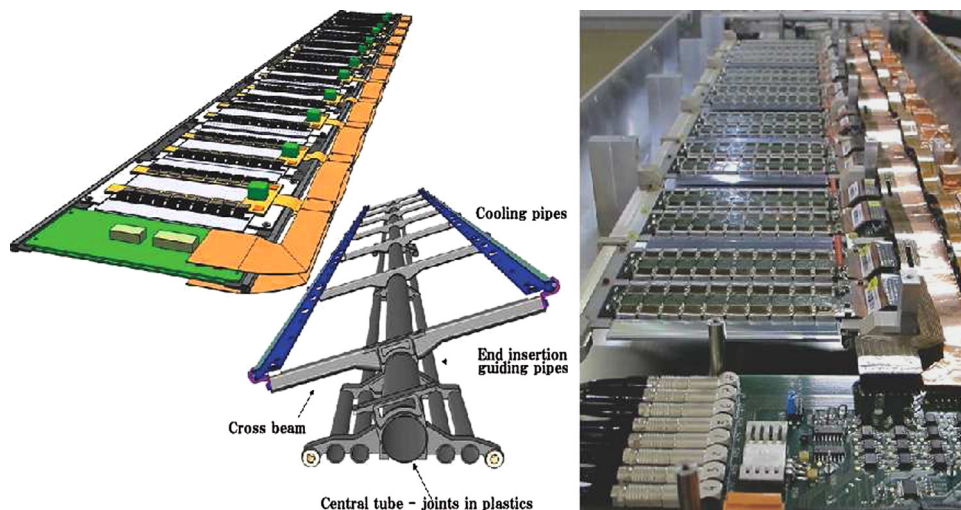


Fig. 9. Concept of super-module frame and prototype of a super-module where eight modules are mounted.

connect to the EOS are distributed to each hybrid via a power bus. The powering is based on either serial power [15] or DC–DC conversion [16].

The front-end ASIC, which is ABC130 based on 130-nm CMOS technology, is a binary readout chip providing only hit information in a manner similar to the functioning of the current SCT ABCD chip. Following a 256-bit deep L0 buffer cycled at a 40 MHz beam crossing rate, another 256-bit deep buffer stores the hits of L0 accepted events, allowing a latency as long as 512  $\mu$ s until L1 or R3 decision is made. In the baseline implementation, the R3 decision is a Region-of-Interest trigger created by other detectors to request a certain region of the strip detector to send hit information to aid the construction an L1 trigger.

Two module integration approaches have been investigated to construct LSs. The LoI baseline uses a stave approach [8] where wafers and bus cables underneath are glued onto a light structure with integrated cooling (see drawing in Fig. 8). The Kapton flex hybrids are glued directly onto the wafers with electronics-grade epoxy. The bus cables provide ASIC communication to the EOS module. The stave is supported sideways as shown in the figure, which displays a shortened version of a prototype stave constructed using ABC250 chips.

The optional approach is a super-module concept. Two wafers are glued on both sides of a baseboard, to which the hybrids are glued so as to bridge over the wafers. A total of 13 such modules are integrated into a super-module by means of a light-weight frame to which cooling pipes are attached. The communication is provided through a bus cable running alongside the module, as shown in Fig. 9. The figure also shows the photograph of a prototype super-module [17,7] comprising eight modules.

Mechanical and electrical capabilities of the two designs have been successfully demonstrated with the use of prototype components. Many of the components such as sensors, front-end ASICs, and powering schemes are common to both approaches.

The construction of the prototype for end-cap integration, termed “petal”, that is based on the stave concept, is one of the major goals to be achieved in this year.

## 5. Summary

The ATLAS experiment is due to undergo an upgrade involving the replacement of the inner tracking system to ensure precise particle tracking in the high-radiation environment expected to be generated in the HL-LHC. The outer volume of the tracker will be

occupied by silicon strip detectors. Sensors produced via n<sup>+</sup>-on-p technology have shown excellent performance in this regard, thereby fulfilling the requested final specifications including radiation hardness. The performance of the new batch of sensors fabricated this year, the ATLAS12 sensors, continues to be monitored and documented from the viewpoint of new developments in sensor fabrication.

A module integration system has been prototyped based on the stave and super-module concepts, with the practical realization of both concepts having demonstrated the requested electrical and mechanical capabilities. Prototyping of the end-cap module integration is in progress.

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