Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs

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***Abstract*— An X-ray irradiation degradation mechanism has been investigated for fully depleted-silicon-on-insulator (FD-SOI) p-channel MOSFETs (p-MOSFETs). It is found that the drain current degradation by the X-ray irradiation has gate length dependence showing 20% degradation for $L = 0.2\ \mu$m, while 8% for $L = 10\ \mu$m after the 1.4 kGy(Si) X-ray irradiation. Using Terada's method, it was found that the degradation is not due to mobility degradation but due to radiation-induced gate length modulation (RIGLEM) and the associated increase of source and drain parasitic resistance. The major cause of degradation induced by the RIGLEM is explained by an analytical model, assuming a positive charge generation in sidewall spacers. It can be suggested that the X-ray irradiation degradation of FD-SOI p-MOSFET can be improved by optimizing the lightly doped drain region.**

***Index Terms*— Fully depleted-silicon-on-insulator (FD-SOI), gate length modulation, MOSFET, sidewall spacer, X-ray radiation hardness.**

I. Introduction

FOR the requirements of advanced and future large scale integrated circuit technologies, a fully depleted-silicon-on-insulator (FD-SOI) technology is the most promising candidate because of its scalability, reduction of power consumption while keeping high-speed operation, wide temperature range operation, and radiation hardness for single-event upset (SEU). In addition, the SOI structure is one of 3-D devices when active devices are composed in the SOI handle wafer. These advantages are suitable for an X-ray imaging sensor of medical or science used to achieve high resolution with smaller pixel size. Then, the X-ray sensors have been reported, utilizing the SOI structures [1]–[5]. However, even though the SOI device has higher immunity to the SEU, it is weak in the total ionizing dose effect [6]. This is due to the existence of relatively thick oxide underneath the MOSFET so-called buried oxide (BOX) in the SOI structure. It is well known that positive charges are generated in oxide by the X-ray irradiation [7]. For the n-channel MOSFET (n-MOSFET) case, the generated positive charge in the BOX alters the back potential. Consequently, the threshold voltages decrease, and the drain-to-source leakage enhancement is observed due to the back channel formation in the n-MOSFET by X-ray irradiation [8]. Because the n-MOSFET degradation is due to the positive charge generation in the BOX, reducing the BOX thickness is one of solutions to improve the radiation hardness [9]. Furthermore, a double SOI structure has been proposed to improve the radiation hardness where the middle SOI layer is used as a compensation electrode for the generated positive charges in the BOX [10], [11]. On the other hand, there are a few studies about the FD-SOI p-MOSFET degradation by the X-ray irradiation, and we found that it shows extremely high degradation. In this paper, the degradation of the FD-SOI p-MOSFET has been investigated. We also present an analytical model for the degradation due to an effective channel length modulation by the X-ray irradiation [12]–[14], utilizing the model of positive charge generation in the sidewall spacers.

II. Experimental Procedure

A test-element group of MOSFETs [15] were fabricated using a 0.2 μm node FD-SOI CMOS process technology for a radiation sensor application prepared by LAPIS Semiconductor Co., Ltd. [16]. Thicknesses of the BOX, the SOI layer, and the gate oxide are 200, 40, and 4.4 nm, respectively. A channel stop implantation into the sidewall of the SOI active edge was employed to prevent the isolation edge effect by the X-ray irradiation [17]. A conventional lightly doped drain (LDD) structure was applied to reduce the hot-carrier and short-channel effects. Co-salicided diffusion and gate poly were also employed to reduce parasitic resistance and make the

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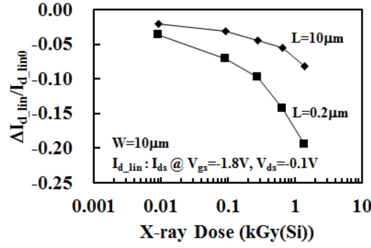

Fig. 1. p-MOSFET's drain current degradation at the linear region as a function of X-ray irradiation dose. For shorter gate length as 0.2 μm, the degradation is around two times faster than that for longer gate length as 10 μm.

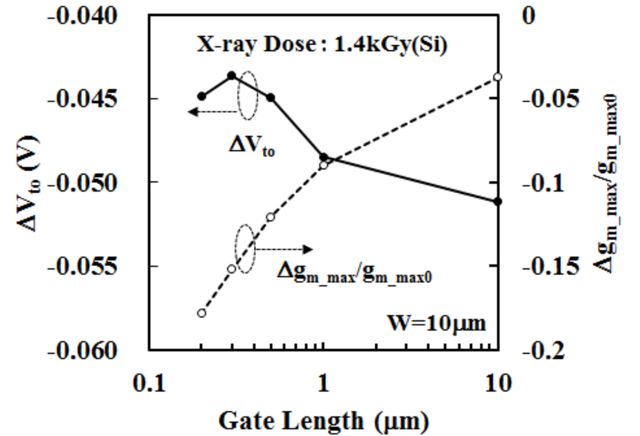

Fig. 2. Threshold voltage and transconductance changes after the 1.4 kGy(Si) X-ray irradiation as a function of the gate length. There is only 5 mV difference in ΔV_{to} among p-MOSFETs with shorter and longer gate length. This means that the generated positive charges in the gate oxide have small gate length dependence. On the other hand, about 15% difference is observed in the g_m degradation.

contact formation process reliable [18]. The designed gate lengths are changed from 0.2 to 10 μm with the constant gate width of 10 μm. To evaluate the MOSFET characteristics before and after the X-ray irradiation, I_d–V_g curves with $V_{\text{ds}} = -0.1$ V were measured for p-MOSFETs. In all of I_d–V_g measurements, the body of MOSFETs was floating, and the substrate was connected to the ground. To estimate the generated charge in the BOX, the I–V characteristics against back gate were measured with the front gate grounded before and after the X-ray irradiation for n-MOSFETs at $V_{\text{ds}} = 0.1$ V. X-ray irradiation was carried out at a constant dose rate of 0.018 Gy(Si)/s using a wafer-level X-ray irradiation system [15]. An X-ray generator with a rotary cathode target of molybdenum (RIGAKU: Ultra18X) was used as the source at an acceleration voltage of 40 kV. An aluminum filter with a thickness of 0.5 mm was inserted to suppress X-rays below 10 keV. During the irradiation, all the pads for MOSFETs were connected to the ground.

III. Results and Discussion

A. Drain Current Degradation by X-Ray Irradiation

The drain current degradation in the linear region is confirmed for p-MOSFETs of 0.2 and 10 μm in gate length, as shown in Fig. 1. The drain currents decrease with the X-ray irradiation dose. Note that similar degradation was observed for gamma-ray irradiation. Since X-ray was irradiated uniformly, the generated charge by X-ray must be uniformly distributed in the channel, because all terminals were grounded during the irradiation. Therefore, the drain current degradation rate should exhibit small gate length dependence. However, the drain current degradation of 0.2 μm MOSFETs is 20% after the 1.4 kGy(Si) irradiation, whereas only 8% degradation for 10 μm MOSFETs. The gate length dependence of threshold voltage shift, ΔV_{to}, and transconductance degradation rate, $\Delta g_{\text{m_max}}/g_{\text{m_max}\,0}$, are also investigated after the 1.4 kGy(Si) X-ray irradiation, as shown in Fig. 2. Even though the gate length was varied from 0.2 to 10 μm, the threshold voltage shifts are distributed from -0.045 to -0.050 V and the difference is only 5 mV. This indicates that the generated charge in the gate oxide should be almost uniformly distributed in the channel of these gate length varied MOSFETs. On the other hand, the transconductance degradation rate depends strongly on the gate length. In general, the transconductance degradation is caused by the generation of interface states between the gate oxide and the silicon or positive charge generation in the gate oxide. In both cases, the threshold voltage is also shifted. Then, the results of Fig. 2 do not clearly show the actual cause of the degradation.

B. Degradation Mechanism Estimation by Terada's Method

To clarify the degradation mechanism, carrier mobility, gate length modulation, and source and drain parasitic resistance are extracted using Terada's method [19]. Assuming that the source and the drain parasitic resistances, R_s and R_d, are connected to the MOSFET in series, the measured total resistance, $R_m = V_{\text{ds}}/I_{\text{ds}}$, is given by

$$R_m = \rho_{\text{ch}} \frac{L_{\text{eff}}}{W_{\text{eff}}} + (R_s + R_d) \quad (1)$$

where ρ_{ch} is the channel sheet resistance and L_{eff} and W_{eff} are the effective gate length and the width, respectively. It is noted that the effective gate length is not the distance between metallurgical junctions of the source and the drain, but the electric effective gate length in which region the surface potential can be modulated by the gate potential. Using the designed gate length, L_{drawn}, the effective gate length is

$$L_{\text{eff}} = L_{\text{drawn}} + \delta L \quad (2)$$

where δL is the bias from the designed length to the effective length. Substituting (2) into (1) and using $R_{\text{ext}} = R_s + R_d$ yields

$$R_m = \frac{\rho_{\text{ch}}}{W_{\text{eff}}} L_{\text{drawn}} + \left(\delta L \frac{\rho_{\text{ch}}}{W_{\text{eff}}} + R_{\text{ext}}\right). \quad (3)$$

From the relation between R_m and L_{drawn}, $\rho_{\text{ch}}/W_{\text{eff}}$ and $\delta L \rho_{\text{ch}}/W_{\text{eff}} + R_{\text{ext}}$ for different V_{gs}–V_{to} can be calculated. Linear relations between $\rho_{\text{ch}}/W_{\text{eff}}$ and $\delta L \rho_{\text{ch}}/W_{\text{eff}} + R_{\text{ext}}$ are confirmed for the samples before and after X-ray irradiation, as shown in Fig. 3. From these relations, δL and R_{ext}

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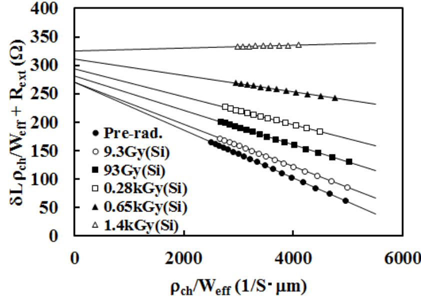


Fig. 3. Plot between $\delta L \rho_{ch}/W_{eff} + R_{ext}$ and ρ_{ch}/W_{eff} calculated from (3) as a parameter of X-ray irradiation dose. Good linear relations for each dose are confirmed for all doses. The Y-intercept and gradient of the lines are R_{ext} and δL, respectively.

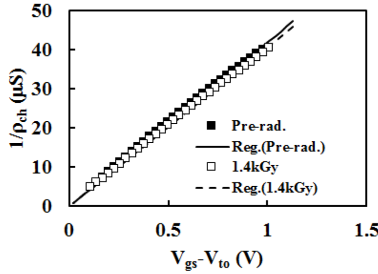
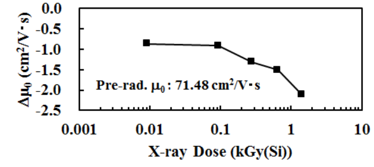


Fig. 4. Relation between $1/\rho_{ch}$ and V_{gs}–V_{to} to extract the mobility of channel holes for the preradiation and 1.4 kGy(Si) irradiated samples. Almost no difference in the mobility is observed by X-ray irradiation.

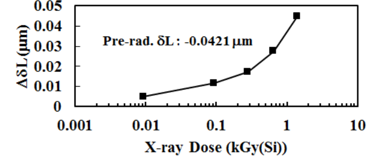
are extracted. On the other hand, the channel sheet resistance can be described as

$$\rho_{ch} = \frac{1}{\mu C_{ox}(V_{gs} - V_{to})} \quad (4)$$

where μ is the carrier mobility, C_{ox} is the gate capacitance, and V_{to} is the threshold voltage. Reciprocals of ρ_{ch} as a function of V_{gs}–V_{to} are shown in Fig. 4 for preradiation and 1.4 kGy(Si) irradiated samples. Then, using this method, μ, δL, and R_{ext} as a function of the X-ray irradiation dose are extracted and shown in Fig. 5. As shown in the figure, the mobility degradation by the X-ray irradiation is small. On the other hand, the effective gate length and the parasitic source and drain resistance increase with the X-ray dose. This is quite interesting that the transconductance degradation shown in Fig. 2 is not induced by the mobility degradation, but by the effective gate length modulation, leading to the transconductance degradation. Because the major factors of the degradation by the X-ray irradiation are related to the gate length modulation and the parasitic source and drain resistance increase, the degradation phenomenon occurs at the edges of the gate. Based on the knowledge that the X-ray irradiation damages are positive charge generation in oxide and surface state generation at the Si–SiO_2 interface [7], the following two degradation mechanisms are suspected. One is that the positive charge generated in the BOX by the X-ray irradiation [20] modulates the LDD region, because the concentration of LDD is as low as 10^{18} cm^{-3} order, and the resistance of LDD layer may be easily changed by the generated positive charge in the BOX. The other is that the generated positive



(a)



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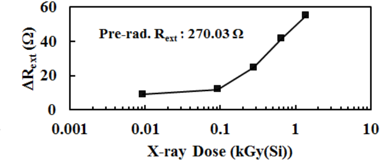

(c)

Fig. 5. Results by Terada's method calculation for (a) mobility changes, (b) gate length bias changes, and (c) parasitic resistance changes of p-MOSFETs as a function of X-ray irradiation dose. The relative changes in mobility are small, whereas those in the gate length modulation and the parasitic resistance are large.

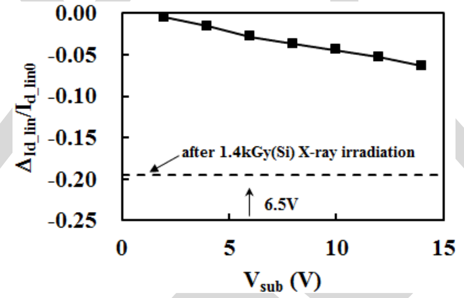

Fig. 6. Degradation of drain current in the linear region by substrate bias for a fresh p-MOSFET. The 6.5 V of V_{sub} is equivalent to the positive charge in the BOX after the 1.4 kGy(Si) irradiation. Dashed line: drain current degradation by the 1.4 kGy(Si) X-ray irradiation.

charge in the sidewall spacers [21] may increase the absolute threshold voltage at gate edge and cause the drain current degradation.

C. Effect of Generated Positive Charge in the Box

The effect of the generated positive charge in the BOX can be easily evaluated from the substrate bias (V_{sub}) dependence of MOSFETs, because the positive charge generation in the BOX is equivalent to supplying the positive bias to the substrate. Fig. 6 shows the I_{d_lin} degradation by V_{sub}. In this figure, the I_{d_lin} degradation after the 1.4 kGy(Si) X-ray irradiation is shown in Fig. 6 (dashed line). The indicated V_{sub} of 6.5 V is equivalent to the positive charge in the BOX after the 1.4 kGy(Si) X-ray irradiation, which was obtained from the backside gate I–V for n-MOSFETs. The I_{d_lin} degradation by the substrate bias accounts for only 6.5% for $V_{sub} = 14$ V, whereas 20% for the 1.4 kGy(Si) X-ray irradiation samples. The μ, δL, and R_{ext}

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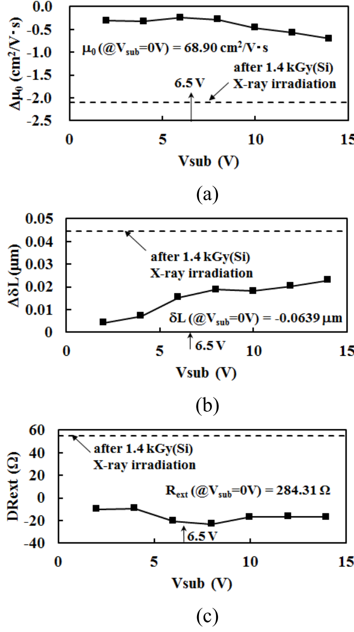

Fig. 7. Results by Terada's method calculation for (a) mobility changes, (b) gate length bias changes, and (c) parasitic resistance changes of p-MOSFETs as a function of substrate bias. The 6.5 V of V_{sub} is equivalent to the positive charge in the BOX after the 1.4 kGy(Si) irradiation. Dashed lines: degradation by the 1.4 kGy(Si) X-ray irradiation similar to Fig. 6. The mobility, gate length bias, and parasitic resistance changes even at $V_{\text{sub}} = 14$ V are within those induced by the 1.4 kGy(Si) X-ray irradiation.

changes by V_{sub} are also extracted using Terada's method and shown in Fig. 7. There is no significant δL and R_{ext} degradations by V_{sub}. Therefore, it is concluded that the p-MOSFET degradation by the X-ray irradiation is not solely due to the generated positive charge in the BOX.

D. Effect of Generated Positive Charge in Spacers

Considering the charge generation by X-ray irradiation, the MOSFET structure can be divided into three regions, as shown in Fig. 8. The drain current of MOSFET through Region II is controlled by the gate potential and affected by the charge in gate oxide after the X-ray irradiation. On the other hand, the drain current of MOSFETs in Region I and Region III, which are in the edge portions of MOSFET, is affected additionally by the positive charge in the sidewall spacers. When the effective gate length of Region II MOSFET is L_{eff2} and that of Region I or Region III is L_{eff1}, then the total effective gate length, L_{eff}, is

$$L_{\text{eff}} = L_{\text{eff2}} + 2L_{\text{eff1}}. \tag{5}$$

The drain currents of each MOSFET are described as

$$I_{\text{ds}} = \frac{W_{\text{eff}}}{L_{\text{eff1}}}\mu C_{\text{ox}}(V_{\text{gs}} - V_{\text{to1}})V_{\text{ds1}} \tag{6}$$

$$I_{\text{ds}} = \frac{W_{\text{eff}}}{L_{\text{eff2}}}\mu C_{\text{ox}}(V_{\text{gs}} - V_{\text{ds1}} - V_{\text{to}})V_{\text{ds2}} \tag{7}$$

$$I_{\text{ds}} = \frac{W_{\text{eff}}}{L_{\text{eff1}}}\mu C_{\text{ox}}[V_{\text{gs}} - (V_{\text{ds1}} + V_{\text{ds2}}) - V_{\text{to1}}]V_{\text{ds3}} \tag{8}$$

and

$$V_{\text{ds}} = V_{\text{ds1}} + V_{\text{ds2}} + V_{\text{ds3}}. \tag{9}$$

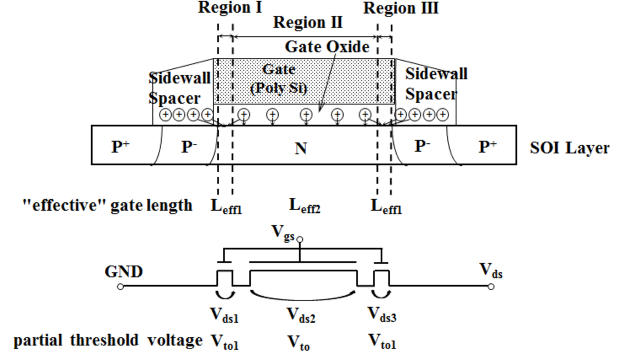

Fig. 8. Schematic cross section and an equivalent circuit to explain parasitic p-MOSFETs at both the source and the drain sides. Effective gate length, drain voltage, and threshold voltage of the center MOSFET are L_{eff2}, V_{ds2}, and V_{to}, respectively. Those of the parasitic source or the drain side MOSFET are L_{eff1}, V_{ds1}, and V_{to1} or L_{eff1}, V_{ds3}, and V_{to1}, respectively.

To simplify the calculation, $R_{\text{ext}} = 0$ is assumed. Substituting (6)–(8) into (9) yields

$$\begin{aligned} R_m &= \frac{V_{\text{ds}}}{I_{\text{ds}}} \\ &= \frac{1}{W_{\text{eff}}\mu C_{\text{ox}}}\left[\frac{L_{\text{eff1}}}{V_{\text{gs}} - V_{\text{to1}}} + \frac{L_{\text{eff2}}}{V_{\text{gs}} - V_{\text{ds1}} - V_{\text{to}}}\right. \\ &\qquad \left. + \frac{L_{\text{eff1}}}{V_{\text{gs}} - (V_{\text{ds1}} + V_{\text{ds2}}) - V_{\text{to1}}}\right]. \end{aligned} \tag{10}$$

It is assumed that $V_{\text{gs}} - V_{\text{to}} \gg V_{\text{ds1}}$ and $V_{\text{gs}} - V_{\text{to1}} \gg V_{\text{ds1}} + V_{\text{ds2}}$, then (10) becomes

$$\begin{aligned} R_m &= \frac{1}{W_{\text{eff}}\mu C_{\text{ox}}}\left(\frac{2L_{\text{eff1}}}{V_{\text{gs}} - V_{\text{to1}}} + \frac{L_{\text{eff2}}}{V_{\text{gs}} - V_{\text{to}}}\right) \\ &= \frac{\rho_{\text{ch}}}{W_{\text{eff}}}\left(L_{\text{eff2}} + 2L_{\text{eff1}}\frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - V_{\text{to1}}}\right). \end{aligned} \tag{11}$$

Comparing (11) with (1) yields

$$L_{\text{eff}} = L_{\text{eff2}} + 2L_{\text{eff1}}\frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - V_{\text{to1}}}. \tag{12}$$

If there are positive charges in the sidewall spacers, V_{to1} should shift to the negative. For p-MOSFET case, V_{gs} is the negative. Then, V_{gs}–V_{to1} decreases and L_{eff} increases. The L_{eff} modulation factor is a fractional expression in the second term in the right-hand side of (12) and can be rewritten as

$$\frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - V_{\text{to1}}} = \frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - (V_{\text{to}} + \Delta V_{\text{to1}})} = \frac{1}{1 - \frac{\Delta V_{\text{to1}}}{V_{\text{gs}} - V_{\text{to}}}} \tag{13}$$

where $\Delta V_{\text{to1}} = V_{\text{to1}}$–$V_{\text{to}}$. With the consideration of V_{to} value ($|V_{\text{to}}| \sim 0.8$ V) and measurement conditions ($|V_{\text{gs}}| \sim 1.8$ V), V_{gs}–V_{to} can be approximated to be 1, and then (13) becomes

$$\frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - V_{\text{to1}}} \cong \frac{1}{1 - \Delta V_{\text{to1}}}. \tag{14}$$

L_{eff} after the X-ray irradiation with the dose of x is given by

$$L_{\text{eff}}(x) = L_{\text{eff2}} + 2L_{\text{eff1}}\frac{1}{1 - \Delta V_{\text{to1}}} \tag{15}$$

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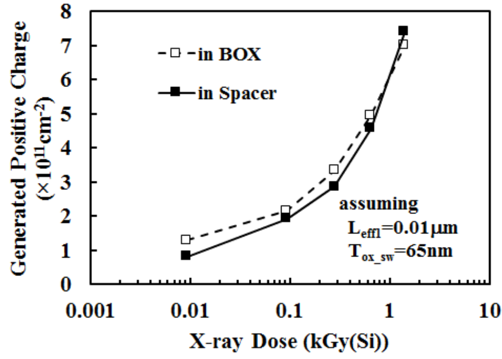

Fig. 9. Trapped hole densities as a function of X-ray irradiation dose in the BOX and the sidewall spacer. To calculate the number of the trapped holes in the sidewall spacer, it is assumed that L_{eff1} is 0.01 μm and the thickness of the sidewall spacer is 65 nm.

and that for the preradiation is also given by (5). Then, the variation of δL by the X-ray radiation, $\Delta\delta L$, is expressed by

$$\begin{aligned}\Delta\delta L &= (L_{\text{eff}}(x) - L_{\text{drawn}}) - (L_{\text{eff}}(0) - L_{\text{drawn}}) \\ &= L_{\text{eff}}(x) - L_{\text{eff}}(0) = 2L_{\text{eff1}}\frac{\Delta V_{\text{to1}}}{1-\Delta V_{\text{to1}}}. \end{aligned} \tag{16}$$

When $\Delta V_{\text{to1}} \ll 1$, (17) becomes

$$\Delta\delta L = 2L_{\text{eff1}}\Delta V_{\text{to1}}. \tag{17}$$

If the effective oxide thickness of the sidewall spacer is $T_{\text{ox_sw}}$, the effective generated charge in the sidewall spacer, $\Delta N_{\text{ot_sw}}$, is

$$\Delta N_{\text{ot_sw}} = \frac{\varepsilon_{\text{SiO2}}}{2qL_{\text{eff1}}T_{\text{ox_sw}}}\Delta\delta L \tag{18}$$

where q is the elementary electron charge and $\varepsilon_{\text{sio2}}$ is the permittivity of oxide. Assuming $L_{\text{eff1}} = 0.01$ μm and $T_{\text{ox_sw}} = 65$ nm, $\Delta N_{\text{ot_sw}}$ is calculated from measured $\Delta\delta L$, as shown in Fig. 9, as a function of the X-ray irradiation dose. In this figure, the generated positive charges in the BOX calculated from the back gate Vt shift of n-MOSFETs are also shown. It is confirmed that both trends for the estimated generated charges in the sidewall spacer and the BOX are almost the same. Based on these results, it is concluded that the gate length modulation by the X-ray irradiation in p-MOSFETs, which is the major cause of degradation, is the local Vt shift at gate edges due to the generated positive charge in the sidewall spacers. This effect must be enhanced when the ON-state bias is used during the X-ray irradiation instead of the OFF-state bias of this experiment. In addition, we have confirmed that the higher LDD dosage suppresses the gate length modulation effect and improves the drain current degradation by the X-ray irradiation. The detailed results will be presented elsewhere in the future.

IV. Conclusion

The X-ray irradiation-induced drain current degradation of FD-SOI p-MOSFET has been studied. The drain current degradation of 20% was observed in the linear region after the 1.4 kGy(Si) X-ray irradiation for 0.2 μm transistors in the gate length, whereas 8% for 10 μm transistors. No obvious gate length dependence of Vt shift but clear dependence of the gm degradation by the X-ray irradiation was confirmed. To investigate the mechanisms of the degradation, the analysis based on Terada's method was examined. It is found that the degradation is due to the effective gate length modulation and the external parasitic source and drain resistance but not due to the mobility reduction. The effective gate length modulation is caused by the generated positive charge in the sidewall spacers, as concluded from the model of local Vt shift induced at the gate edges. Based on this model, the radiation hardness for FD-SOI LDD p-MOSFET should be improved by higher LDD implant dosage such that the gate overlap region of LDD is extended and consequently the gate edge transistors may also be controlled solely by the gate potential, not by charges in the sidewall spacers.

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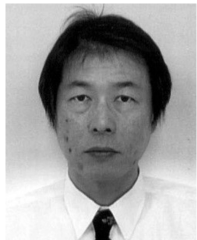

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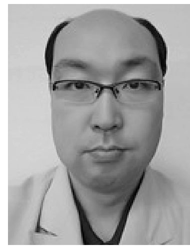

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Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs

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***Abstract*— An X-ray irradiation degradation mechanism has been investigated for fully depleted-silicon-on-insulator (FD-SOI) p-channel MOSFETs (p-MOSFETs). It is found that the drain current degradation by the X-ray irradiation has gate length dependence showing 20% degradation for $L = 0.2$ μm, while 8% for $L = 10$ μm after the 1.4 kGy(Si) X-ray irradiation. Using Terada's method, it was found that the degradation is not due to mobility degradation but due to radiation-induced gate length modulation (RIGLEM) and the associated increase of source and drain parasitic resistance. The major cause of degradation induced by the RIGLEM is explained by an analytical model, assuming a positive charge generation in sidewall spacers. It can be suggested that the X-ray irradiation degradation of FD-SOI p-MOSFET can be improved by optimizing the lightly doped drain region.**

***Index Terms*— Fully depleted-silicon-on-insulator (FD-SOI), gate length modulation, MOSFET, sidewall spacer, X-ray radiation hardness.**

I. Introduction

FOR the requirements of advanced and future large scale integrated circuit technologies, a fully depleted-silicon-on-insulator (FD-SOI) technology is the most promising candidate because of its scalability, reduction of power consumption while keeping high-speed operation, wide temperature range operation, and radiation hardness for single-event upset (SEU). In addition, the SOI structure is one of 3-D devices when active devices are composed in the SOI handle wafer. These advantages are suitable for an X-ray imaging sensor of medical or science used to achieve high resolution with smaller pixel size. Then, the X-ray sensors have been reported, utilizing the SOI structures [1]–[5]. However, even though the SOI device has higher immunity to the SEU, it is weak in the total ionizing dose effect [6]. This is due to the existence of relatively thick oxide underneath the MOSFET so-called buried oxide (BOX) in the SOI structure. It is well known that positive charges are generated in oxide by the X-ray irradiation [7]. For the n-channel MOSFET (n-MOSFET) case, the generated positive charge in the BOX alters the back potential. Consequently, the threshold voltages decrease, and the drain-to-source leakage enhancement is observed due to the back channel formation in the n-MOSFET by X-ray irradiation [8]. Because the n-MOSFET degradation is due to the positive charge generation in the BOX, reducing the BOX thickness is one of solutions to improve the radiation hardness [9]. Furthermore, a double SOI structure has been proposed to improve the radiation hardness where the middle SOI layer is used as a compensation electrode for the generated positive charges in the BOX [10], [11]. On the other hand, there are a few studies about the FD-SOI p-MOSFET degradation by the X-ray irradiation, and we found that it shows extremely high degradation. In this paper, the degradation of the FD-SOI p-MOSFET has been investigated. We also present an analytical model for the degradation due to an effective channel length modulation by the X-ray irradiation [12]–[14], utilizing the model of positive charge generation in the sidewall spacers.

II. Experimental Procedure

A test-element group of MOSFETs [15] were fabricated using a 0.2 μm node FD-SOI CMOS process technology for a radiation sensor application prepared by LAPIS Semiconductor Co., Ltd. [16]. Thicknesses of the BOX, the SOI layer, and the gate oxide are 200, 40, and 4.4 nm, respectively. A channel stop implantation into the sidewall of the SOI active edge was employed to prevent the isolation edge effect by the X-ray irradiation [17]. A conventional lightly doped drain (LDD) structure was applied to reduce the hot-carrier and short-channel effects. Co-salicided diffusion and gate poly were also employed to reduce parasitic resistance and make the

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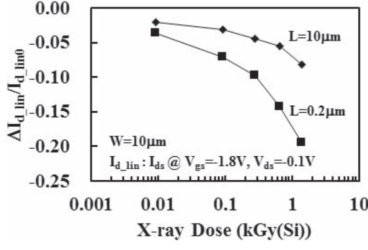

Fig. 1. p-MOSFET's drain current degradation at the linear region as a function of X-ray irradiation dose. For shorter gate length as 0.2 μm, the degradation is around two times faster than that for longer gate length as 10 μm.

contact formation process reliable [18]. The designed gate lengths are changed from 0.2 to 10 μm with the constant gate width of 10 μm. To evaluate the MOSFET characteristics before and after the X-ray irradiation, I_d–V_g curves with $V_{\text{ds}} = -0.1$ V were measured for p-MOSFETs. In all of I_d–V_g measurements, the body of MOSFETs was floating, and the substrate was connected to the ground. To estimate the generated charge in the BOX, the I–V characteristics against back gate were measured with the front gate grounded before and after the X-ray irradiation for n-MOSFETs at $V_{\text{ds}} = 0.1$ V. X-ray irradiation was carried out at a constant dose rate of 0.018 Gy(Si)/s using a wafer-level X-ray irradiation system [15]. An X-ray generator with a rotary cathode target of molybdenum (RIGAKU: Ultra18X) was used as the source at an acceleration voltage of 40 kV. An aluminum filter with a thickness of 0.5 mm was inserted to suppress X-rays below 10 keV. During the irradiation, all the pads for MOSFETs were connected to the ground.

III. Results and Discussion

A. Drain Current Degradation by X-Ray Irradiation

The drain current degradation in the linear region is confirmed for p-MOSFETs of 0.2 and 10 μm in gate length, as shown in Fig. 1. The drain currents decrease with the X-ray irradiation dose. Note that similar degradation was observed for gamma-ray irradiation. Since X-ray was irradiated uniformly, the generated charge by X-ray must be uniformly distributed in the channel, because all terminals were grounded during the irradiation. Therefore, the drain current degradation rate should exhibit small gate length dependence. However, the drain current degradation of 0.2 μm MOSFETs is 20% after the 1.4 kGy(Si) irradiation, whereas only 8% degradation for 10 μm MOSFETs. The gate length dependence of threshold voltage shift, ΔV_{to}, and transconductance degradation rate, $\Delta g_{\text{m_max}}/g_{\text{m_max}\,0}$, are also investigated after the 1.4 kGy(Si) X-ray irradiation, as shown in Fig. 2. Even though the gate length was varied from 0.2 to 10 μm, the threshold voltage shifts are distributed from -0.045 to -0.050 V and the difference is only 5 mV. This indicates that the generated charge in the gate oxide should be almost uniformly distributed in the channel of these gate length varied MOSFETs. On the other hand, the transconductance degradation rate depends strongly on the gate length. In general, the transconductance degradation is caused

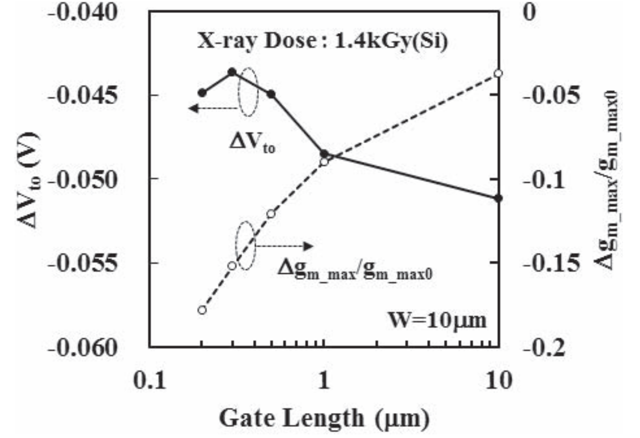

Fig. 2. Threshold voltage and transconductance changes after the 1.4 kGy(Si) X-ray irradiation as a function of the gate length. There is only 5 mV difference in ΔV_{to} among p-MOSFETs with shorter and longer gate length. This means that the generated positive charges in the gate oxide have small gate length dependence. On the other hand, about 15% difference is observed in the g_m degradation.

by the generation of interface states between the gate oxide and the silicon or positive charge generation in the gate oxide. In both cases, the threshold voltage is also shifted. Then, the results of Fig. 2 do not clearly show the actual cause of the degradation.

B. Degradation Mechanism Estimation by Terada's Method

To clarify the degradation mechanism, carrier mobility, gate length modulation, and source and drain parasitic resistance are extracted using Terada's method [19]. Assuming that the source and the drain parasitic resistances, R_s and R_d, are connected to the MOSFET in series, the measured total resistance, $R_m = V_{\text{ds}}/I_{\text{ds}}$, is given by

$$R_m = \rho_{\text{ch}} \frac{L_{\text{eff}}}{W_{\text{eff}}} + (R_s + R_d) \tag{1}$$

where ρ_{ch} is the channel sheet resistance and L_{eff} and W_{eff} are the effective gate length and the width, respectively. It is noted that the effective gate length is not the distance between metallurgical junctions of the source and the drain, but the electric effective gate length in which region the surface potential can be modulated by the gate potential. Using the designed gate length, L_{drawn}, the effective gate length is

$$L_{\text{eff}} = L_{\text{drawn}} + \delta L \tag{2}$$

where δL is the bias from the designed length to the effective length. Substituting (2) into (1) and using $R_{\text{ext}} = R_s + R_d$ yields

$$R_m = \frac{\rho_{\text{ch}}}{W_{\text{eff}}} L_{\text{drawn}} + \left(\delta L \frac{\rho_{\text{ch}}}{W_{\text{eff}}} + R_{\text{ext}} \right). \tag{3}$$

From the relation between R_m and L_{drawn}, $\rho_{\text{ch}}/W_{\text{eff}}$ and $\delta L \rho_{\text{ch}}/W_{\text{eff}} + R_{\text{ext}}$ for different V_{gs}–V_{to} can be calculated. Linear relations between $\rho_{\text{ch}}/W_{\text{eff}}$ and $\delta L \rho_{\text{ch}}/W_{\text{eff}} + R_{\text{ext}}$ are confirmed for the samples before and after X-ray irradiation, as shown in Fig. 3. From these relations, δL and R_{ext}

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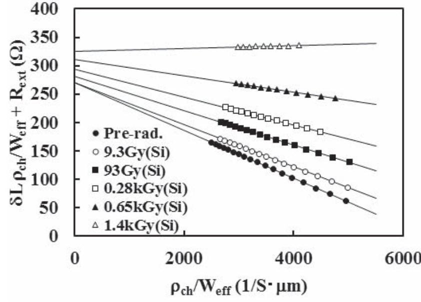


Fig. 3. Plot between $\delta L\rho_{\mathrm{ch}}/W_{\mathrm{eff}} + R_{\mathrm{ext}}$ and $\rho_{\mathrm{ch}}/W_{\mathrm{eff}}$ calculated from (3) as a parameter of X-ray irradiation dose. Good linear relations for each dose are confirmed for all doses. The Y-intercept and gradient of the lines are R_{ext} and δL, respectively.

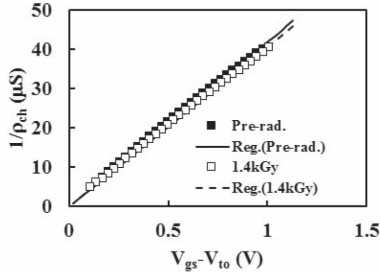
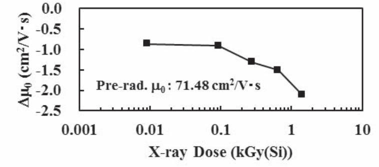


Fig. 4. Relation between $1/\rho_{\mathrm{ch}}$ and V_{gs}–V_{to} to extract the mobility of channel holes for the preradiation and 1.4 kGy(Si) irradiated samples. Almost no difference in the mobility is observed by X-ray irradiation.

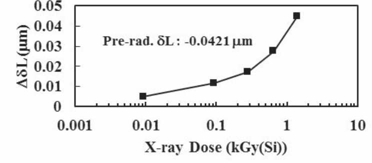
are extracted. On the other hand, the channel sheet resistance can be described as

$$\rho_{\mathrm{ch}} = \frac{1}{\mu C_{\mathrm{ox}}(V_{\mathrm{gs}} - V_{\mathrm{to}})} \tag{4}$$

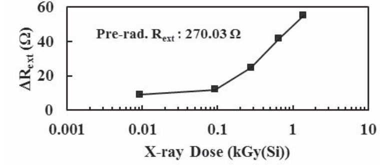
where μ is the carrier mobility, C_{ox} is the gate capacitance, and V_{to} is the threshold voltage. Reciprocals of ρ_{ch} as a function of V_{gs}–V_{to} are shown in Fig. 4 for preradiation and 1.4 kGy(Si) irradiated samples. Then, using this method, μ, δL, and R_{ext} as a function of the X-ray irradiation dose are extracted and shown in Fig. 5. As shown in the figure, the mobility degradation by the X-ray irradiation is small. On the other hand, the effective gate length and the parasitic source and drain resistance increase with the X-ray dose. This is quite interesting that the transconductance degradation shown in Fig. 2 is not induced by the mobility degradation, but by the effective gate length modulation, leading to the transconductance degradation. Because the major factors of the degradation by the X-ray irradiation are related to the gate length modulation and the parasitic source and drain resistance increase, the degradation phenomenon occurs at the edges of the gate. Based on the knowledge that the X-ray irradiation damages are positive charge generation in oxide and surface state generation at the Si–SiO_2 interface [7], the following two degradation mechanisms are suspected. One is that the positive charge generated in the BOX by the X-ray irradiation [20] modulates the LDD region, because the concentration of LDD is as low as 10^{18} cm^{-3} order, and the resistance of LDD layer may be easily changed by the generated positive charge in the BOX. The other is that the generated positive



(a)



(b)



(c)

Fig. 5. Results by Terada's method calculation for (a) mobility changes, (b) gate length bias changes, and (c) parasitic resistance changes of p-MOSFETs as a function of X-ray irradiation dose. The relative changes in mobility are small, whereas those in the gate length modulation and the parasitic resistance are large.

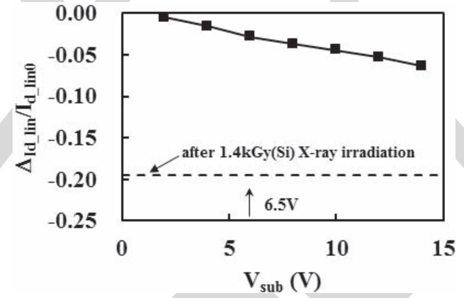


Fig. 6. Degradation of drain current in the linear region by substrate bias for a fresh p-MOSFET. The 6.5 V of V_{sub} is equivalent to the positive charge in the BOX after the 1.4 kGy(Si) irradiation. Dashed line: drain current degradation by the 1.4 kGy(Si) X-ray irradiation.

charge in the sidewall spacers [21] may increase the absolute threshold voltage at gate edge and cause the drain current degradation.

C. Effect of Generated Positive Charge in the Box

The effect of the generated positive charge in the BOX can be easily evaluated from the substrate bias (V_{sub}) dependence of MOSFETs, because the positive charge generation in the BOX is equivalent to supplying the positive bias to the substrate. Fig. 6 shows the I_{d_lin} degradation by V_{sub}. In this figure, the I_{d_lin} degradation after the 1.4 kGy(Si) X-ray irradiation is shown in Fig. 6 (dashed line). The indicated V_{sub} of 6.5 V is equivalent to the positive charge in the BOX after the 1.4 kGy(Si) X-ray irradiation, which was obtained from the backside gate I–V for n-MOSFETs. The $I_{\mathrm{d_lin}}$ degradation by the substrate bias accounts for only 6.5% for $V_{\mathrm{sub}} = 14$ V, whereas 20% for the 1.4 kGy(Si) X-ray irradiation samples. The μ, δL, and R_{ext}

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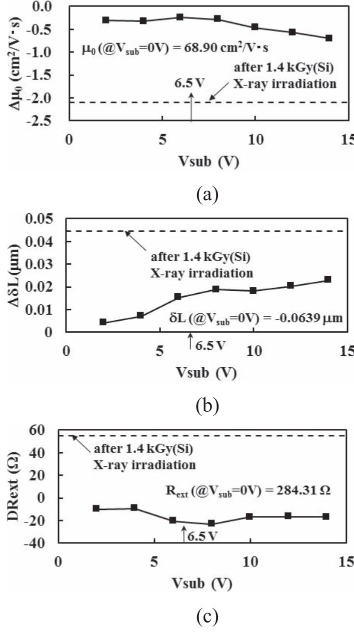

Fig. 7. Results by Terada's method calculation for (a) mobility changes, (b) gate length bias changes, and (c) parasitic resistance changes of p-MOSFETs as a function of substrate bias. The 6.5 V of V_{sub} is equivalent to the positive charge in the BOX after the 1.4 kGy(Si) irradiation. Dashed lines: degradation by the 1.4 kGy(Si) X-ray irradiation similar to Fig. 6. The mobility, gate length bias, and parasitic resistance changes even at $V_{\text{sub}} = 14$ V are within those induced by the 1.4 kGy(Si) X-ray irradiation.

changes by V_{sub} are also extracted using Terada's method and shown in Fig. 7. There is no significant δL and R_{ext} degradations by V_{sub}. Therefore, it is concluded that the p-MOSFET degradation by the X-ray irradiation is not solely due to the generated positive charge in the BOX.

D. Effect of Generated Positive Charge in Spacers

Considering the charge generation by X-ray irradiation, the MOSFET structure can be divided into three regions, as shown in Fig. 8. The drain current of MOSFET through Region II is controlled by the gate potential and affected by the charge in gate oxide after the X-ray irradiation. On the other hand, the drain current of MOSFETs in Region I and Region III, which are in the edge portions of MOSFET, is affected additionally by the positive charge in the sidewall spacers. When the effective gate length of Region II MOSFET is L_{eff2} and that of Region I or Region III is L_{eff1}, then the total effective gate length, L_{eff}, is

$$L_{\text{eff}} = L_{\text{eff2}} + 2L_{\text{eff1}}. \tag{5}$$

The drain currents of each MOSFET are described as

$$I_{\text{ds}} = \frac{W_{\text{eff}}}{L_{\text{eff1}}}\mu C_{\text{ox}}(V_{\text{gs}} - V_{\text{to1}})V_{\text{ds1}} \tag{6}$$

$$I_{\text{ds}} = \frac{W_{\text{eff}}}{L_{\text{eff2}}}\mu C_{\text{ox}}(V_{\text{gs}} - V_{\text{ds1}} - V_{\text{to}})V_{\text{ds2}} \tag{7}$$

$$I_{\text{ds}} = \frac{W_{\text{eff}}}{L_{\text{eff1}}}\mu C_{\text{ox}}[V_{\text{gs}} - (V_{\text{ds1}} + V_{\text{ds2}}) - V_{\text{to1}}]V_{\text{ds3}} \tag{8}$$

and

$$V_{\text{ds}} = V_{\text{ds1}} + V_{\text{ds2}} + V_{\text{ds3}}. \tag{9}$$

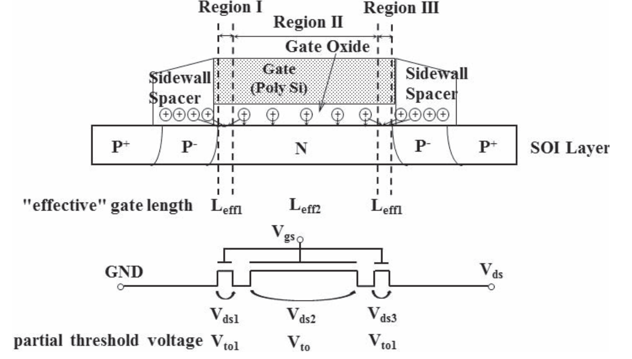

Fig. 8. Schematic cross section and an equivalent circuit to explain parasitic p-MOSFETs at both the source and the drain sides. Effective gate length, drain voltage, and threshold voltage of the center MOSFET are L_{eff2}, V_{ds2}, and V_{to}, respectively. Those of the parasitic source or the drain side MOSFET are L_{eff1}, V_{ds1}, and V_{to1} or L_{eff1}, V_{ds3}, and V_{to1}, respectively.

To simplify the calculation, $R_{\text{ext}} = 0$ is assumed. Substituting (6)–(8) into (9) yields

$$\begin{aligned} R_m &= \frac{V_{\text{ds}}}{I_{\text{ds}}} \\ &= \frac{1}{W_{\text{eff}}\mu C_{\text{ox}}}\left[\frac{L_{\text{eff1}}}{V_{\text{gs}} - V_{\text{to1}}} + \frac{L_{\text{eff2}}}{V_{\text{gs}} - V_{\text{ds1}} - V_{\text{to}}}\right. \\ &\quad \left. + \frac{L_{\text{eff1}}}{V_{\text{gs}} - (V_{\text{ds1}} + V_{\text{ds2}}) - V_{\text{to1}}}\right]. \end{aligned} \tag{10}$$

It is assumed that $V_{\text{gs}} - V_{\text{to}} \gg V_{\text{ds1}}$ and $V_{\text{gs}} - V_{\text{to1}} \gg V_{\text{ds1}} + V_{\text{ds2}}$, then (10) becomes

$$\begin{aligned} R_m &= \frac{1}{W_{\text{eff}}\mu C_{\text{ox}}}\left(\frac{2L_{\text{eff1}}}{V_{\text{gs}} - V_{\text{to1}}} + \frac{L_{\text{eff2}}}{V_{\text{gs}} - V_{\text{to}}}\right) \\ &= \frac{\rho_{\text{ch}}}{W_{\text{eff}}}\left(L_{\text{eff2}} + 2L_{\text{eff1}}\frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - V_{\text{to1}}}\right). \end{aligned} \tag{11}$$

Comparing (11) with (1) yields

$$L_{\text{eff}} = L_{\text{eff2}} + 2L_{\text{eff1}}\frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - V_{\text{to1}}}. \tag{12}$$

If there are positive charges in the sidewall spacers, V_{to1} should shift to the negative. For p-MOSFET case, V_{gs} is the negative. Then, V_{gs}–V_{to1} decreases and L_{eff} increases. The L_{eff} modulation factor is a fractional expression in the second term in the right-hand side of (12) and can be rewritten as

$$\frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - V_{\text{to1}}} = \frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - (V_{\text{to}} + \Delta V_{\text{to1}})} = \frac{1}{1 - \frac{\Delta V_{\text{to1}}}{V_{\text{gs}} - V_{\text{to}}}} \tag{13}$$

where $\Delta V_{\text{to1}} = V_{\text{to1}}$–$V_{\text{to}}$. With the consideration of V_{to} value ($|V_{\text{to}}| \sim 0.8$ V) and measurement conditions ($|V_{\text{gs}}| \sim 1.8$ V), V_{gs}–V_{to} can be approximated to be 1, and then (13) becomes

$$\frac{V_{\text{gs}} - V_{\text{to}}}{V_{\text{gs}} - V_{\text{to1}}} \cong \frac{1}{1 - \Delta V_{\text{to1}}}. \tag{14}$$

L_{eff} after the X-ray irradiation with the dose of x is given by

$$L_{\text{eff}}(x) = L_{\text{eff2}} + 2L_{\text{eff1}}\frac{1}{1 - \Delta V_{\text{to1}}} \tag{15}$$

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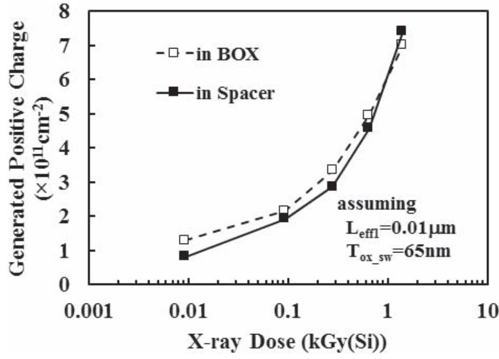

Fig. 9. Trapped hole densities as a function of X-ray irradiation dose in the BOX and the sidewall spacer. To calculate the number of the trapped holes in the sidewall spacer, it is assumed that L_{eff1} is 0.01 μm and the thickness of the sidewall spacer is 65 nm.

and that for the preradiation is also given by (5). Then, the variation of δL by the X-ray radiation, $\Delta\delta L$, is expressed by

$$\begin{aligned}\Delta\delta L &= (L_{\text{eff}}(x) - L_{\text{drawn}}) - (L_{\text{eff}}(0) - L_{\text{drawn}}) \\ &= L_{\text{eff}}(x) - L_{\text{eff}}(0) = 2L_{\text{eff1}}\frac{\Delta V_{\text{to1}}}{1-\Delta V_{\text{to1}}}. \qquad (16)\end{aligned}$$

When $\Delta V_{\text{to1}} \ll\ 1$, (17) becomes

$$\Delta\delta L = 2L_{\text{eff1}}\,\Delta V_{\text{to1}}. \qquad (17)$$

If the effective oxide thickness of the sidewall spacer is $T_{\text{ox_sw}}$, the effective generated charge in the sidewall spacer, $\Delta N_{\text{ot_sw}}$, is

$$\Delta N_{\text{ot_sw}} = \frac{\varepsilon_{\text{SiO2}}}{2qL_{\text{eff1}}T_{\text{ox_sw}}}\Delta\delta L \qquad (18)$$

where q is the elementary electron charge and $\varepsilon_{\text{sio2}}$ is the permittivity of oxide. Assuming $L_{\text{eff1}} = 0.01\ \mu$m and $T_{\text{ox_sw}} = 65$ nm, $\Delta N_{\text{ot_sw}}$ is calculated from measured $\Delta\delta L$, as shown in Fig. 9, as a function of the X-ray irradiation dose. In this figure, the generated positive charges in the BOX calculated from the back gate Vt shift of n-MOSFETs are also shown. It is confirmed that both trends for the estimated generated charges in the sidewall spacer and the BOX are almost the same. Based on these results, it is concluded that the gate length modulation by the X-ray irradiation in p-MOSFETs, which is the major cause of degradation, is the local Vt shift at gate edges due to the generated positive charge in the sidewall spacers. This effect must be enhanced when the ON-state bias is used during the X-ray irradiation instead of the OFF-state bias of this experiment. In addition, we have confirmed that the higher LDD dosage suppresses the gate length modulation effect and improves the drain current degradation by the X-ray irradiation. The detailed results will be presented elsewhere in the future.

IV. Conclusion

The X-ray irradiation-induced drain current degradation of FD-SOI p-MOSFET has been studied. The drain current degradation of 20% was observed in the linear region after the 1.4 kGy(Si) X-ray irradiation for 0.2 μm transistors in the gate length, whereas 8% for 10 μm transistors. No obvious gate length dependence of Vt shift but clear dependence of the gm degradation by the X-ray irradiation was confirmed. To investigate the mechanisms of the degradation, the analysis based on Terada's method was examined. It is found that the degradation is due to the effective gate length modulation and the external parasitic source and drain resistance but not due to the mobility reduction. The effective gate length modulation is caused by the generated positive charge in the sidewall spacers, as concluded from the model of local Vt shift induced at the gate edges. Based on this model, the radiation hardness for FD-SOI LDD p-MOSFET should be improved by higher LDD implant dosage such that the gate overlap region of LDD is extended and consequently the gate edge transistors may also be controlled solely by the gate potential, not by charges in the sidewall spacers.

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