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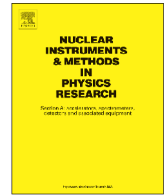

Development of $N+$ in P pixel sensors for a high-luminosity large hadron collider

Shintaro Kamada [a,*], Kazuhisa Yamamura [a], Yoshinobu Unno [b], Yoichi Ikegami [b]

[a] *Hamamatsu Photonics, 1126-1 Ichino-cho, Hamamatsu City 435-8558, Japan*
[b] *Institute of Particle and Nuclear Study, KEK, Oho 1-1, Ibaraki, Tsukuba 305-0801, Japan*

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ABSTRACT

Hamamatsu Photonics K. K. is developing an $N+$ in a p planar pixel sensor with high radiation tolerance for the high-luminosity large hadron collider (HL-LHC). The $N+$ in the p planar pixel sensor is a candidate for the HL-LHC and offers the advantages of high radiation tolerance at a reasonable price compared with the $N+$ in an n planar sensor, the three-dimensional sensor, and the diamond sensor. However, the $N+$ in the p planar pixel sensor still presents some problems that need to be solved, such as its slim edge and the danger of sparks between the sensor and readout integrated circuit. We are now attempting to solve these problems with wafer-level processes, which is important for mass production. To date, we have obtained a 250-μm edge with an applied bias voltage of 1000 V. To protect against high-voltage sparks from the edge, we suggest some possible designs for the $N+$ edge.

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1. Introduction

Several candidates exist to serve as pixel sensors for the high-luminosity large hadron collider (HL-LHC), such as the $N+$ in a p planar sensor, the $N+$ in an n planar sensor, the three-dimensional (3D) sensor, and the diamond sensor. Hamamatsu Photonics K. K. has been developing an $N+$ in the p planar pixel sensor with high radiation tolerance for the HL-LHC.

The $N+$ in the p planar sensor offers several advantages, the first of which is its cost effectiveness. Because $N+$ in p planar sensors is fabricated by a simple wafer process with masks only on a single side, the process has good yield compared with other types of sensors. In addition, in the high radiation environment, the lifetime of the $N+$ in p planar sensor is longer than that of other $P+$ in n sensors fabricated via the single-side process [1]. Because the $N+$ in the p sensor does not rely on induced type inversion after irradiation, it is possible to read signals even when the sensor is partially depleted (i.e., after the full depletion voltage has exceeded the bias voltage applied after irradiation).

However, $N+$ in p planar sensor type also has certain disadvantages, the first of which involves the width of the inactive edge, which is typically wider than the $N+$ in the n planar sensor [2] and the 3D sensor [3]. The second problem involves sparking between the sensor and the readout application-specific integrated circuit (ROIC), which occurs because the edge of $N+$ in the p sensor is exposed to high voltage and the gap between sensor and ROIC is only 20 μm. If we can overcome these problems, the $N+$ in the p planar sensor would be very competitive. Herein, we report preliminary results of research that aims to resolve these problems.

2. Slim edge

2.1. Previous results

Pixel sensors are located at the heart of large complex detectors and serve to track signals close to the interaction point. This area contains a lot of important signals, so detecting all tracks is desirable. However, it is not realistically possible to detect all tracks that cross a pixel sensor because of the dead area of sensors. The edge of an ordinary pixel sensor constitutes such a dead area because a certain distance is needed to prevent the depletion region from contacting the dicing edge.

In a previous study [4], by shrinking the distance from the active area to the dicing edge to 400 μm, we obtained a tolerance of over 1000 V (see Figs. 1 and 2). However, at 1000 V and with less than 400 μm from active area to dicing edge, the depletion region contacted the dicing edge, and a significant leakage current flowed from the dicing edge. Thus, 1000 V tolerance was not possible with an edge distance of less than 400 μm.

* Corresponding author.
E-mail address: skamada@ssd.hpk.co.jp (S. Kamada).

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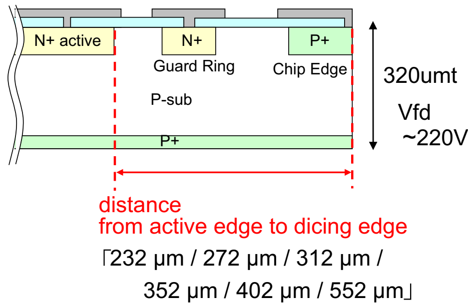


Fig. 1. Cross-section of previous slim-edge trial. The edge was shrunk by a simple planar process.

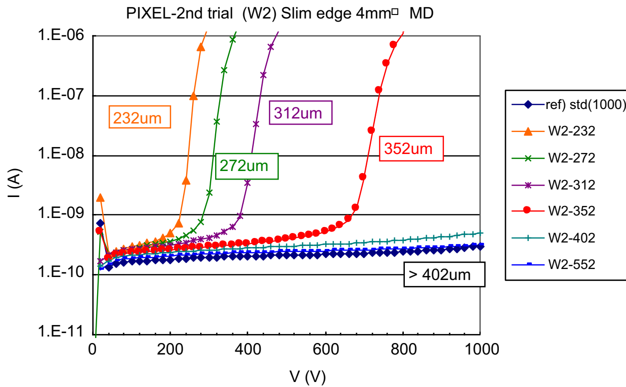


Fig. 2. *I–V* curves from previous slim-edge trial. For an edge distance of less than 400 μm, the voltage tolerance was less than 1000 V.

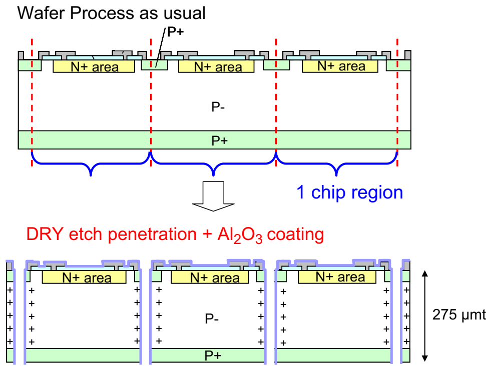


Fig. 3. Process flow for slim-edge trial.

2.2. Slim edge process

To overcome this limit, a new technology had to be developed to prevent the depletion region from contacting the sensor edge. We based our approach on the sidewall Al_2O_3 passivation trial by SCIPP [5] and expanded the technology to the wafer process. Note that completing the process on wafer form is important for mass production.

For our first trial, we used a square 4-mm monitor diode and made one side the slim edge. Fig. 3 shows the process flow.

1. Fabricate *PN* junction and metallize as usual.
2. Penetrate through wafer by dry etching. In this trial, standard trench width was 200 μm, and in addition, we confirmed 20 μm width trench also went well.
3. Deposit Al_2O_3 by atomic layer deposition (ALD). Just before the deposition, we executed a process of eliminating a thin native oxide layer. The total thickness of Al_2O_3 was 30 nm. Al_2O_3 layer made by ALD gives good coverage of the side wall. The Si–Al_2O_3 or SiO_2–Al_2O_3 interface makes positive charges at the Si surface. The depletion layer and negative space charge in the *p*-type wafer are suppressed by the positive charges that accumulate at the Si surface, and the depletion region does not touch the sensor edge. Thus, no leakage current flows from the sensor edge.
4. The final process is dicing of non-slim edge lines.

2.3. Test pattern to evaluate minimum distance

To evaluate the minimum distance, we fabricated a test pattern consisting of a 4-mm monitor diode with a single slim-edge side, as shown in Figs. 4 and 5. We made four types, which were distinguished by the distance from the active area to edge of 210, 250, 290, and 310 μm.

The current–voltage (*I–V*) results are shown in Fig. 6. The data indicating a tolerance of 1000 V is obtained for over 250 μm from the active area to slim edge. In addition, we also confirmed the poor *I–V* characteristics and low voltage tolerance when Al_2O_3 passivation was not used. Thus, the Al_2O_3 charge effect contributed to the good *I–V* characteristics, which implies that the depletion region was not contacting the sensor edge.

For the 210-μm edge pattern, breakdown occurred at 700 V. However, by observing the hot electrons [6], we confirmed that the breakdown occurred between guard-ring *N+* and edge *P+*. This breakdown was induced by the strong electric field across the narrow *PN* gap, not by contact between the slim edge and depletion region. Thus, by optimizing the design, we may obtain a tolerance of 1000 V with an edge of less than 200 μm. This work is planned for the near future.

2.3. Apply slim edge to a 20-mm pixel sensor for FE-I4 ATLAS-upgrade

As mentioned in the previous section, we confirmed the 250-μm slim edge by using a 4-mm monitor diode. Next, we applied this

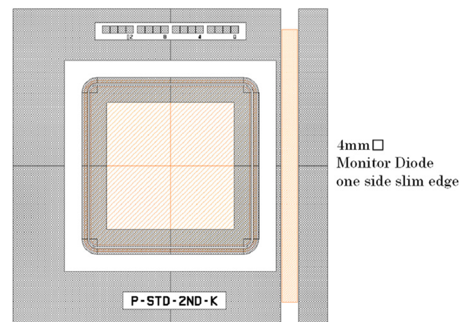


Fig. 4. Top view of test pattern consisting of 4-mm monitor diode and a single slim-edge side.

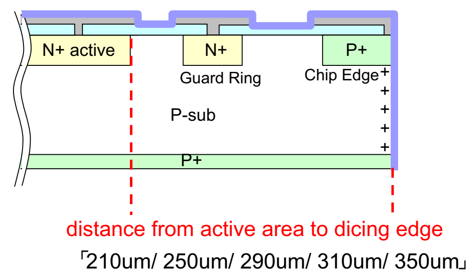


Fig. 5. Cross-section of test pattern.

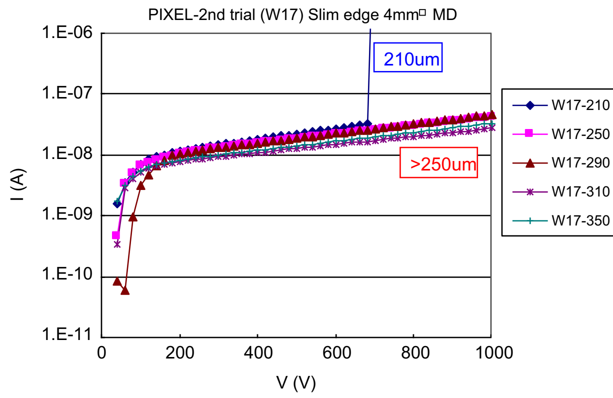


Fig. 6. *I–V* curve for slim-edge trial. For 250 μm, 290 μm, 310 μm, and 350 μm from active area to slim edge, a tolerance of 1000 V was obtained.

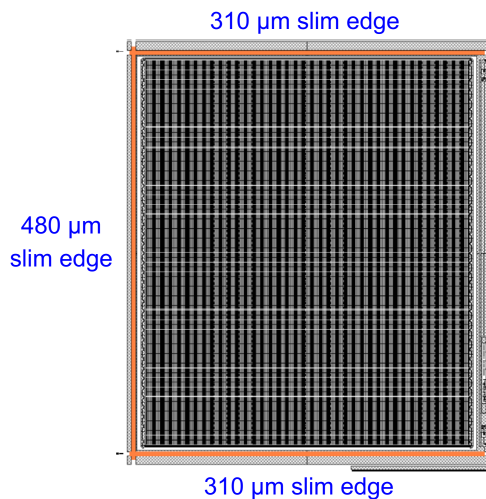


Fig. 7. Top view of a 20-mm pixel sensor. We fabricated slim edges on three sides.

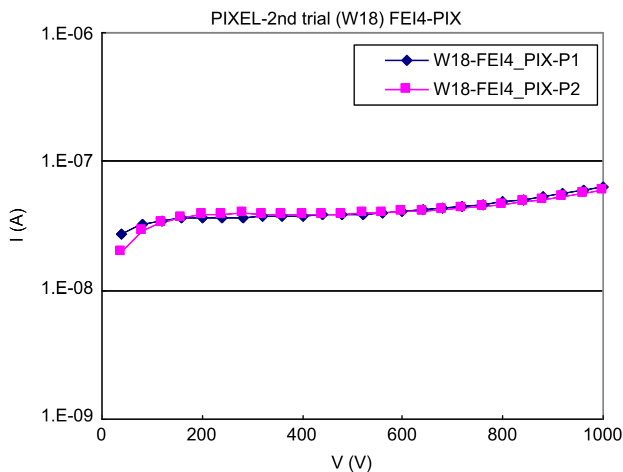


Fig. 8. *I–V* curves for the 20-mm pixel sensor with slim edges on three sides. The voltage tolerance was greater than 1000 V.

technology to a real pixel sensor for the FE-I4 ATLAS upgrade. The pixel sensor surface area is about 20 × 20 mm^2 and the thickness is 275 μm. We fabricated slim edges on three sides by Si penetration and Al_2O_3 passivation.

As shown in Fig. 7, slim-edge distances in this trial were 310 and 480 μm, which are wider than those for the trial described in Section 2.3. The reason for the larger edges in this trial is that we applied the edge-slimming process to existing wafers that were not optimized for minimum-edge design. However, 310-μm edges were sufficiently slim for our purpose. As mentioned in Section 2.1, a 310-μm edge fabricated by the usual planar process has a tolerance of only 400 V. Fig. 8 shows the *I–V* results for this trial. The results confirm the good *I–V* characteristics and the tolerance of over 1000 V.

Based on these results and those of Sections 2.3, we believe it is possible to fabricate three-side slim-edge detectors with edges of less than 250 μm. This study is planned for the near future.

2.4. Reliability test of slim edge under UV irradiation

Thus far, we have discussed the desirable results regarding the initial characteristics of the detector. However, we must guarantee that these good characteristics still apply in the HL-LHC environment. To determine this, we used irradiation experiments to simulate the HL-LHC environment. These experiments were done at KEK and consisted of irradiating these samples by 70 MeV protons. The results should be available in the near future and will be reported in a future presentation.

To obtain results more rapidly, we tested the resistance of the samples to UV irradiation. The samples consisted of 4-mm monitor diodes with a single slim-edge side. However, these samples differed from those described in Section 2.2 (those samples were not available in time for irradiation tests). The samples used for UV-irradiation experiments had a wafer thickness of 275 μm and trench depth of 160 μm (i.e., not penetrated). We used deposited Al_2O_3 and stealth dicing in various lines, as shown in Fig. 9.

The distance from the active area to trench was a constant 350 μm, and that from the active area to dicing edge was 360, 400, and 450 μm. Fig. 10 shows the initial *I–V* characteristics of the samples.

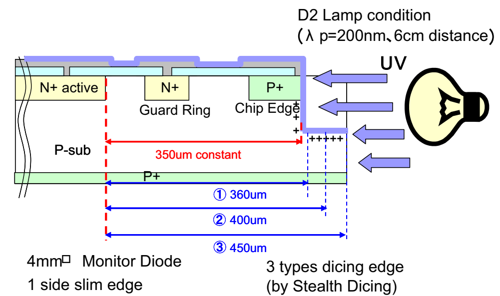


Fig. 9. Cross-section of slim-edge pattern and setup for UV irradiation.

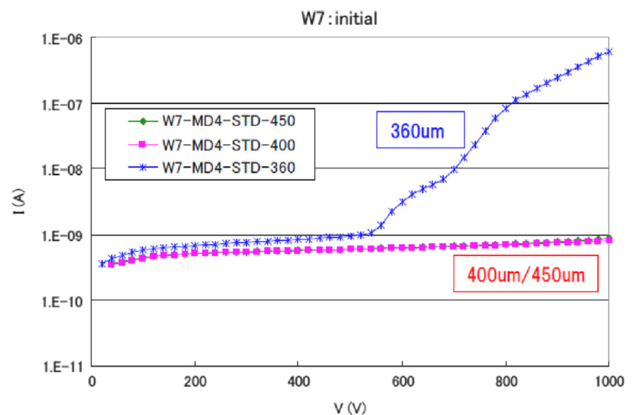


Fig. 10. *I–V* curves for test pattern from Fig. 9.

Breakdown occurred at 600 V for the 360-μm edge. However, the 400 and 450 μm edges had a tolerance of over 1000 V. These results indicate two things: first, when the depletion region reaches the trench, the leakage current did not increase by the Al_2O_3 interface charge. Second, when the depletion region reached the dicing edge, significant leakage current flowed from the dicing edge, which was the case for the 360-μm edge. Thus, the samples with 400 and 450 μm edges had a tolerance of 1000 V because of the Al_2O_3 interface charge and sufficient distance to the dicing edge.

Next, we describe the experimental conditions and discuss the results of the UV irradiation experiment. The UV spectrum is shown in Fig. 11. The peak wavelength was 200 nm and the irradiation intensity was about 0.1 μW/cm^2 at 50 cm from the source. In the experiments, the UV source was about 6 cm from the sample.

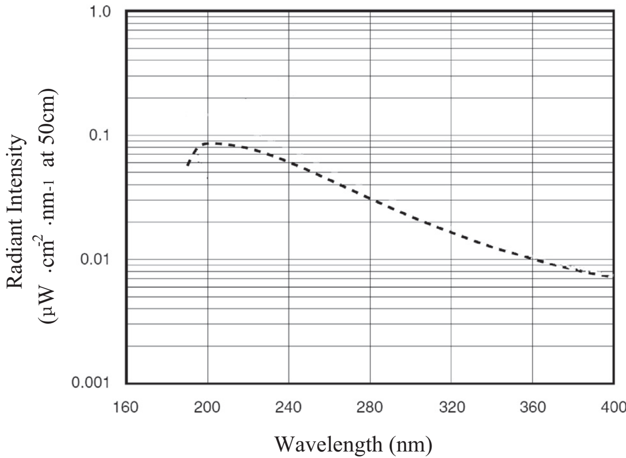


Fig. 11. Spectrum of a D2 lamp used for reliability experiments.

We irradiated the Al_2O_3 side wall with UV light, as indicated in Fig. 9. Irradiation time was up to 111 h. Fig. 12 shows the *I–V* results for various irradiation times.

Ten hours of UV irradiation produced no change from the initial result. However, after 25 h of UV irradiation, the leakage current from 400- and 450-μm edges increased at about 600 V. After 111 h of UV irradiation, the *I–V* characteristics were essentially the same as for 25 h of UV irradiation.

We attribute these results to the disappearance of the Al_2O_3 interface-charge effect, which allows the depletion region to contact the trench edge. But the increase in the dark current for the samples with 400- and 450-μm edges was more moderate than for samples with a 360-μm edge, which we explain as follows: for the 400- and 450-μm-edge samples, the depletion region contacted only the trench edge (not the dicing edge), and the trench edge is less damaged by the dry-etching process. As for the disappearance of the Al_2O_3 interface-charge effect, we cannot determine the cause, but we guess two possibilities. One is the change of Al_2O_3 layer itself. Short wavelength light (<300 nm) may generate and accumulate holes to Al_2O_3 layer. The other cause may be charge up of SiO_2 under the Al_2O_3 layer. In any case, we need to do irradiation test assumption for the HL-LHC.

3. Edge-spark protection

We now discuss edge-spark protection, which is mainly in the planning phase. Normally, $N+$ in p planar sensors has $P+$ edges to prevent depletion from spreading to the dicing edge. In addition,

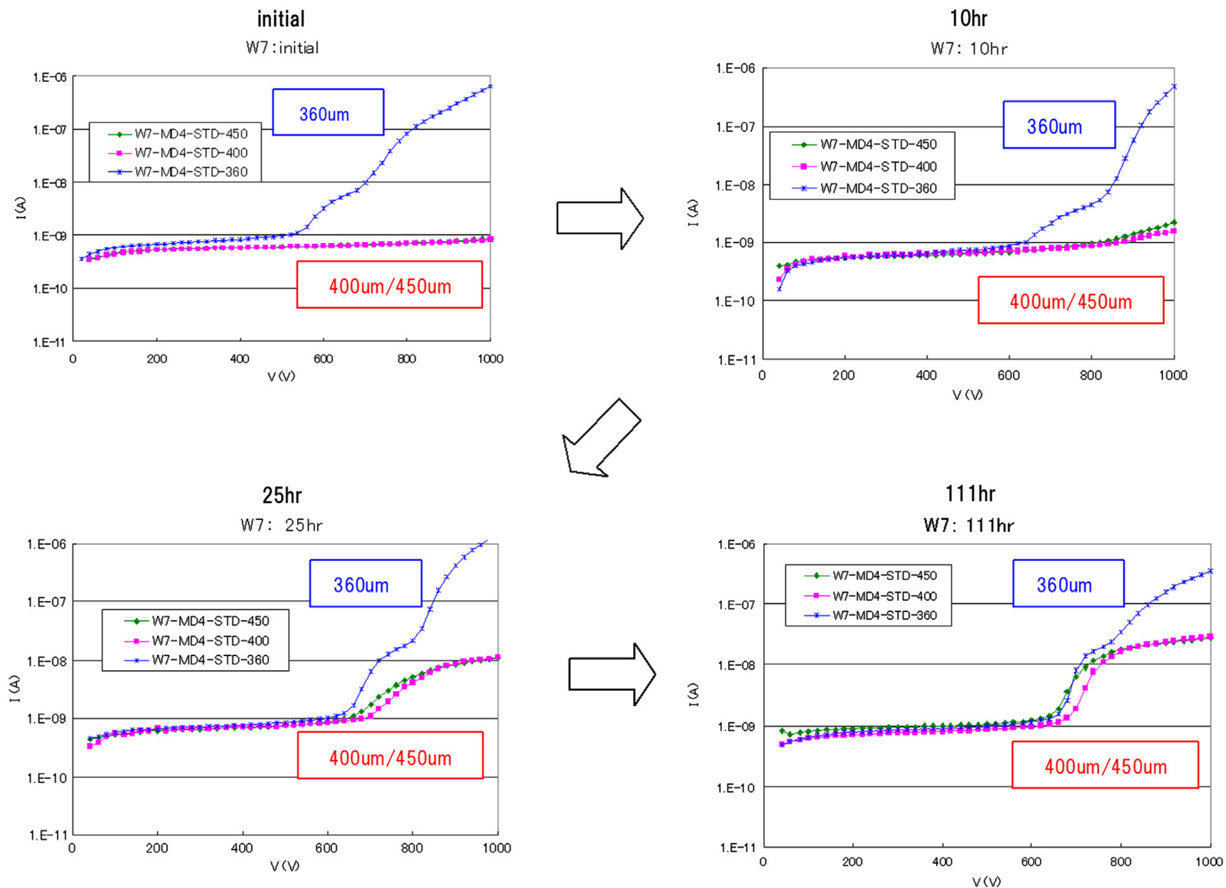


Fig. 12. *I–V* curves after UV irradiation of samples for up to 111 h.

high voltage (from a few hundred volts to 1000 V) is applied from the backside to obtain full depletion, and the voltage of the $P+$ edge is high because the carrier types going from the back side to the front side are all the same. However, the ROIC is near zero volts, and the ROIC–sensor gap is only about 20 μm. Thus, sparks may occur between sensor and ROIC, which destroys the device.

Various approaches have been taken to avoid this problem, for example, inserting a dielectric adhesive [7]. In fact, inserting a dielectric adhesive produces good results, but it needs to be done after dicing, so it is not suitable for mass production.

To overcome this problem, we take a different approach, which involves a countermeasure in the wafer process and so is suitable for mass production. The concept is simple: make an $N+$ edge (instead of $P+$) and drop the edge voltage (as shown in Fig. 13). At this point, this approach is at the stage of proof-of-principle test, but in the near future experiments are planned to test it with a pixel sensor.

3.1. Simulation of edge voltage

To roughly estimate the trend in edge voltage, we simulated three types of $N+$ in p planar sensors:

Type A: standard $P+$ edge.
Type B: $N+$ edge with no isolation.
Type C: $N+$ edge with P-spray isolation (we suggest this type).
Types B and C are new types, and we suggest type C to solve the problem of edge sparks.

The simulation conditions were as follows: assume a diode structure with high voltage applied from the back side. The $N+$ active region was ground and the guard ring was floating.

The dicing edge was assumed to be an ideal clean surface to simplify the simulation (i.e., we did not consider dicing damage). Fig. 14 shows the results of the simulation of the edge voltage.

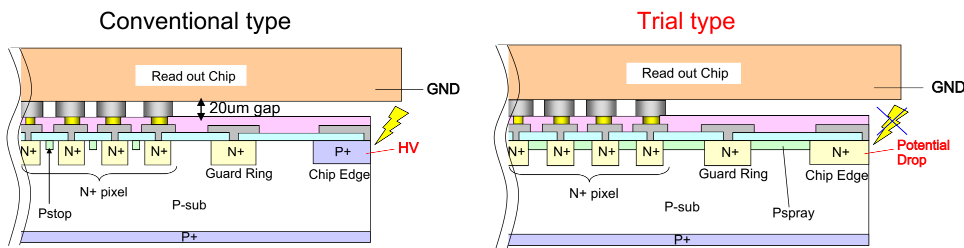
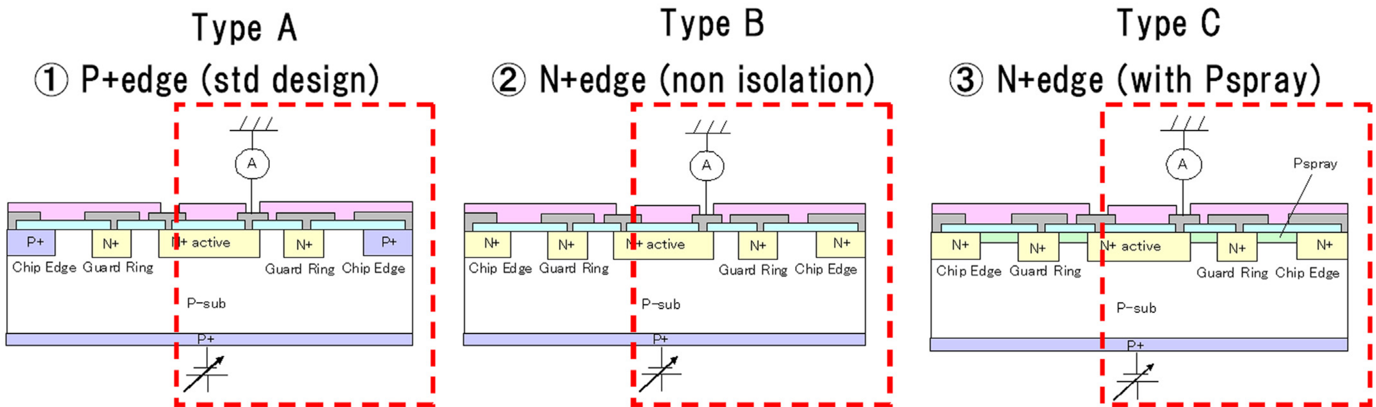
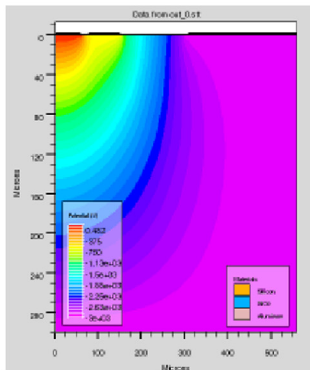
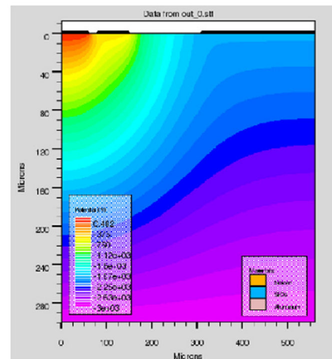
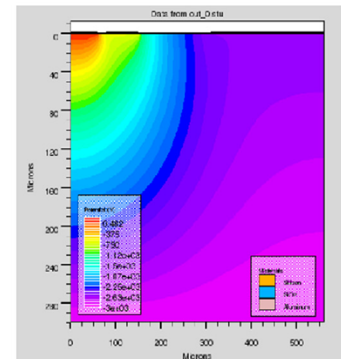


Fig. 13. Concept for protection of edge against high voltage.









chip edge potential dropped

chip edge potential dropped

Fig. 14. Simulation of edge voltage for sample types A, B, and C.

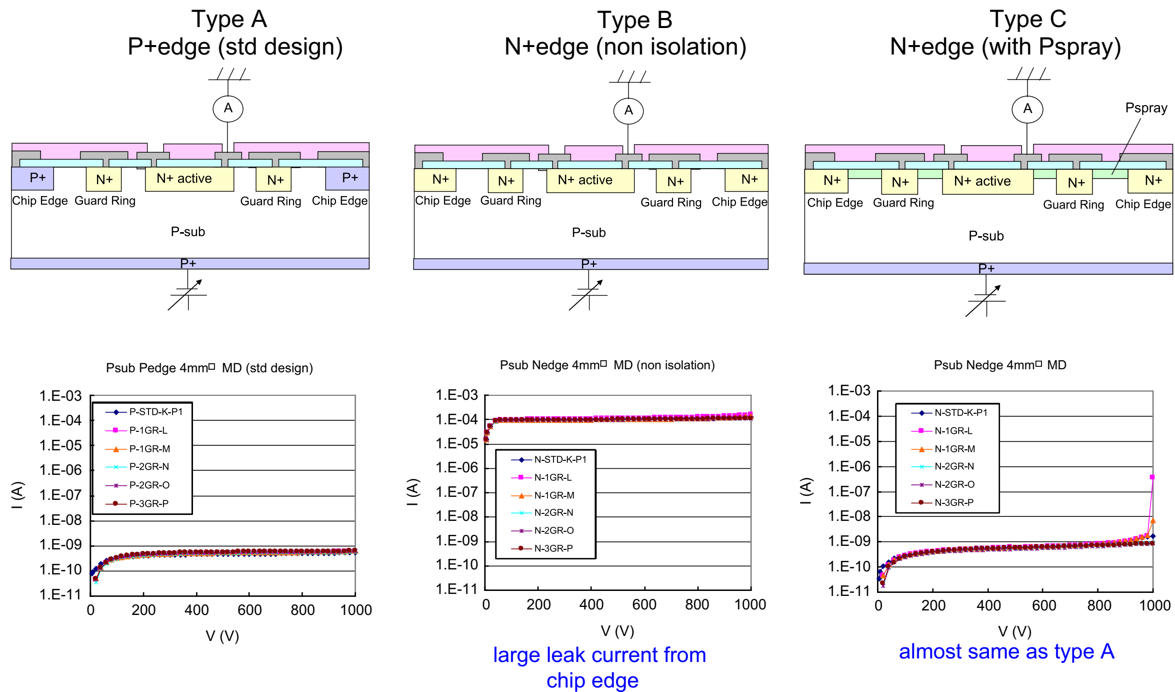


Fig. 15. *I–V* curves for structure types A, B, and C.

Type A: edge voltage was equal to the backside voltage.
Type B: edge voltage was approximately 50% of the backside voltage.
Type C: edge voltage was approximately 80% of the backside voltage.

3.2. I–V experiment for three types of structures

Initially, we fabricated structure types A–C as monitor diodes by chance. This time, we measured the *I–V* characteristics (see Fig. 15). For all type, the distance between the active area and the edge implant was 320 μm.

Type A: flat *I–V* curve up to 1000 V.
Type B: very large leakage current from chip edge even at 5 V.
Type C: almost same *I–V* curve as for type A.

Thus, based on these results and those presented in Section 3.1, structure type C presents a good possibility because of both the voltage drop and *I–V* characteristics.

3.3. Easy test for edge-spark protection

We used an easy test to evaluate edge-spark protection. Ideally, the evaluation should be done with a real pixel sensor that is bump bonded with an ROIC. However, because we did not have a real pixel sensor with an $N+$ edge, we used the 4-mm monitor diode mentioned in Section 2.2 instead. Thus, we used the temporary setup shown in Fig. 16 to evaluate edge-spark protection.

On the bottom side, we set types A–C 4-mm monitor diode and applied the high voltage from the backside. On the top side, we set the type A 4-mm monitor diode and applied the ground from the back side. Between the lower and upper sensors, we inserted a 60-μm-thick mending tape, so the gap was about

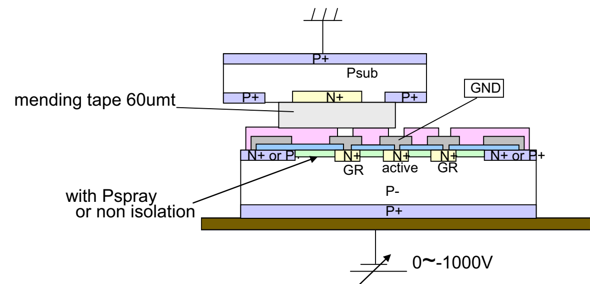


Fig. 16. Setup of easy test to evaluate edge-spark protection.

60 μm, which was wider than the 20 μm of the real bump bonding gap.

The results were as follows:

Type A: edge spark occurred at 740 V.
Type B: no edge spark occurred, even at 1000 V.
Type C: edge spark occurred at 960 V.

As mentioned before, this is only a preliminary test, but the result implies that an $N+$ type edge should work well for edge-spark protection. We are currently processing wafers to produce $N+$ edge pixel sensors and will demonstrate bump bonding and edge-spark evaluation. We expect results in the near future.

4. Summary

Hamamatsu Photonics K. K. has been developing $N+$ in p planar pixel sensors with high radiation-tolerance for the HL-LHC. For the slim edge, we applied Al_2O_3 sidewall passivation technology for wafer processing and achieved a tolerance of 1000 V with a 250-μm edge. The results also suggest that by

optimizing the design, it would be possible to obtain less than 250 or 200 μm. This is our next step.

We used UV irradiation tests to evaluate the reliability of the Al_2O_3 slim edge. After UV irradiation, the Al_2O_3 interface charge disappeared. Other reliability tests are planned that simulate the conditions of the HL-LHC.

For edge-spark protection, we suggest using an $N+$ edge with an isolation structure. Results on edge-spark protection are expected in the near future.

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