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Development of n-in-p silicon planar pixel sensors and flip-chip modules for very high radiation environments

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ABSTRACT

In this paper we present R&D of n-in-p pixel sensors, aiming for a very high radiation environment up to a fluence of 10^{16} n_{eq}/cm^2. To fabricate these sensors, two batches with different mask sets were employed: the first resulted in pixel sensors compatible with the ATLAS pixel readout frontend chip called FE-I3, and the second in FE-I3 and a new frontend chip, FE-I4, compatible sensors; small diodes were employed to investigate the width from the active diode to the dicing edge and the guard rings. Tests involving the diodes showed that the strong increase of leakage current was attributed to the edge current when the lateral depletion zone reaches the dicing edge and the lateral depletion along the silicon surface was correlated with the 'field' width. The onset was observed at a voltage of 1000 V when the width was equal to ~400 μm. The pixel sensors that were diced at a width of 450 μm could successfully maintain a bias voltage of 1000 V. Hybrid flip-chip pixel modules with dummy and real chips were also fabricated. Lead (PbSn) solder bump bonding proved to be successful. However, lead-free (SnAg) solder bump bonding requires further optimization.

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1. Introduction

A characteristic case of a very high radiation environment is the Large Hadron Collider (LHC) and the future Super LHC (SLHC). While the ATLAS experiment [1] at the LHC collects proton collision data of approximately 700 fb^{-1}, the inner detector (ID) is exposed to an integrated particle fluence of $\sim 2\times 10^{14}$ and $\sim 3\times 10^{15}$ (1-MeV neutron equivalent (n_{eq}))/cm^2, including a safety factor of 1.5 for the luminosity, at distances (R) of 30 cm (microstrip detectors) and 5 cm (pixel detectors) from the collision point, respectively. LHC is planned to be upgraded to SLHC with the ultimate aim to maximize its research capabilities by achieving one order of magnitude higher luminosity ($\sim 10^{35}$ cm^{-2} s^{-1}) and an integrated luminosity of $\sim$3000 fb^{-1}. By including a safety factor of 2 for the integrated luminosity, the inner detector of SLHC is then expected to be exposed to fluencies of $\sim 1\times 10^{15}$ and $\sim 2\times 10^{16}$ n_{eq}/cm^2 at distances of 30 and 5 cm, respectively. It should be noted that the fluence of neutrons dominates that of other charged particles at $R \geq 25$ cm.

Over the past year, R&D efforts for highly radiation tolerant silicon microstrip sensors have been made on n-in-p microstrip sensors [2,3] and many were reported in conferences [4,5]. Our recent fabrications were miniature sensors of 1 cm × 1 cm and large area sensors of 9.75 cm × 9.75 cm using 6-in. (150 mm diameter) wafers made of p-type float-zone (FZ) material with a thickness of 320 μm at Hamamatsu Photonics K.K. (HPK) [6]. These include an innovative design for n-in-p sensors that promises a significantly enhanced leakage current performance without breakdown (onset of microdischarge) up to a voltage of 1000 V [7,8]; extensive testing of radiation damage expected with proton and neutron fluencies is up to $\sim 10^{15}$ 1-MeV n_{eq}/cm^2 [9,10], and as an example of usage, single- and double-sided prototype modules fabricated on the basis of large area n-in-p sensors [11,12].

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By utilizing the achievements obtained in the strip sensors, we have fabricated n-in-p pixel sensors with a goal of R&D efforts to develop a device that can operate under particle fluences $\geq 10^{16}\ n_{eq}/cm^2$, and a bias voltage up to 1000 V in order to achieve enhanced charge collection capabilities than charge trapping in the bulk of silicon wafers heavily damaged by radiation. An additional aim is to address the 'charge multiplication' effect that is observed in heavily damaged silicon sensors whose thickness is as small as 150 μm under bias voltages as high as 1000 V [13]. Another goal of R&D is to evaluate the required width from the end of the active diode to the dicing edge in order to minimize the insensitive area.

2. R&D of n-in-p sensors

Two batches of 6-in. wafers were processed using different mask sets. The fist mask set (batch/wafer #1), as shown in Fig. 1(a), was composed of pixel sensors in a section named as parts 1–29, among which the numbers between 12 and 16 and between 26 and 29 were the ones compatible with the pixel readout frontend chip called FE-I3 [14] of ATLAS pixel detector. The second mask set (batch/wafer #2) is shown in Fig. 1(b). This mask was composed of pixel sensors compatible with FE-I3 and a new much larger pixel readout frontend FE-I4 [15] chips: FE-I3 and FE-I4 single-chip compatible (parts number 1–7 and 34–39), FE-I4 double-chip compatible (28–33), FE-I3 quad-chip compatible pixel sensors (40–42), together with other various pixel sensors. The small square parts at the perimeter in both mask sets were diodes used for the study of effects of the sensors' slim edges and the guard rings.

In batch #1, pixel sensors and diodes were processed in p- and n-type wafers to make n-in-p and p-in-n samples. The nominal thickness of the wafers was 320 μm, while a number of n-type wafers were thinned down to the thickness of 200 μm. The resistivities of p-type and n-type wafers were ~7 and ~4 kΩ cm, respectively. The isolation of n+ pixels of the n-in-p pixel sensors was achieved by a p-stop structure with a concentration of 4×10^{12} Boron ions/cm^2. From batch #1, FE-I3 single-chip compatible pixel sensors were used later for bump bonding and in a test beam (see Section 4.1). The pixel structure (polysilicon biasing and a 'common-type' p-stop structure) used for the test beam is shown in Fig. 1(c).

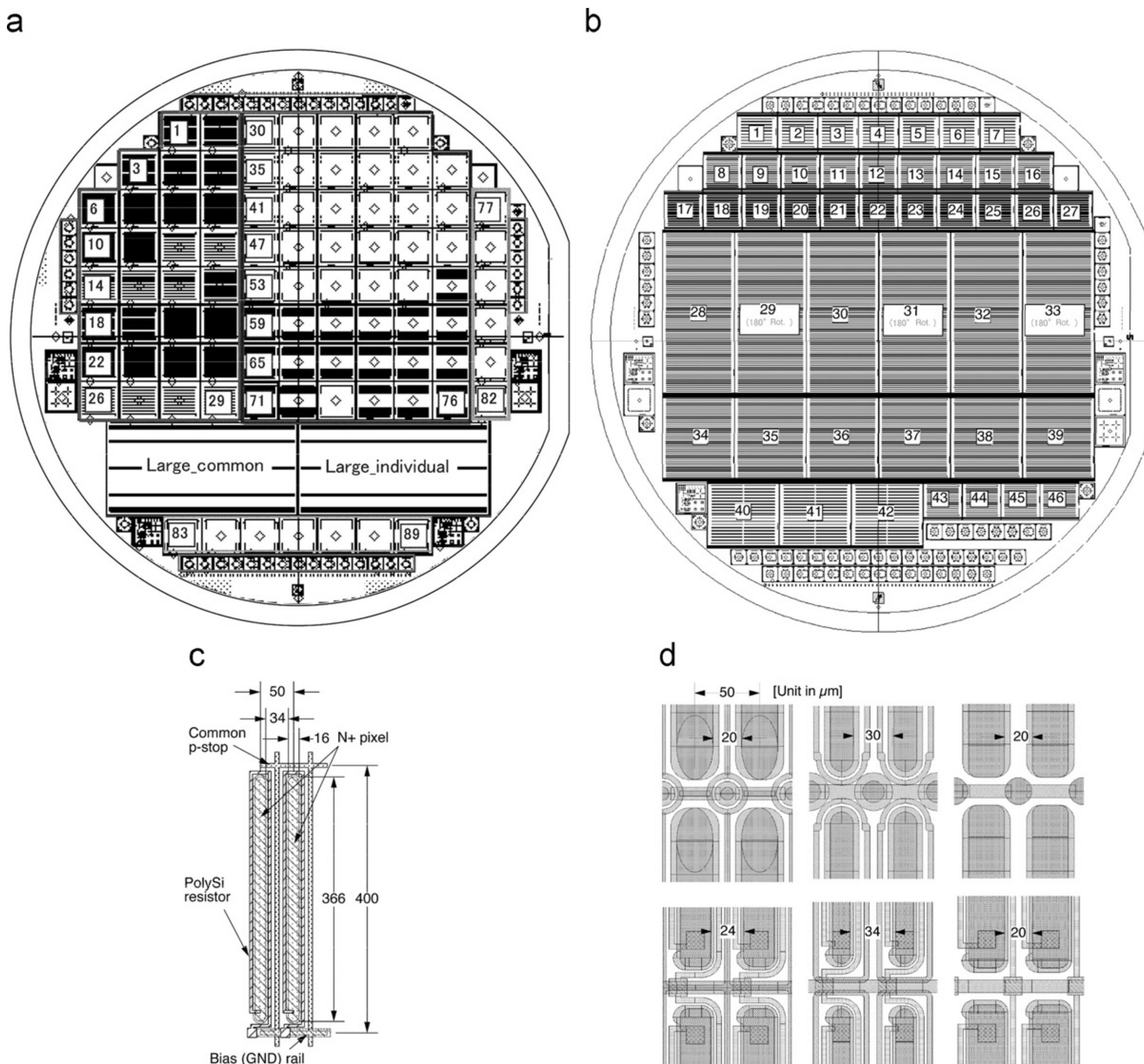

Fig. 1. Layout of the mask sets: (a) batch/wafer #1, FE-I3 compatible pixel sensors (parts number 12–16, 26–29) and with various pixel designs (the rest of 1–29); (b) batch/wafer #2, FE-I3 compatible sensors (1–7), FE-I4 double-chip compatible sensors (28–33), FE-I4 single-chip compatible sensors (34–39), and FE-I3 quad-chip compatible sensors (40–42). The small square parts at the perimeter are diodes, which have been added for the study of effects of the sensor's slim-edge and the multiple guard rings; (c) a pixel structure with a polysilicon bias resistor and a common p-stop structure in batch #1; (d) biasing and isolation structures for pixel sensors in batch #2, 4-to-1 PT combined with a common p-stop isolation (top-left), individual p-stop structure (top-middle), p-spray (top-right) isolation, polysilicon bias with common p-stop isolation (bottom-left), individual p-stop (bottom-middle) and p-spray isolation (bottom-right).

In batch #2, the outer dimensions of the FE-I4 pixel sensors leave the possibility of dicing them at 360, 450, 600, 750, and 1011 μm nominally along the longitudinal-pixel side edges. Each pixel's structure is a combination of n-side isolation and biasing substructures as shown in Fig. 1(d). The n-side isolation was achieved by either common or individual p-stops of a concentration of 4×10^{12} ions/cm^2 or p-sprays of 2×10^{12} ions/cm^2. The biasing structure was made of punch-through structures or polysilicon resistors including punch-through structures having 4 pixels per one bias dot (4-to-1 PT) or one pixel to one dot (1-to-1 PT). Only p-type wafers were processed. The nominal thickness of each wafer was 320 μm and a number of wafers were being thinned down to 150 μm.

Studies on different kinds of punch-through structures were performed in the past [16]. In order to reduce potentially less-efficient area resulting from the bias dot in each pixel, we introduced one bias dot at the corner of 4 pixels (4-to-1 PT) and polysilicon biasing (Fig. 1(d): top figure for the 4-to-1 PT with the common, individual, and p-spray isolation). Alternatives based on polysilicon resistors are shown in the bottom figures for all different isolation structures. It should be noted that in the case of 4-to-1 PT structures, the gap between two adjacent pixel implants is 20 μm in both the common p-stop and the p-spray isolations. In the case of polysilicon resistors, the gaps are 24 and 20 μm, respectively. On the other hand, in the case of individual p-stop isolation the gaps are wider, 30 and 34 μm in the 4-to-1 and in the polysilicon resistor, respectively. The requirement of not having a significant signal distribution to the neighbor pixels within a typical shaping time of 25 ns leads to a lower limit of the inter-pixel resistance of ~1 MΩ [16]. Thus, the polysilicon biasing of ~2.7 MΩ in the batch/wafer #2 is sufficient and could be a good stable solution. The main features of wafers and pixel sensors are summarized in Table 1.

Table 1
Main features of wafers and sensors.

Silicon wafer diameter	6-in. (150 mm)		
Type	FZ (high grade)		
Orientation	<1 0 0>		
Resistivity (bulk type)	~7 (p), ~4 (n) kΩ cm		
Thickness	320 μm (nominal)		
Thinned	200 μm (n-type), 150 μm (p-type)		
FE-I3 compatible pixel sensor: single-chip			
Sensor dimensions	10.5 mm × 10.0 mm		
Pixel dimensions	50 μm × 400 μm[a]		
Number of pixels	164 × 18 = 2952		
FE-I4 compatible pixel sensor: single-chip			
Sensor dimensions	18.7 mm × 20.9 mm[b]		
Pixel dimensions	50 μm × 250 μm		
Number of pixels	336 × 80 = 26,880		
FE-I4 compatible pixel sensor: double-chip			
Sensor dimensions	18.7 mm × 41.3 mm[b]		
Pixel dimensions	50 μm × 250 μm		
Number of pixels	336 × 160 = 53,760		
n+ pixel isolation:			
p-stop (common or individual)	4×10^{12} ions/cm^2		
p-spray	2×10^{12} ions/cm^2		
Bias structures:			
Punch-through	4-to-1 or 1-to-1		
Polysilicon	~1 MΩ (batch #1), ~2.7 MΩ (batch #2)		
Parts no.:	**4-to-1 PT**	**1-to-1 PT**	**Polysilicon**
p-stop (common)		#1–13,-27	#1–15,-29
	#2-1	#2–4	#2–6
	#2–28,-29,-34		#2–37
	#2–40		
p-stop (individual)		#1–12,-26	#1–14,-28
	#2-2	#2–5	#2–7
	#2–30,-31,-35		#2–38
	#2–41		
p-spray	#2-3		
	#2–32,-33,-36		#2–39
	#2–42		

[a] Outermost pixels are 600 μm long.
[b] In the case that the edge width is 450 μm.

3. Results

3.1. Slim-edge diodes

Silicon sensors exploiting the depleted volume inside the silicon wafer require extra edge space so that the depleted volume is confined away from the dicing edge. As this extra edge space is an insensitive volume, there is increasing interest to minimize this space. In order to investigate the required space systematically, we fabricated 'slim-edge' diodes of various edge widths.

In our design, the edge termination is achieved with only two guard rings, one close to the active diode and another at the dicing edge. The layout of such a diode and a schematic diagram for the width definition are shown in Fig. 2. Both p+ and n+ implantations in the guard ring at the dicing edge were prepared irrespective of the bulk material. In the subsequent measurements, either n-bulk/n+ edge or p-bulk/p+ edge samples were used. The thicknesses of the n-bulk material were 320 μm (W5) and 200 μm (W7, 13), where the names in the parentheses are for the wafers' identification. The thickness of the p-bulk sample was 320 μm (W3). The total edge width, from the edge of the diode to the dicing edge, ranged between 80 and 640 μm, and between 280 and 1011 μm, in the n- and p-bulk materials, respectively.

The leakage current as a function of bias voltage for various p-bulk samples is shown in Fig. 3. A strong increase of leakage current was observed in the narrow width samples at lower bias voltages, which can be attributed to the increase of edge current when the lateral depletion zone reaches the dicing edge.

In Fig. 4, relationship between the total edge width and the square root of the onset voltage ($\sqrt{V_{bias}}$) at the strong increase of leakage current is summarized in p-bulk/p+ edge samples (top panel) and in n-bulk/n+ edge samples (bottom panel). In both panels, a near-linear dependence of the onset voltage on the total edge width is observed. The onset voltage reached the value of 1000 V (i.e., $\sqrt{V_{bias}}$ of 31.6 V) when the total edge width was equal to ~400 μm, irrespective of the bulk material or its thickness. From the linear dependence of the square root of the bias voltage on total edge width, we concluded that the onset voltage and the total edge width were defined by the laterally depleted volume along the surface of silicon wafer.

3.2. Guard rings

The guard rings are implemented in the context of the edge termination for high voltage operation [16]. Recently, investigations have been made in the context of reducing the insensitive edge space [17]. Our next step was to systematically investigate the role of the guard rings in the edge space. For this purpose, samples of small diodes were fabricated by varying the number of guard rings (1–3 GR), the total width of the guard rings (N, M, W), and the width of the edge implantation. The layouts of the multiple guard rings are shown in Fig. 5.

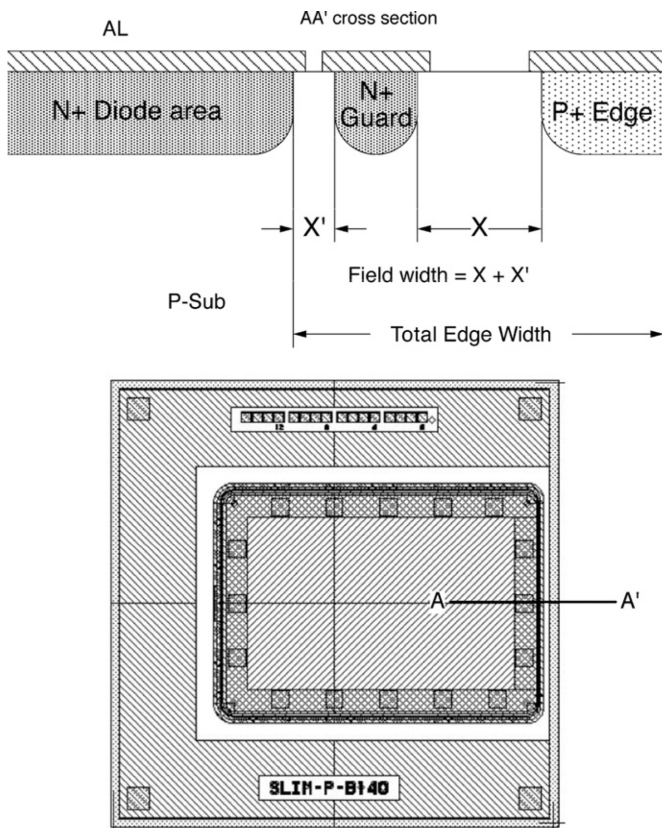

Fig. 2. An example of slim-edge diodes (4 mm × 4 mm) with a narrowed edge width.

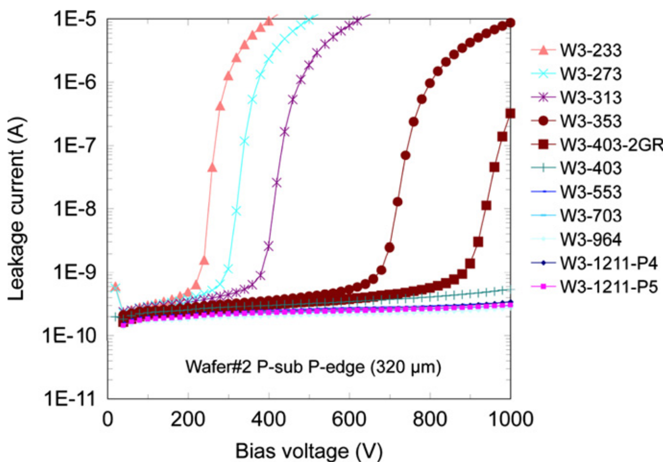

Fig. 3. Strong increase of leakage current observed in the slim-edge diodes as a function of bias voltage. In the legend, 'nnn' following W3 (W3-nnn) denotes the total edge width of the sample.

The onset voltage of strong increase of leakage current was measured in the n-bulk/p+ edge samples. In n-bulk/n+ edge samples where the edge space was as large as 1000 μm, the onset could not be observed for bias voltages up to 1000 V.

In analyzing the data, we used the 'field' width as defined by the width of the surface without implantation (see Fig. 2). The relation between the total 'field' width and the square root of the onset voltage of strong increase of leakage current of the guard ring samples is shown in Fig. 6. Shown together with this is the relation of the n-bulk/p+ edge samples in the 'slim-edge' diodes. From the linear relation, we concluded that lateral depletion along the 'field' surface of silicon wafer was the fundamental factor of defining the edge space and the surface implantation was shortening the silicon surface owing to its characteristic low resistivity.

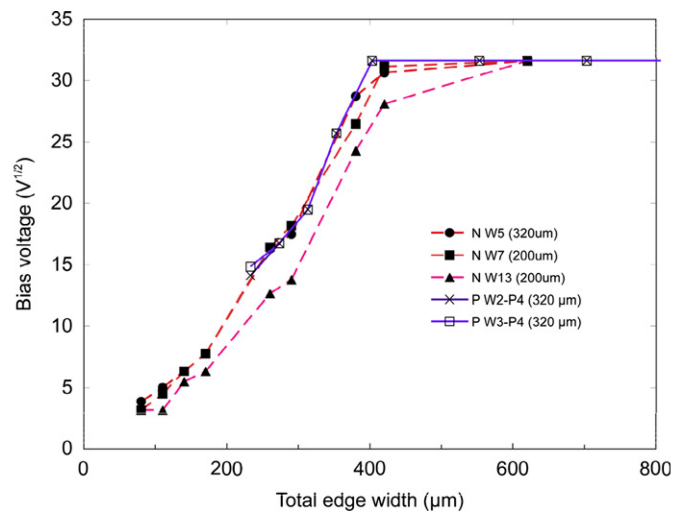

Fig. 4. Square root of bias voltage as measured at the strong increase of leakage current as a function of total edge width. The letter 'N' or 'P' in the legend indicates the bulk material. The data point at 1000 V (i.e., $\sqrt{V_{bias}}$ of 31.6 V) indicates that the strong increase of leakage current is above 1000 V.

3.3. FE-I4 double-chip compatible pixel sensor

The typical leakage current dependence on bias voltage (*I–V*) applied to the FE-I4 double-chip compatible n-in-p pixel sensors with a 4-to-1 PT biasing structure is shown in Fig. 7. The sensor was 320 μm thick and the total edge width was equal to 450 μm. The n-side isolation was of either a common p-stop (COM) or an individual p-stop (IND) structure with a p-concentration of 4×10^{12} ions/cm^2 (P4), or a p-spray structure with a concentration of 2×10^{12} ions/cm^2 (R2).

The COM-P4 and IND-P4 samples exhibited excellent *I–V* characteristics, while the onset of microdischarge was not observed for voltages up to 1000 V. On the contrary, increase of leakage current was observed in the R2 samples at a significantly lower voltage. We attributed this difference to the higher electric field at the contact of the n+ pixel and p+ spray and possible microscopic defects at the edge of the n+ pixel implantation.

It should be noted that the level of saturation of the leakage current in the area of ~3.3 cm^2 was equal to ~4 nA/cm^2, which is consistent with the level of saturation of leakage current of ~7 nA/cm^2 observed in a small diode of ~0.04 cm^2 (see Fig. 3). This fact supports that the leakage current is proportional to the sensor area and 4-to-1 PT biasing to each pixel is successfully working.

In samples of FE-I3 single-chip compatible p-in-n pixel sensors thinned down to 200 μm, the onset of microdischarge was not observed for voltages up to 1000 V.

3.4. Irradiation

Selected samples from batch #1 were irradiated with 70-MeV protons generated from the AVF cyclotron at CYRIC, Japan [18]. A batch of samples was irradiated to a fluence of 5×10^{12}, 1×10^{13}, 1×10^{14}, 1×10^{15}, or 1×10^{16} n_{eq}/cm^2 separately, stacked in an area of ~8 cm × ~2 cm on an irradiation board. Owing to the high current of the cyclotron, 1.5 h was required to reach fluence values as high as 10^{15} n_{eq}/cm^2 and approximately 8 h was required to reach 10^{16} n_{eq}/cm^2, while the beam current was limited to 800 nA.

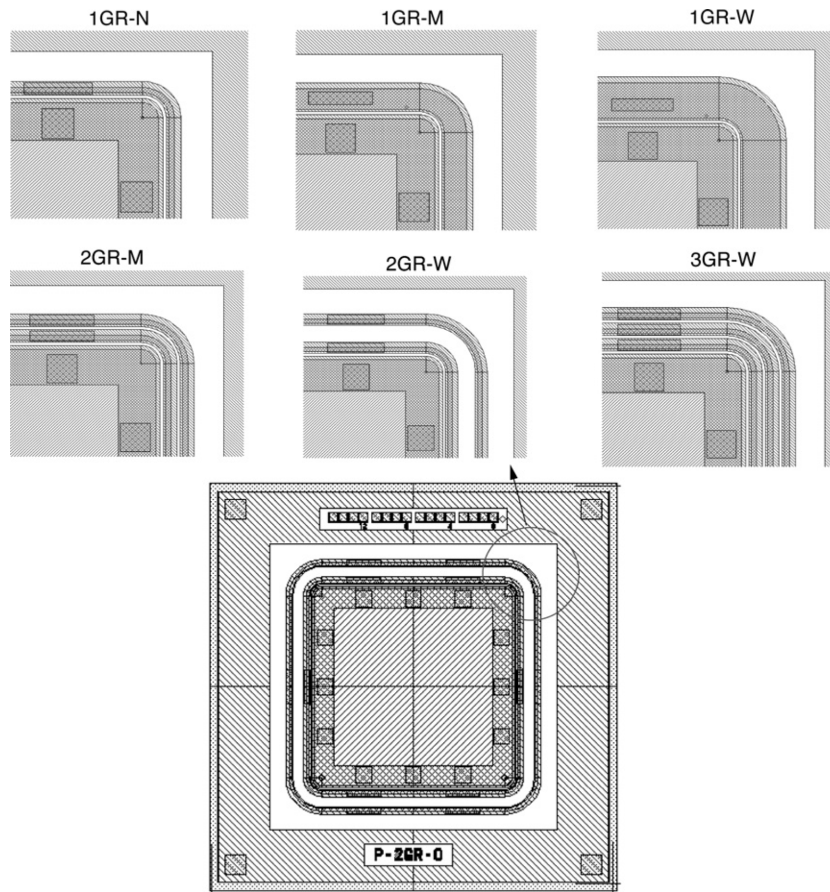

Fig. 5. Diodes with multiple guard rings with both varying number of guard rings and widths.

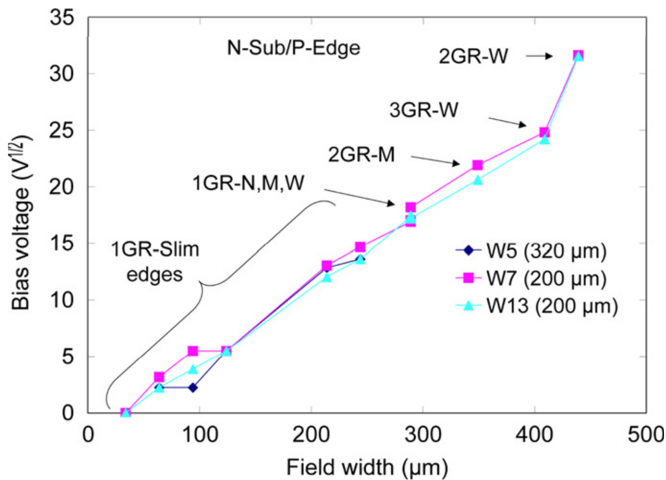

Fig. 6. Square root of bias voltage as observed at the strong increase of leakage current as a function of 'field width' in the n-bulk material with a p+ edge implantation.

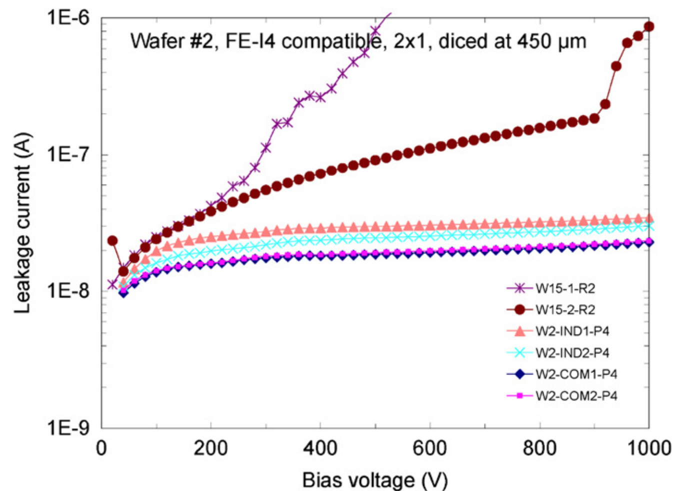

Fig. 7. Typical leakage current-bias voltage behavior of FE-14 double-chip compatible n-in-p pixel sensors; 4-to-1 PT, common (COM-P4) and individual (IND-P4) p-stop with 4×10^{12} ions/cm^2 and p-spray (R2) with 2×10^{12} ions/cm^2, diced along the longitudinal edge at 450 μm.

These series of measurement and their analysis are still ongoing and the results will be reported elsewhere.

4. Bump bonding of pixel sensors at HPK

The bump bonding technology for developing 'hybrid' pixel modules was verified with dummy and real chips. The dummy chips with aluminum patterns produce a daisy chain that passes through all bump-bonding pads. A probe pad was made in a loop of every two rows of pixel pads and cumulative and differential resistances were measured. HPK has experimented with two different types of solder bumps, lead (PbSn) and lead-free (SnAg), and has been optimizing the fabrication process.

4.1. PbSn solder bump bonding

One of the issues with solder bump bonding is the 'under bump metallization' (UBM), which is done either by electroplating or electroless-plating. On the first dummy chips, electroplating UBM and PbSn solder bump deposition were applied at IZM [19]. The UBM and PbSn solder deposition developed at IZM not only ensure that the PbSn solder bumps are compatible with FE-I3 chips with the solder bumps by IZM, but also are well developed processes, which were carried out at high yield in the ATLAS pixel modules.

The flip-chip assembly was carried out at HPK. A number of dummy chips were joined (bump-bonded) to make flip-chip (FC) modules: FE-I3 or FE-I4 single-chip or quad-chip compatible FCs. A typical profile of the daisy chain resistance in the case of FE-I4 single-chip dummy FCs is shown in Fig. 8 (a), where it is clearly seen that no open or little, if not none, shorted bumps exist, while the resistance is equal to $\sim 0.14\,\Omega$ per bump. Subsequently, one of the sample FCs underwent thermal cycling (10 times) between -30 and $+50\,^{\circ}$C with a ramp-up/down time of $\sim$30 min. Still, no opening of the bump bonds was observed.

Further FC samples were fabricated by HPK by applying electroless-plating UBM on dummy and pixel sensors as a low-cost alternative to electroplating. Peel testing of the FC samples of dummy chips revealed $\sim$50% of fractures in the solder bumps and $\sim$50% at the boundary between UBM and the chips, which was an evidence of uniform mechanical strength over the bump structures.

A few FE-I3 single-chip compatible real n-in-p pixel sensors with the electroless-plating UBM were bump-bonded with the real FE-I3 chips and evaluated with the use of a test beam. A preliminary result showed that a good tracking efficiency of $\sim$99% over the full sensor area was obtained, which means that the bump yield was $\sim$100% [20].

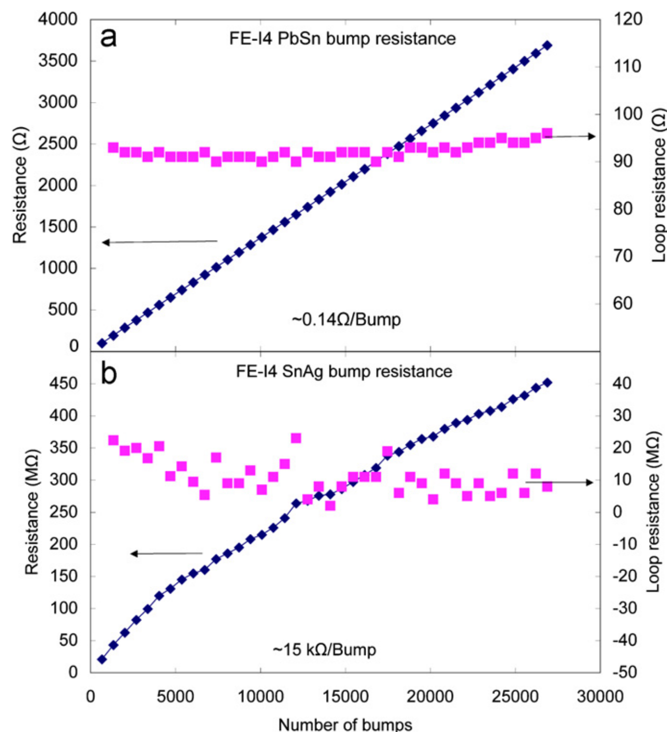

Fig. 8. Typical cumulative (diamonds, left vertical axis) and loop resistance of two rows (squares, right vertical axis) of a daisy chain of bump-bonded dummy chips: (a) with PbSn solder bumps and (b) with SnAg solder bumps.

4.2. AgSn solder bump bonding

As the electronics industry is moving towards lead-free solders, HPK also has fabricated FC samples, with AgSn solder bumps and electroless-plating UBM, both of which were created by HPK. The peel strength was found to be satisfactorily high and fractures were $\sim$50% in solder bumps and $\sim$50% at the boundary. The typical profile of the daisy chain resistance for a FE-I4 single-chip compatible dummy FC is shown in Fig. 8 (b). No opening or little shortening of the solder bumps was observed, but the resistance varied and reached such high values as $\sim 15\,\mathrm{k}\Omega$ per solder bump. The resistance was found to decrease to $<1\,\Omega$ per bump once a voltage of a few volts was applied to the daisy chain. This result implies the existence of a thin insulating layer, whose removal is currently being investigated.

4.3. Bumpless bonding at HPK

In the search for further low-cost bump bonding technology for future use, we are looking into 'bumpless' bonding, particularly the development of a 'thermal compression' technique allowing an electrode of gold or copper to be fused while being compressed at a temperature of 100–200 °C. It should be noted that the chip-to-wafer bonding is of greater value than wafer-to-wafer bonding because of the difference in the wafer size and more importantly the difference in yield for readout chips and pixel sensors. The technology will be evaluated when it becomes available in the near future.

5. Summary

In our attempt to develop a state-of-the-art n-in-p silicon microstrip sensor suitable for very high radiation environments, e.g., under conditions of a fluence of $10^{16}\,\mathrm{n_{eq}/cm^2}$ that is expected near the collision point in the upgraded LHC, we fabricated n-in-p pixel sensors in two batches of different mask sets: batch #1 mainly for the pixel sensors that was compatible with the pixel readout frontend chip called FE-I3 of ATLAS pixel detector, and batch #2 for FE-I3 and FE-I4 compatible sensors, along with small diodes used to evaluate the effects of the edge width and the guard rings.

Tests on the effects of the edge width and the guard rings showed that the strong increase of leakage current was attributed to the edge current when the lateral depletion zone reaches the dicing edge and the lateral depletion along the surface of silicon wafer was correlated with the 'field' width. For both p- and n-bulk wafers used in this study, the strong increase of leakage current was observed at a voltage of 1000 V when the total edge width was equal to $\sim 400\,\mu$m. Pixel sensors diced at $450\,\mu$m could successfully maintain a bias voltage of 1000 V.

Hybrid flip-chip pixel modules were fabricated with dummy and real chips that were bump-bonded at HPK. The lead (PbSn) solder bump bonding was successful. The real FE-I3 single-chip flip-chip modules were tested in a test beam successfully. Lead-free (SnAg) solder bumps were created with relatively high resistance, possibly due to the formation of a thin insulating layer, whose removal is currently under investigation.

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