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# Radiation hardness of silicon-on-insulator pixel devices

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ABSTRACT

Silicon-on-Insulator (SOI) CMOS is an attractive technology because of pixel sensor applications for its inherent advantages such as superior isolation of each FET by the surrounding insulator. We have been developing SOI pixel devices since 2005 using the FD-SOI technology and noticed that the insulator layers impose significant sensitivity to the total ionization dose (TID) effect. Research activities in the last ten years to improve radiation hardness are reviewed, such as introduction of buried wells and double SOI wafers.

## 1. Introduction and first evaluation results

Pixel devices based on SOI technology are being developed by the research group (SOIPIX group) organized in 2005 when KEK started the Detector Technology Project. We adopt the SOI handle wafer as the sensor material and the generated signal is fed to the top SOI readout electronics [1]; thus, monolithic pixel devices can be fabricated. As we employ the SOI wafers fabricated by the Soitec SmartCut™ technology, we can choose the wafer resistivity so that fully-depleted monolithic sensors are realized. Commercial 0.15-μm FD-SOI CMOS technology by then OKI Electric Company was available until 2011; then 0.20-μm FD-SOI CMOS by Lapis Semiconductor has been investigated. Several technological improvements have been the keys to successfully adopt SOI to pixel devices, which is detailed in [2] and [3].

The superior feature of SOI pixel devices owe much to the superior isolation of individual FETs achieved by surrounding $SiO_2$ insulator, which reduces the leakage current and makes the sensor immune against single event effects as the active layer thickness is substantially reduced, to 40 nm for FD-SOI. At the same time, FETs fully enclosed in insulator become sensitive to the hole accumulation in the insulator caused by the total ionization dose (TID) effect [4].

Evaluation of the TID effects has been one of major activities in this research. The target TID tolerance in applications in high-energy experiments, for example, is 1 kGy annually for the ILC (International Linear Collider) vertex tracker [5] or 0.53 MGy in lifetime at the outermost pixel layer for the High-Luminosity Large-Hadron Collider ATLAS experiment [6]. The study was carried out mainly using the dedicated Test-Element Group (TEG) composed of various types of FETs, i.e., TrTEGs [7]. First evaluations of the radiation hardness to TID damages were carried out for $^{60}$Co $\gamma$'s and 70 MeV protons [7,8]. As shown in Fig. 1 [8], substantial threshold shifts were recognized. The degradation by proton irradiation was identified to be similar to that of the TID by $^{60}$Co $\gamma$'s if the proton fluence is expressed in terms of the ionization dose. A crew to survive with such devices was shown that the threshold shifts caused by positive charges are compensable by applying negative voltage to the back of the substrate, typically −15 to −50 V at 1 MGy depending on the FET type, NMOS and PMOS through 350 μm thick substrate.

Such a significant effect compared to conventional CMOS FETs can be attributed to the insulator surrounding the FETs. Both the gate oxide (GOX) of 5 nm thickness and the buried oxide (BOX) of 200 nm thickness contribute to the TID effect. The trapped hole density and induced threshold voltage shift are calculated from the PMOS irradiation data; the method is detailed in [3]. According to the results shown in Fig. 2, the trapped hole density is larger in the BOX by a factor of 10 above 10 kGy, and the threshold voltage shift reaches approximately 0.3 V by the BOX charge and 0.04 V by the GOX charge at 100 kGy.

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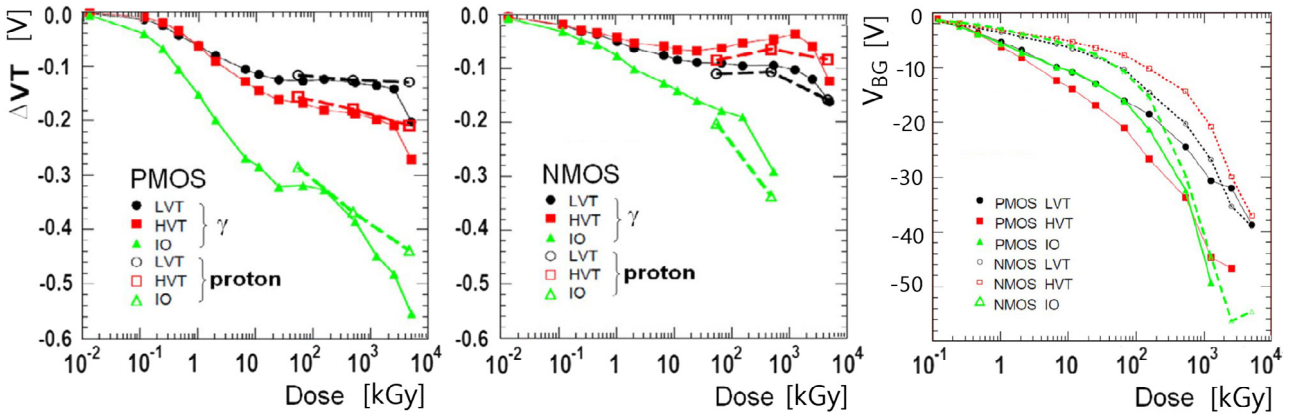


**Fig. 1.** Threshold voltage shifts of (left) PMOS and (middle) NMOS low-threshold (LVT) and normal threshold (HVT) core and IO FETs as a function of dose. The samples irradiated with $^{60}$Co $\gamma$'s and 70 MeV protons are compared. (right) The voltages applied to the backside of the substrate required to compensate the threshold voltage shifts [8].

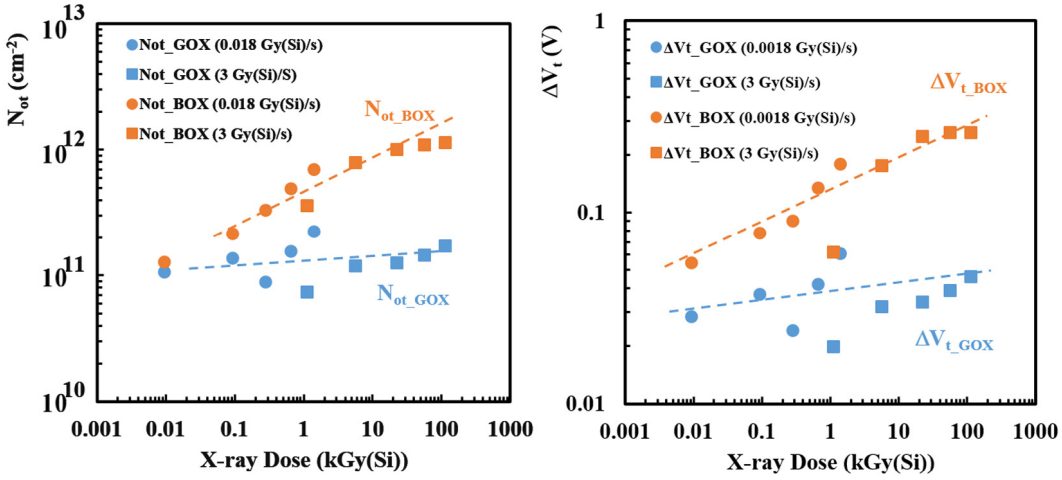


**Fig. 2.** (left) Trapped hole density in and (right) threshold voltage shift caused by the BOX and GOX calculated for PMOS FETs as a function of the dose. The data corresponding to the two dose rates are combined.

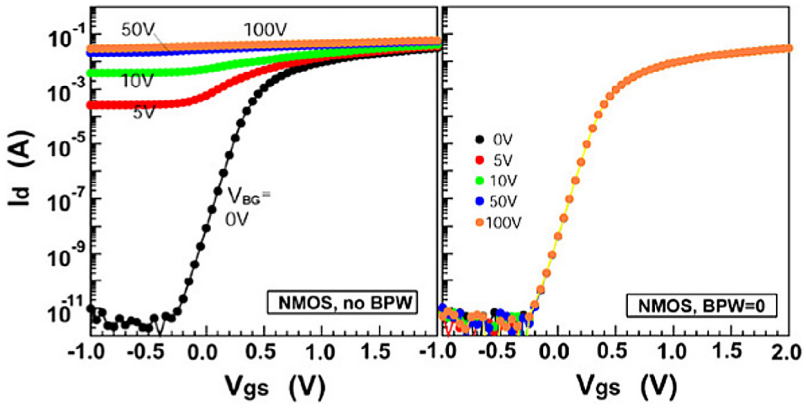


**Fig. 3.** Id-Vg curves of NMOS FET samples irradiated to $1.3 \times 10^{12}$ 1-MeV $n_{eq}$ cm$^{-2}$ measured for varied voltages applied to the backside. (left) Sample with no BPW, and (right) sample with BPW. The BPW tied to the ground eliminates the back-gate effect [9].

## 2. Buried well

The buried wells are lightly doped layers underneath the BOX, with p-type doping (BPW) for n-type substrate and vice versa. The buried well acting as a shield layer to the top circuit successfully eliminates the back-gate effect. Radiation hardness was successfully demonstrated to proton irradiation up to a fluence of $1.3 \times 10^{12}$ n/cm$^2$, as shown in Fig. 3 [9]. The potential of the buried well could be adjusted for the TID compensation, but it is often tied to the pixel node shaping the electric field for better charge collection. In addition, the back-gate effect suppression was found degraded for higher proton fluence. Therefore, it was highly important to have an additional independent control of the potential underneath the SOI circuitry.

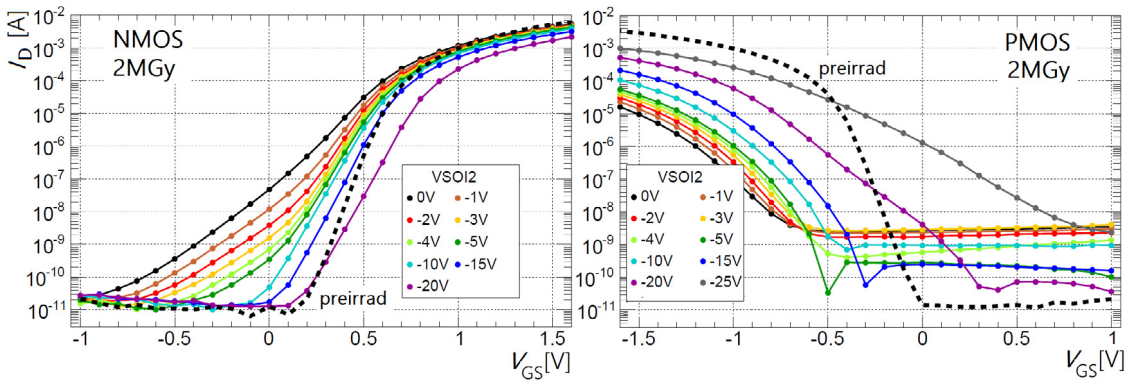


**Fig. 4.** Id-Vg curves of (left) NMOS and (right) PMOS irradiated to 2 MGy for various settings of the SOI2 voltages. The curve for pre-irradiation is shown in broken lines.

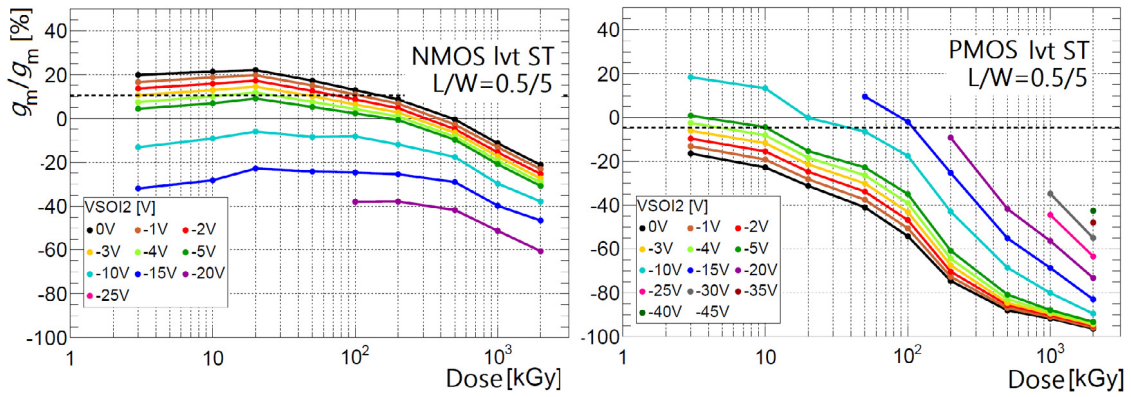


**Fig. 5.** Relative evolution of $g_m$ as a function of dose for (left) NMOS and (right) PMOS FET. The curves are for different settings of SOI2 voltages.

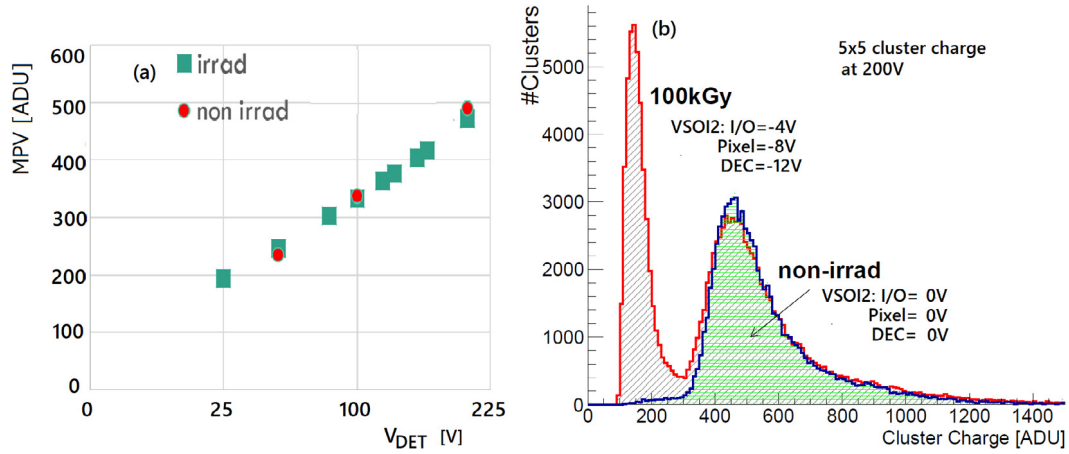


**Fig. 6.** (a) Most probable ADC values to 120-GeV protons compared between non-irradiated and 100 kGy irradiated FPIX2 of 300 μm thickness [13]. The horizontal scale is linear in $\sqrt{V_{DET}}$. (b) Charge distributions at 200 V bias are compared between non-irradiated (darker histogram) and 100 kGy irradiated (lightly shaded histogram) samples. The VSOI2 settings are as shown in the plot.

## 3. Double SOI with original LDD profile

Double SOI (DSOI) is the ultimate innovation to address these problems. The DSOI wafer is fabricated by repeating the Soitex SmartCut™ process twice. The two BOX layers are each 145 nm thick and the middle Si layer (SOI2) is 80 nm thick, first fabricated by Soitec with n-type Cz of 0.6 kΩ cm handle wafer resistivity, and then by Shin-etsu Chemical with low-oxygen n-type Cz (1 kΩ cm). The latest fabrication technique uses DSOI of p-type FZ of 5 kΩ cm resistivity. The middle SOI silicon was changed to n-type to reduce the sheet resistance for negative voltages applied, which is required for TID compensation.

Systematic and detailed compensation studies were carried out [10,11]. Fig. 4 shows a comparison of the FET Id-Vg curve before (broken lines) and after 2 MGy (black solid) irradiation for NMOS and PMOS FETs. Also shown are evolution of the Id-Vg curves by changing the voltage to SOI2, VSOI2. As the curve returns beyond the pre-irradiation threshold point, we can find the VSOI2 to be compensated, although the Id-Vg characteristics is not identical to the pre-irradiation case, especially for PMOS. Furthermore, substantial degradation is recognized

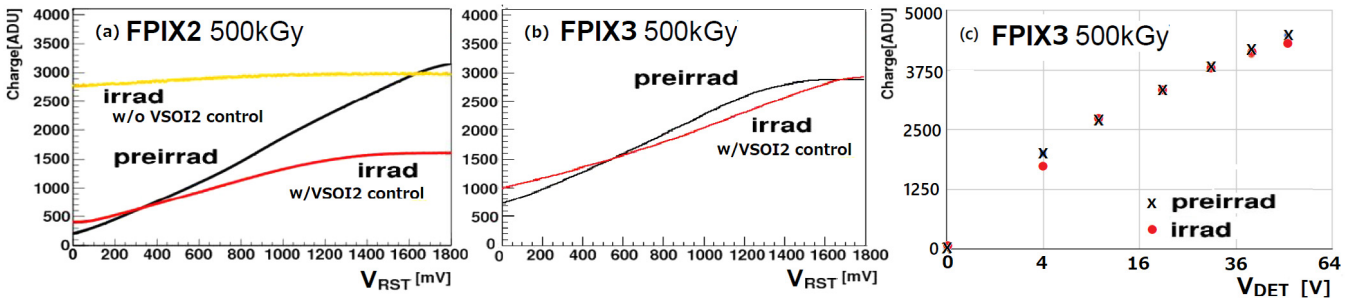


**Fig. 7.** Response to reset voltages of (left) FPIX2 and (right) FPIX3, compared between non-irradiated and 500 kGy irradiated samples. (c) Response to IR laser of 500 kGy irradiated FPIX3 as a function of the detector bias.

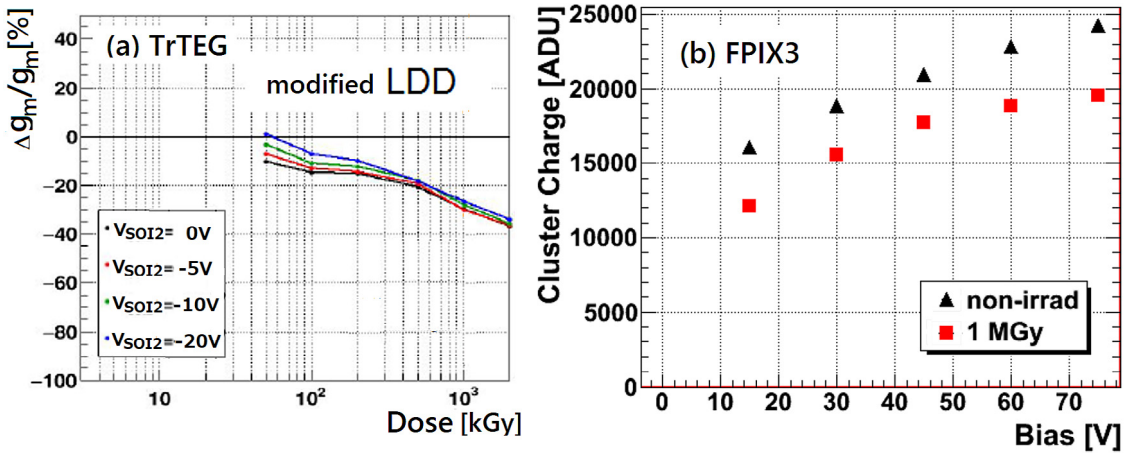


**Fig. 8.** (a) Degradation of trans-conductance as a function of dose for LDD modified TrTEG. (b) Response to IR laser as a function of bias voltage of FPIX3 irradiated to 1 MGy compared with non-irradiated sample.

in the PMOS trans-conductance $g_m$ as shown in Fig. 5; which shows that the trans-conductance is degraded to 10% at 1 MGy and recovers only modestly with VSOI2.

At this stage, however, it seems that the TID effect should be manageable up to ~100 kGy, which is well beyond the target dose to design the sensor for the ILC [5]. Then, demonstrator pixel sensors for TID compensation were fabricated: INTPIXh2 and FPIX2. INTPIXh2 is the first device with VSOI2 control, which successfully demonstrated almost full response recovery examined using IR laser after 100 kGy irradiation [12]. FPIX2 contains three VSOI2 controls for the pixel, decoder and IO regions individually, to take into account the TID difference between IO and core FETs. Because a PMOS-FET in the pixel region is the most sensitive, PMOS/NMOS difference can also be partially taken into account. The response to 120-GeV protons was examined for FPIX2 irradiated to 100 kGy [13]. As shown in Fig. 6, the most probable values are maintained identical to those of the non-irradiated sample by applying VSOI of −4 V to the IO, −12 V to the decorder, and −8 V to the pixel region. The noise level slightly increased from 1.8 ± 0.1 ADU to 5.4 ± 0.5 ADU measured at room temperature, which resulted in larger pedestal tail contribution observed below 300 ADU. This, however, can be eliminated by increasing the cluster seed (100 ADU in the figure) without loosing the efficiency.

## 4. Double SOI with modified LDD profile

The reason for substantial degradation in $g_m$ above 100 kGy was understood [14] and attributed to the fact that the LDD (Lightly Doped Drain) dose profile originally adopted was not optimum in view of the TID. The hole accumulated in the PMOS sidewall affects the lightly doped region underneath such that the doping concentration is not high enough to control the channel region, effectively enlarging the gate length with dose.

FPIX3 was fabricated with modified LDD profile, the LDD concentration increased by several times without changing other conditions, and with five VSOI2 controls; PMOS/NMOS in pixel, PMOS/NMOS in decorder and one for the IO region. As shown in Fig. 7, the reset voltage response (DC testing of the amplifier) is improved significantly from FPIX2 to FPIX3 irradiated to 500 kGy. The response to IR laser also verifies that FPIX3 is fully operational at 500 kGy irradiation.

FPIX3 irradiated to 1 MGy showed noticeable response degradation. In Fig. 8, the degradation of the trans-conductance is plotted for PMOS with modified LDD profile as a function of TID for various VSOI2 settings, which is to be compared with Fig. 5 with original LDD concentration. At 1 MGy, $g_m$ is reduced by 30%, which indicates substantial improvement by modification, but the dependence on VSOI2 became weaker. The $g_m$ reduction affects the signal amplification leading to noticeable degradation in the charge amplification as evident from the response to IR laser. However, as FPIX3 irradiated to 1 MGy exhibits a wide response region, the device should still be usable for such as particle tracking.

## 5. Summary

Research activity to adopt SOI technology to pixel devices has been conducted aiming at improving the radiation hardness as substantial degradation was observed originally even at the order of 100 Gy irradiation. The TID sensitivity of SOI pixel devices has been reduced substantially over the last ten years by introducing double SOI wafers. After optimizing the LDD profile, FPIX3 irradiated to 500 kGy showed a response equivalent to non-irradiated samples. At 1 MGy, although the response is reduced, FPIX3 showed a wide response range, indicating that it is adaptable for particle tracking.

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