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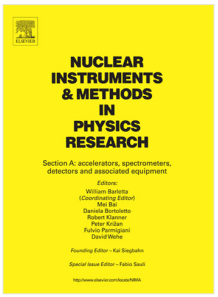

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Development of a monolithic pixel sensor based on SOI technology for the ILC vertex detector

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Abstract

SOI detector SOFIST is a pixel sensor optimized for the International Linear Collider vertex detector. SOFIST stores both position and timing information of charged particles. Our aim is to achieve 3 μm single-point resolution with a 20 $\times$ 20 μm^2 pixel. The first prototype sensor SOFIST Ver.1 was evaluated with a 120 GeV proton beam at the FermiLab Test Beam Facility. The position resolution was about 1.3 μm. We are currently evaluating the next version of sensor, SOFIST Ver.2, which has an in-pixel comparator and timestamp.

Keywords: SOI detector, Vertex detector, ILC

1. Introduction

Silicon-on-Insulator (SOI) technology integrates both silicon sensor and readout electronics in the same wafer [1]. Pixel detectors based on the SOI technology have several advantages compared with conventional hybrid detectors which are used for high energy physics experiments. The SOI detector realizes a low material budget, small pixel size, and low detector capacitance owing to the monolithic structure without bump-bonding. In addition, the detector employs

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a double SOI structure to improve radiation tolerance and to reduce cross talk between circuits and sensors (Figure 1). The double SOI wafer has an additional silicon layer for compensating the effect caused by the accumulation of holes in the oxide layer [2].

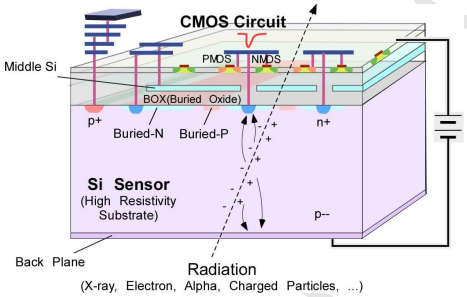

Figure 1: Structure of the double SOI pixel sensor. The additional silicon layer is in the middle of the buried oxide layer.

We are developing a new SOI pixel sensor for the vertex detector of the International Linear Collider (ILC) experiment. The ILC requires a new vertex detector system with high spatial resolution in order to identify the decay vertex of short-life-time particles for the precise measurement of Higgs boson and the search for physics beyond the Standard Model. We are currently designing an SOI pixel sensor, SOi sensor for FIne measurement of Space and Time (SOFIST), which has a pixel circuit with high position resolution and fine time resolution.

In this paper, we report the development and evaluation results of the SOFIST prototype sensors.

2. SOI sensor for ILC

The overview of the SOFIST sensor is shown in Figure 2. The following are requirements for the SOFIST development [3].

- Single point resolution : 3 μm
- Identification of 1300 bunches in ILC beam collisions every 554 ns

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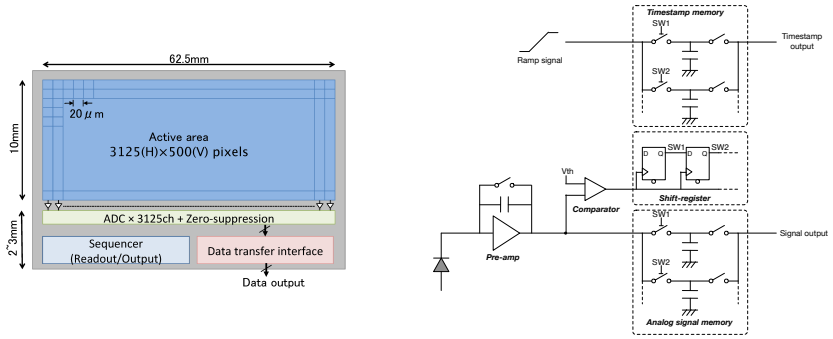

Figure 2: SOFIST chip overview (left panel) and pixel architecture (right panel). The sensor chip has 500 × 3,125 pixels. The column-parallel ADC circuits are arranged along the longitudinal direction of the sensor chip.

The pixel circuit of the SOFIST has an area of 20 × 20 μm^2. For each pixel, the signal amplitude and timing information are stored in corresponding memories when the signal amplitude is higher than the threshold of the comparator. The timing information is used for the hit bunch identification. The timestamp memory holds the voltage level of the ramping signal. The ramp voltage is proportional to the integration time and provided globally to all pixels in a chip. This timestamp circuit records the hit timing as the ramp voltage. In order to handle possible multiple hits during the signal accumulation, the pixel has multiple sets of analog signal memories and timestamps. It is necessary to optimize the implementation of these functions in a small pixel area. We are prototyping step sensors for realizing this pixel circuit .

3. SOFIST Ver.1

The prototype chips were fabricated with the 0.2 μm Fully Depleted Silicon-on-Insulator (FD-SOI) CMOS process of Lapis semiconductor [4]. The first chip is called SOFIST Ver.1. It has 50 × 50 pixels with a pitch of 20 μm (Figure 3). The sensor thickness is 500 μm. Each pixel circuit has a pre-amplifier and memory capacitors. The pre-amplifier is a charge sensitive amplifier with a common-source stage and feedback capacitance. The sensor chip also has 8-bit

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Wilkinson-type ADC circuits of 50 channels.

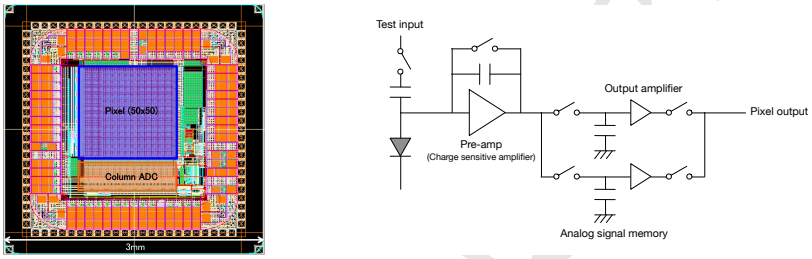

Figure 3: Chip overview (left panel) and pixel schematic (right panel) of SOFIST Ver.1. The sensor chip has 50 × 50 pixels.

The Ver.1 sensor was evaluated with a 120 GeV proton beam at the FermiLab Test Beam Facility [5]. The detector setup consists of two SOFIST Ver.1 and four FPIX, SOI Fine PIXel detector (Figure 5). The FPIX also acts as the SOI detector and has small pixels with a pitch of 8 μm [6]. The FPIX sensors were used as the tracking detector for evaluating the SOFIST position resolution.

Since the collected charge signal is proportional to the depletion thickness, we measured the backplane bias dependence of the SOFIST signal (Figure 4). The SOFIST signal was saturated about -80 V, so the sensor layer of 500 μm was fully depleted at this voltage.

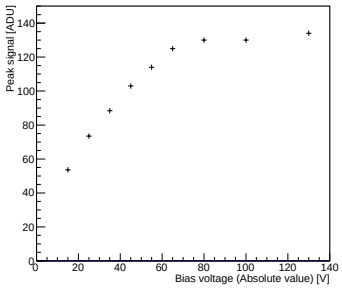

Figure 4: The back plane bias dependence of the SOFIST signal. The bias voltage was applied from -15 to -130 V. The signal saturation indicates full depletion of the sensor layer.

The SOFIST sensor data were taken with backplane biases of -130 and -15 V, which correspond to the sensor depletion thicknesses of 500 and 200 μm,

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respectively. The charge signal was digitized by 12-bit ADC on the readout board. The hit signal was reconstructed by clustering 5 × 5 pixels around the hit pixel. The hit position on the SOFIST chip was calculated from the weighted center of the cluster signal.

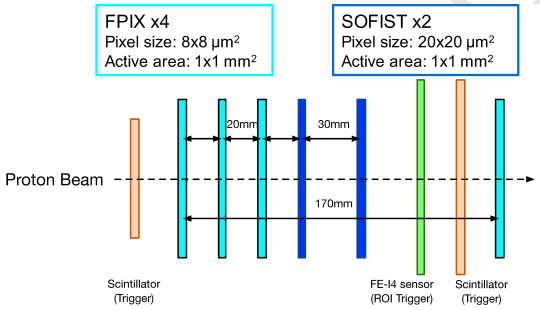

Figure 5: Detector setup for the beam test. The trigger signal was generated by a scintillator and an ATLAS pixel detector with an FE-I4 readout chip.

We analyzed the position resolution by using the particle tracks. We extracted the track candidates from the hits of four FPIX sensors. There were some spurious hit combinations due to the long integration time of FPIX. The track with minimum chi-square to the straight line was chosen for the analysis. We analyzed the residual of the hit position of the SOFIST to the reconstructed track. Figures 6 and 7 show the residual distributions of X (horizontal) and Y (vertical) directions at 500 μm and 200 μm depletion thickness, respectively. The standard deviation of the residual distribution was evaluated as the position resolution. We obtained position resolutions of 1.37 in X direction and 1.35 μm in Y direction at a depletion thickness of 500 μm. The residuals were still narrow at a depletion thickness of 200 μm, and the position resolution is 1.33 μm in X direction and 1.32 μm in Y direction. The measured residual is the sum of the squares of the intrinsic resolution of SOFIST Ver.1 and the track uncertainty. The track uncertainty is expressed in terms of the FPIX resolution and the geometrical position of the SOFIST. The FPIX is shown to have an intrinsic resolution of about 0.65 μm [6] and the track uncertainty on the SOFIST

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sensor becomes about 0.65 μm. The SOFIST intrinsic resolution was extracted about 1.2 μm.

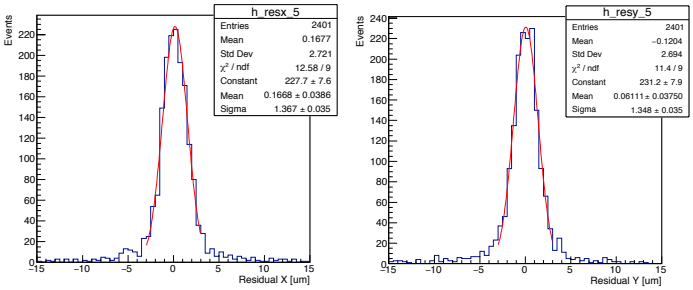

Figure 6: Residual distributions of X (left panel) and Y (right panel) at 500 μm depletion.

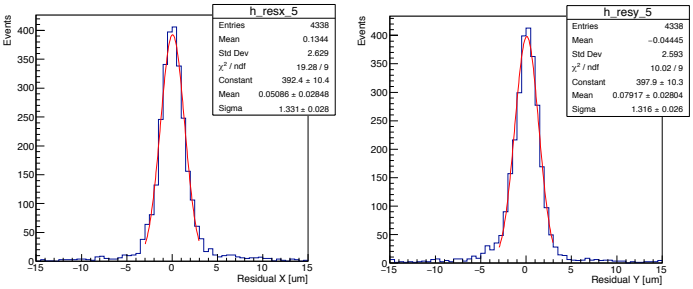

Figure 7: Residual distributions of X (left panel) and Y (right panel) at 200 μm depletion.

4. SOFIST Ver.2

Figure 8 shows the SOFIST Ver.2 sensor chip. The sensor has 80 × 64 pixels with a pitch of 25 μm. Since ILC detector requires the sensor thickness less than 100 μm for reducing multiple scattering effect, the Ver.2 sensor layer is thinned to 75 μm by grinding the back side of the chip. The Ver.2 pixel has a comparator circuit for discriminating the signal exceeding the threshold voltage. We have designed two types of pixel circuits, namely Analog signal pixel and Timestamp pixel (Figure 9).

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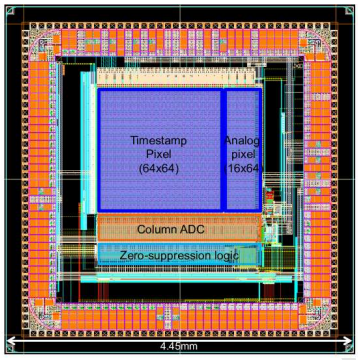

Figure 8: Chip overview of SOFIST Ver.2. The sensor chip has 80 × 64 pixels, column-parallel ADC circuits, and digital Zero-suppression logic.

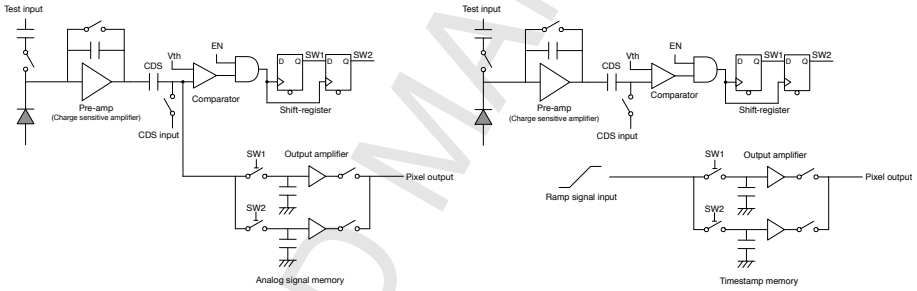

Figure 9: The Ver.2 chip has Analog signal pixel (left panel) and Timestamp pixel (right panel).The Analog signal pixel stores the signal amplitude of the pre-amplifier output. The Timestamp pixel stores the ramp voltage for the analog time-stamp.

We will verify in-pixel timestamp function and the degradation of the position resolution. The pixel circuit and size will be optimized for satisfying both the timestamp and the resolution based on the evaluation of the Ver.2 sensor. The sensor production has been completed. We are currently evaluating the Ver.2 pixel circuits. Figure 10 shows the responses of Analog signal and Timestamp pixel when a test pulse is inputted. The charge signal is input to the sensor node of the pixel. The pixel memory holds the signal voltage when the input signal exceeds the threshold level. Figure 11 shows the pixel timestamp signal with inputting test pulse at specific timings. The ramp signal was generated with 1 mV per microsecond and delivered to each pixel. The slope of measured

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timestamp became about 0.96 mV per microsecond. We have confirmed the functionality of Ver.2 pixel circuits.

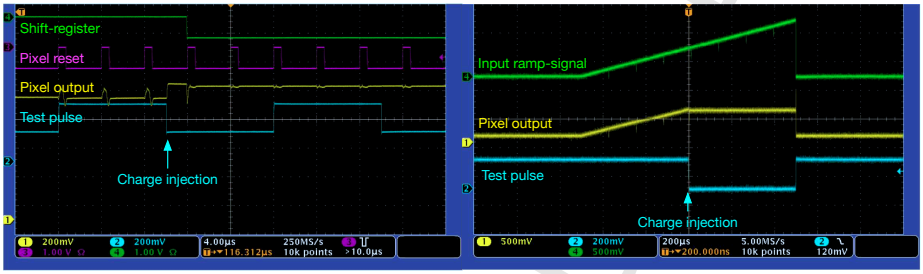

Figure 10: Output responses of Analog signal pixel (left panel) and Timestamp pixel (right panel) when the input signal is over the threshold. The pixel signal is reset every 4 μs (magenta line). The charge signal is injected at the falling edge of the test pulse (cyan line).

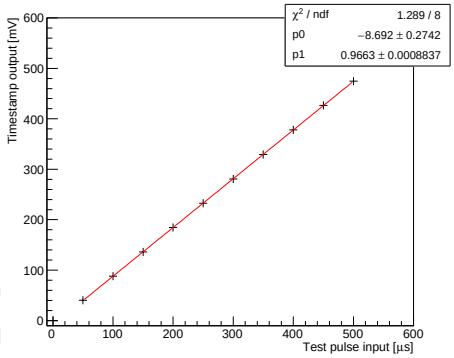

Figure 11: The readout signal of in-pixel timestamp with inputting test pulse. Horizontal and Vertical axis are the pulse input timing and the readout signal of the timestamp memory.

5. Conclusion and future prospect

We have developed two prototype chips for realizing a new SOI pixel sensor SOFIST optimized for the ILC vertex detector. SOFIST Ver.1 chip has a pixel area of 20 $\times$ 20 μm^2 and column parallel ADC circuits. We evaluated the position resolution with a 120 GeV proton beam at the Fermilab Test Beam Facility. We obtained a position distribution of about 1.3 μm at a depletion

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thickness of 200 μm. The SOFIST Ver.1 resolution meets the requirement for the ILC experiment. SOFIST Ver.2 chip has a pixel area of 25 $\times$ 25 μm^2. We designed an in-pixel comparator for storing the amplitude and timestamp of the hit signal. These pixel functions have been verified by inputting the test pulse. We are planning a beam test for Ver.2 sensor in February 2018. We are also developing next sensors, Ver.3 and Ver.4, with full SOFIST functionality. The pixel of Ver.3 sensor has both analog signal and timestamp memories within 30 $\times$ 30 μm^2. The Ver.4 sensor is to be processed with 3D stacking technology in order to shrink the pixel size [7]. These sensor chips will be delivered by spring 2018.

Acknowledgement

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References

[1] Y. Arai, T. Miyoshi, Y. Unno, T. Tsuboyama, S. Terada, Y. Ikegami, T. Kohriki, K. Tauchi, Y. Ikemoto, R. Ichimiya, et al., Developments of soi monolithic pixel detectors, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 623 (1) (2010) 186–188.

[2] K. Hara, Y. Arai, S. Honda, I. Kurachi, T. Tsuboyama, N. Tobita, T. Miyoshi, M. Asano, S. Mitsui, Initial characteristics and radiation damage compensation of double silicon-on-insulator pixel device, PoS (2015) 033.

ACCEPTED MANUSCRIPT

[3] H. Abramowicz, et al., The international linear collider technical design report—volume 4: detectors, arXiv preprint arXiv:1306.6329.

[4] M. Okihara, H. Kasai, N. Miura, N. Kuriyama, Y. Nagatomo, T. Hatsui, M. Omodani, T. Miyoshi, Y. Arai, Progress of fd-soi technology for monolithic pixel detectors, in: Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2012 IEEE, IEEE, 2012, pp. 471–474.

[5] Fermilab test beam facility, url: http://ftbf.fnal.gov.

[6] K. Hara, D. Sekigawa, S. Endo, W. Aoyagi, S. Honda, T. Tsuboyama, M. Yamada, S. Ono, M. Togawa, Y. Ikegmi, Y. Arai, I. Kurachi, T. Miyoshi, J. Haba, K. Hanagki, Fine-pixel detector fpix realizing sub-micron spatial resolution developed based on fd-soi technology, Springer Proceedings in Physics, Technology and Instrumentation in Particle Physics (TIPP2017).

[7] M. Motoyoshi, T. Miyoshi, M. Ikebec, Y. Arai, 3d integration technology for sensor application using less than 5m-pitch gold cone-bump connpdfection, Journal of Instrumentation 10 (03) (2015) C03004.

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