

# Results of early phase of series production of ATLAS SCT barrel hybrids and modules

Y.Ikegami<sup>a,\*</sup>, R.Apsimon<sup>b</sup>, L.Batchelor<sup>b</sup>, G.Beck<sup>c</sup>, A.Belymam<sup>c</sup>, R.Brenner<sup>c</sup>, A.Barr<sup>d</sup>, J.Carter<sup>d</sup>, A.Carter<sup>e</sup>, D.Charlton<sup>f</sup>, A.Ciocio<sup>g</sup>, O.Dorholt<sup>h</sup>, T.Ekelof<sup>c</sup>, L.Eklund<sup>c</sup>, K.Emoto<sup>j</sup>, V.Fadeyev<sup>g</sup>, B.Gallo<sup>f</sup>, M.Gibson<sup>b</sup>, M.Gilchriese<sup>g</sup>, M. Goodrick<sup>d</sup>, A.Grillo<sup>k</sup>, C.Haber<sup>g</sup>, K.Hara<sup>j</sup>, J. Hill<sup>d</sup>, T.Huse<sup>o</sup>, A.Ikeda<sup>l</sup>, A.Ito<sup>l</sup>, Y.Iwata<sup>m</sup>, P.Jovanovic<sup>f</sup>, Y.Kato<sup>j</sup>, T.Kawachi<sup>n</sup>, K.Kobayashi<sup>l</sup>, T.Kohriki<sup>a</sup>, T.Kondo<sup>a</sup>, M.Kurita<sup>l</sup>, S.McMahon<sup>b</sup>, M.Minagawa<sup>j</sup>, T.Miyamoto<sup>l</sup>, T.Morinaka<sup>l</sup>, M.Morrissey<sup>b</sup>, J.Morin<sup>e</sup>, J.Morris<sup>e</sup>, E.Mulder<sup>k</sup>, W.Murray<sup>b</sup>, K.Nagai<sup>c</sup>, I.Nakano<sup>l</sup>, T.Ohsugi<sup>m</sup>, M.Palmar<sup>d</sup>, P.Phillips<sup>b</sup>, D.Robinson<sup>d</sup>, F.Rosenbaum<sup>k</sup>, A.Seiden<sup>k</sup>, H.Sengoku<sup>j</sup>, S.Shimma<sup>j</sup>, N.Spencer<sup>k</sup>, S.Stapnes<sup>h</sup>, B.Stugu<sup>o</sup>, R.Takashima<sup>n</sup>, R.Tanaka<sup>l</sup>, S.Terada<sup>a</sup>, Y.Tomeda<sup>l</sup>, M.Tyndel<sup>b</sup>, Y.Unno<sup>a</sup>, J. Wilson<sup>f</sup>

<sup>a</sup> High Energy Accelerator Research Organisation (KEK), Oho 1-1, Tsukuba 305-0801, Japan

<sup>b</sup> Rutherford Appleton Laboratory, Chilton, Didcot, UK

<sup>c</sup> University of Uppsala, Uppsala, Sweden

<sup>d</sup> Department of Physics, University of Cambridge, Cambridge, UK

<sup>e</sup> Department of Physics, Queen Mary and Westfield College, University of London, London, UK

<sup>f</sup> School of Physics and Astronomy, University of Birmingham, Birmingham, UK

<sup>g</sup> Lawrence Berkeley Laboratory and University of California, Berkeley, CA., USA

<sup>h</sup> Department of Physics, University of Oslo, Oslo, Norway

<sup>j</sup> University of Tsukuba, Tsukuba, Japan

<sup>k</sup> Institute for Particle Physics, University of California, Santa Cruz, CA, USA

<sup>l</sup> Faculty of Science, Okayama University, Okayama, Japan

<sup>m</sup> Faculty of Science, Hiroshima University, Hiroshima, Japan

<sup>n</sup> Kyoto University of Education, Kyoto, Japan

<sup>o</sup> University of Bergen, Bergen, Norway

\* Corresponding author: ikegami@post.kek.jp

## Abstract

A status of early series production of the barrel hybrids and modules of the ATLAS Semiconductor Tracker (SCT) is reported. 120 hybrids (with ASIC's) and 98 modules were fabricated in Japan by the mid. August 2002 and gone through extensive quality assurance tests. Defective channels were found much less than 1% in hybrids and still less than 1% in modules. No increase of defective channels was observed, in hybrids after 100-hours burn-in at an elevated temperature, and in modules after thermal cycling and 24-hrs long-term test at the operation temperature of the experiment.

## I. INTRODUCTION

The ATLAS Semiconductor Tracker (SCT) [1] covers the region from 300 to 520 mm in radius from the beam line. It consists of the barrel part of 4 cylindrical layers in the central region and the forward part of 9 disks in each side. The total area of the SCT silicon micro strip sensors is 61 m<sup>2</sup>. The area is implemented with 4,088 detector units called "modules" which are stand-alone mechanical objects providing rigidity as well as electrical and thermal functionalities.

Total number of barrel SCT modules is 2,112 in the experiment. Close to 700 modules will be assembled in Japan including spares. Series production of modules was started in early 2002 in Japan, and other clusters, Nordic, UK, and US, are expected to follow soon.

## II. BARREL SCT MODULE

A picture of the module is shown in Figure 1. The module is made of four silicon microstrip sensors, a central baseboard, and hybrids wrapping around the upper and the lower sensors at the centre of the module. The hybrids are bridging over the sensor area with air-gap in between. This construction gives several characteristics. No material other than aluminium wire-bonds is touching the sensitive surface of the sensors. The heat of the ASIC's is not going into the sensors directly. The module has clean edges for overlapping. Major parameters of the module are listed in Table 1. Detailed description of the design and performance of the modules are given in references [2].

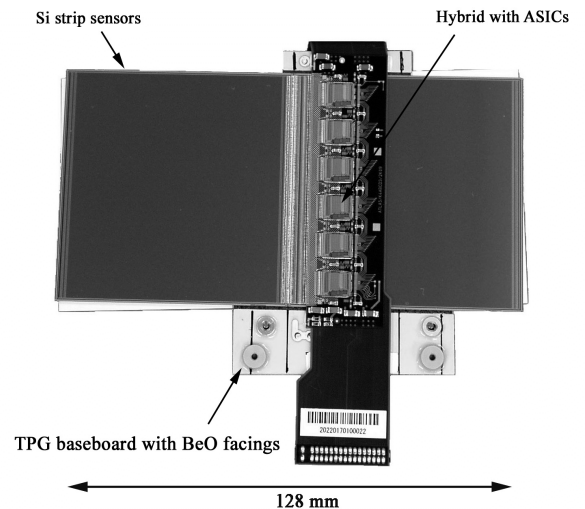


Figure 1: A picture of the barrel SCT module

Table 1: Major parameters of the ATLAS barrel SCT module

Number of sensors	2 in upper, 2 in lower
Total number of readout channels	1536 channels
Dimension of a strip sensor [mm]	63.96 x 63.56 x 0.285
Strip pitch / stereo angle	80 $\mu$ m / 40 mrad
Sensor operating temperature	< 0 °C, optimum -7 °C
Number of ABCD chips	6 in upper, 6 in lower
Hybrid power consumption	6W nom., 8.1 W max.
Thermal runaway heat flux in sensor	> 240 $\mu$ W/mm <sup>2</sup> at 0 °C
Thickness (sensor/module max.)	1.15 / 5.78 mm
Radiation length averaged	1.17 % Xo/module

### A. Silicon microstrip sensor

The module has four identical silicon microstrip sensors of single-sided, AC-coupled, p-strips on n-type wafer. Pairs of sensors are glued on the upper and the lower side of the central baseboard, being rotated by 40 mrad. to form a stereo angle. Strips of the pair of sensors are wire-bonded to form strips of 126 mm length. The sensor has 768 readout strips with a pitch of 80  $\mu$ m.

### B. Baseboard

The baseboard acts as a mechanical core, a thermal conductor to transfer the heat generated in the sensors to the cooling pipe, and a path for electrical high voltage (HV). The baseboard is made of thermalized pyrolytic graphite, TPG, (or VHCPG: Very High thermal Conductivity Pyrolytic Graphite). Its thermal conductivity is 1450 to 1850 W/m/K in plane and 6 W/m/K out of plane. The baseboard is encapsulated with 20  $\mu$ m thick epoxy. Each protruding end is covered with Beryllium-Oxide (BeO) facings for mechanical rigidity and thermal contact for hybrids [3]. Small openings are made in the surface of the baseboard, 4 in each side, for electrical HV connection to the rear side of the silicon sensors. The facing has precision washers providing a hole and a slot for precision module mounting and also gold-plated pads for HV connection to the baseboard.

### C. Hybrid

The hybrid is made of flexible circuit of copper/polyimide laminate. The entire section: connector, pigtail cable, upper hybrid, wrap-around cable, and lower hybrid, is a single-piece construction. The hybrids and the connector sections are 4 conductive-layer structure. The cable sections are 2 layers by etching out the top and bottom layers. Thickness of the hybrid section is 270  $\mu$ m and 150  $\mu$ m in the other sections.

Electrical connection across different layers is realised with either through-holes which drill through all 4 layers, or laser-cut via-holes which connect two layers, between the top (L1) and the second (L2) layer. The diameters of the through- and via- holes are 0.3 and 0.15 mm, respectively. The use of the laser-via makes the layout of traces freer and the width of the hybrid narrower, being 21 mm, which reduces the material of the hybrid. The wire-bonding pads are plated with nickel (3  $\mu$ m), a barrier metal, and a flash of gold (0.3  $\mu$ m). The bottom

side of the flexible circuit has openings for electrical contact to the carbon-carbon (CC) substrate. The electrical contacts are connected to the ASIC pads on the top surface with bunches of through-holes for solid electrical and thermal connection.

The hybrid sections of the flexible circuit are reinforced with a carbon-carbon substrate. The CC material is “uni-directional”. The Young’s modulus is as high as ceramics, in the fibre direction, that makes the ultrasonic wedge wire bonding possible even it is bridging over the sensor. The thermal conductivity is nearly twice that of copper, in the fibre direction, and providing a thermal path of the hybrids. The electrical conductivity provides additional electrical ground reinforcement.

The CC is machined to a thickness of 300  $\mu$ m at the bridging section and 800  $\mu$ m at the edges contacting the BeO facings. The surface of CC is coated with a polymer called parylene of a thickness of 10  $\mu$ m in order to prevent carbon fluffs coming off. The coated surface is roughened where adhesive is to be applied or removed where electrical connection is required, with high-power lasers.

The basic pitch of input pads of the readout ASIC is 48  $\mu$ m, while that of the silicon strip sensor is 80  $\mu$ m. In order to make parallel wire-bonding, a pitch-adapter (PA) is attached in front of the ASIC’s. The aluminium pads and traces are fabricated on a glass substrate with a deposition of a thickness of about 1  $\mu$ m.

All passive electrical components are of surface mount types of 1608 or 3216 with a length/width of 1.6/0.8 or 3.2/1.6 mm, respectively. All capacitors are of the X7R type which capacitance change is less than 5% for the temperature change between -20 and +40 °C. The resistors are of thin metal film with a 0.5% tolerance. Two thermistors are mounted to monitor the hybrid temperature.

### D. Readout ASIC

The readout ASIC, ABCD3TA, does amplification and shaping, discrimination, and buffering of the signals from 128 strips [4]. The gain of the amplifier is 50 mV/fC and the peaking time of uni-polar shaping is 20 nsec. The equivalent noise charges (ENC) with 12 cm strips are designed to be about 1500 electrons at room temperature initially and increase to about 1800 e, after 10 years of operation, due to radiation damage in the sensors and the ASIC’s.

In order to make the threshold, in charge, uniform, a 4-bit DAC is implemented in each channel by adjusting the offset of signals. The DAC is called “trim DAC” and its range is selectable from 60, 120, 180 and 240 mV to cover increased spreads of threshold due to radiation damage. Four calibration lines are equipped alternatively in channels. One line can injects charges into 32 channels simultaneously, in coincidence with strobe signals.

The threshold for hits in experiment is set to be 1 fC. The on-off hit information is sent to channel mask registers that block any bad or noisy channels, thus preventing them from increasing the data rate due to false hits. The hit information is then stored in 132 bit deep pipeline buffers until being accepted by Level 1 triggers.

### E. Data Acquisition (DAQ)

A software package, SCTDAQ, developed for reading out the ABCD chips [5], executes electrical tests on the hybrids and the modules for quality assurance (QA). It runs on a PC (Windows NT) and consists of a compiled Dynamic Link Library (DLL) and a set of ROOT [6] macros.

The PC is connected to a VME crate via VME-VXI interface [7]. A VME module, MuSTARD, reads out the ABCD buffers and a VME module, SLOG, sends commands and clock [8]. One set can handle six hybrids or modules simultaneously, together with three SCTLV modules for low voltage power supply [9] and three SCTHV modules for high voltage power supply for the modules [10]. There are two sets for hybrids and one set for modules at KEK in order to maintain a production rate of 10 modules or more in a week.

### III. HYBRID TESTS AND RESULTS

120 hybrids with ASIC's were assembled in Japan by the middle of August 2002. Two hybrids were found to have cracks in the glass pitch-adapters (PA), which were later identified to have occurred in packing the hybrids (without ASIC) for transportation. One hybrid was found to have bubbles in the epoxy gluing the pitch-adapter. These defective hybrids should have been rejected by visual inspection before stuffing ASIC's.

The ASIC's were delivered to the hybrid assembly site after screening [11]. After stuffing the ASIC's, a full set of electrical examinations called "Characterization Sequence" was performed that was consisted of examinations of, (a) bypass functionalities, (b) redundancy lines, (c) pipeline efficiencies, (d) strobe delays, (e) gains, offsets, and noises using 3 threshold points, (f) Trim-DAC tuning, (g) response curves, gains, offsets, and noises, using 10 threshold points and tuned Trim-DAC parameters, (h) noise occupancies, and (i) time-walks. A subset from (a) to (e) formed the "Confirmation Sequence" and provided a minimal set for ensuring the digital functionality and the analog performance. Characterization or Confirmation Sequence took about 50 min. or 20 min. per hybrid (12 ASIC's), respectively. The hybrid was mounted on a fixture during all electrical tests and set in an environmental chamber with a flow of dry nitrogen.

Out of the electrical tests, defects in ASIC's were classified. The channels that were defective and subsequently masked by the channel mask registers in front of the pipeline buffers were, completely inefficient (DEAD), always on (STUCK), or un-trimmable (UNTRIMMABLE) channels. These channels were eventually become dead by masking. The channels that had a bit error in the pipeline buffers or after and showed prevailing hits were STUCKCELL channels. This defect is severe because it produces unnecessary traffic. The ASIC's which had all 128 channels DEAD, STUCK, or UNTRIMMABLE, were classified as DEAD ASIC's. The ASIC's which had one or more STUCKCELL channels were classified as STUCKCELL ASIC's. Other classes of faulty ASIC's were found. ASIC's which had very large spread of gain in all channels, 30 to 70 mV/fC, were classified as "Large gain spread" ASIC's. ASIC's which threshold uniformity in all channels were worse than expected after trim tuning were classified as "Trim-DAC loading failed" ASIC's.

ASIC's which responses were faulty below a threshold because of negative offsets were classified as "Negative offset" ASIC's. ASIC's which had abnormal calibration line were classified as "Abnormal calib line" ASIC's. Figure 2 shows an example of such "Large gain spread" and "Trim-DAC loading failed" ASIC's.

Fifteen hybrids were found to have defective ASIC's. Four hybrids were come from a batch of "damaged ASIC's" which were identified to have occurred in dicing wafers and picking ASIC's. Excluding those hybrids made from the batch of "damaged ASIC's" and with inadequate PA's, 113 hybrids were remained. A breakdown of defective ASIC's is shown in Table 2. The defect rate of hybrids was 9.7%. The defect rate of ASIC's was 0.8% since there were 12 ASIC's in a hybrid. The defective ASIC's of the hybrids can be replaced later. By removing those "Large gain spread", "Trim-DAC loading failed", "Negative offset", and "Abnormal calib line" ASIC's in the ASIC screening, the defect rate of hybrids can be reduced to 3%. Since the number of the defective ASIC's is small, rejection of these ASIC's affects the yield of ASIC's minutely.

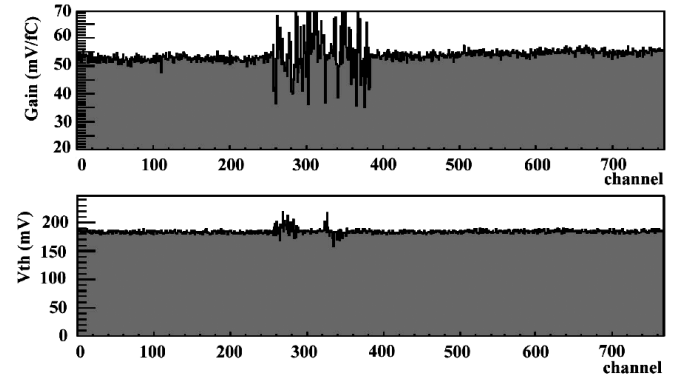


Figure 2: Example of "Large gain spread" (top plot) and "Trim-DAC loading failed" ASIC's (bottom plot). There are 6 ASIC's in a plot.

Table 2: Breakdown of defective ASIC's

Defective ASIC's	Hybrids	ASIC's	Channels
DEAD (most channels)	1	1	
STUCKCELL	2	2	3
Large gain spread	2	2	
Trim-DAC loading failed	2	2	
Negative offset	3	3	
Abnormal calib line	1	1	
Defect Rate	11 / 113 = 9.7%	11/113/12 = 0.8%	

Excluding those defective ASIC's in the above, the number of defective channels were found to be 1 DEAD, 6 STUCK, and 16 UNTRIMMABLE. Most of the un-trimmable channels were due to very high noises in the channels. The average number of dead channels per hybrid was 23 ch./ 102 hybrids = 0.2 ch./hybrid. The maximum number of dead channels was 6 ch./hybrid.

After initial electrical examination, two tests were performed in order to check the ASIC's and ASIC-hybrid

integrity further: (1) 80 to 100 hrs burn-in at an elevated temperature, and (2) 20 hrs long-term at the operation temperature in experiment. The elevated temperature was 37 °C at the thermistors of the hybrid, which was about 50 °C in the ASIC temperature. The operation temperature was 0 °C at the thermistors. The Characterization Sequences were executed before and after the above two tests and the Confirmation Sequences in every 6 hours during the later. There was no increase of defects after the burn-in and the long-term cold tests.

#### IV. MODULE TESTS AND RESULTS

A total of 98 modules were assembled in Japan by the middle of August 2002. Two modules were discarded because of mechanical damages in assembly: a sensor was cracked in one module and a BeO facing was cracked in the other. An area of wirebonds of one module was damaged in the handling for metrology. Slightly inadequate gluing of hybrids on the BeO facing was found in 8 modules. These latter 8 modules were electrically good and could be kept as spares.

The 95 modules were gone through mechanical and electrical QA examinations. The mechanical examinations were visual inspection, metrology, thermal cycle, and long-term cold tests. The electrical examinations were leakage current measurement as a function of bias voltage up to 500 V (I-V), and the Characterization or Confirmation Sequence. The sequence of the module QA flow was:

- (1) Initial test at manufacturing site: Visual inspection, Metrology, I-V and Characterization Sequence
- (2) Reception at KEK: Visual inspection, Metrology, I-V, and Confirmation Sequence
- (3) Thermal cycle test
- (4) Check after the thermal cycle test: Visual inspection, Metrology, I-V, and Confirmation Sequence
- (5) Long term cold test: Confirmation Sequence in every 6 hours
- (6) Final test: Visual inspection, Metrology, I-V, and Characterization Sequence

Mechanical and electrical integrity against the thermal stresses as expected in experiment was examined by cycling thermally between -25 and +40 °C for 10 times. The transition and holding time was 30 minutes each. Integrity and stability at the operation temperature were examined by keeping for 24 hrs at 0 °C at the thermistors. The modules were stored in a module box and set in an environmental chamber with a flow of dry nitrogen during the electrical tests.

In Metrology, the positions of the sensors and shape of the modules were surveyed with a 3-dimensional metrology machine [12]. One of the critical parameters that was difficult to achieve was the alignment of the upper and the lower sensors, called “midyf”, the deviation of centre of the upper pair relative to the centre of the upper and the lower pairs. Figure 3 shows the “midyf” in serial order. The tolerance for the “midyf” was  $\pm 5 \mu\text{m}$ . Four modules were out of tolerance in early phase. Together shown in the figure is the assembly parameter that controls the “midyf”. The parameter was set to  $-5 \mu\text{m}$  in that phase, which was later identified as mistake. The coincidence of the assembly parameter and the

measured “midyf” was good and the spread of the “midyf” around central values was well within the specification.

Behaviour of leakage current was measured for the bias voltage up to 500 V at a temperature of 15 °C. Figure 4 shows the I-V curves of 95 modules. Most of the modules draw little current, less than 400 nA, smoothly up to 500 V, which were consistent with the sum of four sensors used in the modules. Two modules showed breakdown (we call it “microdischarge”) below 350 V and 10 modules above 350 V. The former 2 modules were identified to have damages on the bonding pads that were made at the time of bonding repairing. The microdischarges above 350 V were accepted. In experiment, the bias voltages required are below 200 V initially, and after type inversion and growth of full depletion voltage due to radiation damage, the microdischarge will not occur for the voltages to deplete the sensors in 10 yrs of operation. This has been confirmed in irradiated sensors. Also, the increased currents decayed down to normal currents after applying the bias voltages, e.g., 500V, for hours, a characteristic of microdischarge.

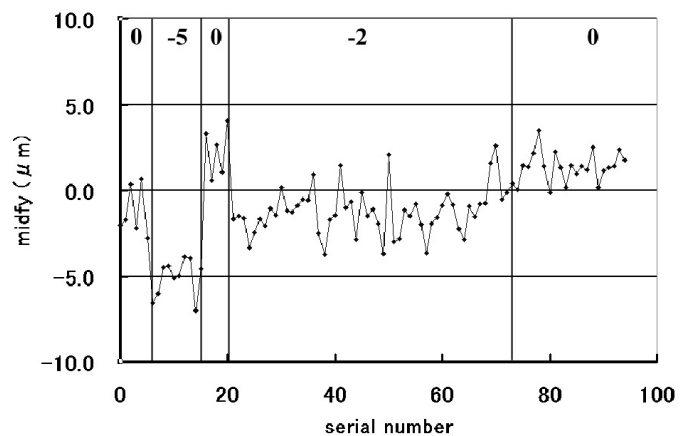


Figure 3: The measured upper-lower alignment “midyf” in serial order. The values of the assembly alignment parameter are also shown in the plot.

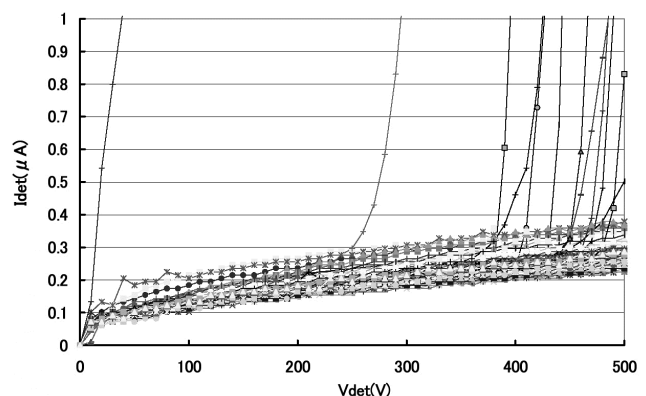


Figure 4: I-V measurement of the modules

Electrical examinations showed no increase of problematic ASIC’s or channels, in the module assembly, and in the thermal cycle and the long-term tests. There was no increase of DEAD, STUCK, or STUCKCELL channels, but there was increase of UNTRIMMABLE channels from 15 in the hybrids to 37 (the number after the thermal cycle and the long-term

tests) in the modules. The UNTRIMMABLE channels were caused by high noises in the channels due to the increase of input capacitance by sensors.

Figure 5 shows the number of defective channels in a module in serial order. The plot “dead” was the number of channels of DEAD, STUCK, or UNTRIMMABLE channels that were subsequently masked by the channel mask registers. The plot “unbonded” was the channels that had the noise equivalent in the hybrids ( $ENC < 700$  e). The plot “noisy” was the channels with  $ENC > 2000$  e. The average ENC was found to be  $1695 \pm 53$  (stat.)  $\pm 200$  (sys.) e from all channels in all modules. The plot “total” was the sum of the above. The “dead” and “noisy” occurred randomly. The “unbonded”, however, had a structure: very small number below the module 60 and high above. Below the module 60, re-wire-bonding was made. Above the module 60, no re-wire-bonding was tried, after the finding of the bonding pad damage in the repairing.

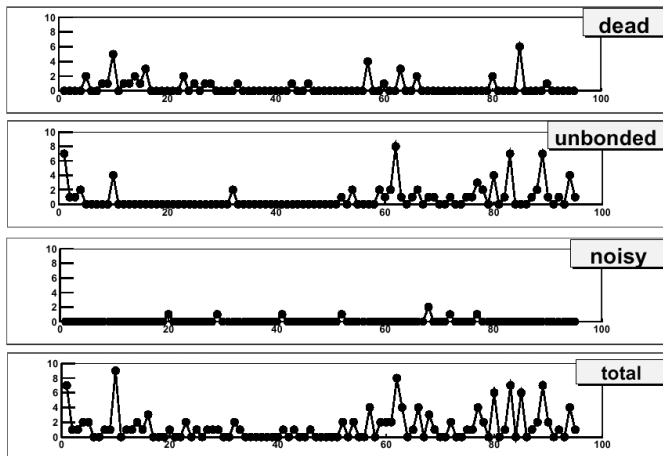


Figure 5: Number of defective channels in serial order

Table 3: Summary of defective channels in modules

Defect channels	Sum	Average no. per module	Maximum no. per module
“dead”	44	0.5	5
“unbonded”	76	1.2(*)	8
“noisy”	8	0.1	2
Total	128	1.8(*)	9

(\*) These were calculated using the modules larger than 60.

A summary of defective channels in modules is given in Table 3. The average of “unbonded” channels is calculated by using the modules greater than 60. The loss of channels was very small, less than 2 channels in average and 9 channels maximum that was still less than 1% of 1536 channels in a module. Although the loss was small, the largest loss was in “unbonded” channels. The reason of “unbonded” is being investigated and could be reduced by improving components and also by introducing re-wire-bonding with improvement in the process damaging the bonding pads.

## V. CONCLUSIONS

By the middle of August 2002, we have fabricated 120 hybrids with ASIC’s and 98 modules in Japan. We obtained 102 hybrids without defective ASIC’s and 93 electrically good modules. The rate of hybrids with defective ASIC’s was 9.7% and would be reduced to a smaller value by improving the ASIC screening that eliminates “Large gain spread”, “Trim-DAC loading failed”, “Negative offset”, and “Abnormal calib line” ASIC’s.

The yield of the modules was 83% if we rejected modules that were damaged in assembly or in handling, out of specification in the upper-lower alignment, and slightly inadequate in gluing hybrids. The yield in future will be improved as we have already achieved alignment well within specification and improvement in gluing hybrids. The loss of channels due to “unbonded” should be improved after finding the reason and introducing wire-bonding repairing without damaging the bonding pads.

## VI. ACKNOWLEDGEMENTS

The series module production is made possible by contributions of many individuals in the ATLAS SCT community. We would like to acknowledge E. Perrin of Univ. of Geneva, especially, for supporting the barrel module community as the SCT barrel system engineer.

## REFERENCES

- [1] Y. Unno, “ATLAS silicon microstrip Semiconductor Tracker (SCT)”, Nucl. Instr. Meth. A453 (2000) 109-120; M. Turala, “The ATLAS semiconductor tracker”, Nucl. Instr. Meth. A466 (2001) 243-254.
- [2] T. Kondo, et al., “Construction and Performance of the ATLAS silicon microstrip barrel modules”, Nucl. Instr. Meth. A485 (2002) 27-42 and references therein
- [3] AA. Carter, R. de Oliveira and A. Gandi, "Novel Thermal Management Structures and their Applications in New Hybrid Technologies and Feed-through Structures", CERN Report 99-08 (ISBN 92-9083-152-9). Also patent World International Property Organization: WO 00/03567A1 January 2000
- [4] W. Dabrowski, et al., “Progress in Development of the Readout Chip for the ATLAS Semiconductor Tracker”, in Cracow 2000, Electronics for LHC experiments, pp. 115-119, and references therein
- [5] P.W. Phillips, G.F. Moorhead, et al., <http://sct-testdaq.home.cern.ch/sct-testdaq/sctdaq/sctdaq.html>
- [6] R. Brun et al., An Object-oriented Data Analysis Framework, <http://root.cern.ch/>
- [7] National Instruments, VME-PCI8015 MXI-2
- [8] M. Morrissey et al., MuSTARD, SLOG documents, RAL internal notes
- [9] J. Bohm et al., ATLAS SCT Low Voltage Power Supply, V2.2, ATLAS SCT internal note
- [10] P. Malecki, ATLAS SCT High Voltage Power Supply, V2.04, ATLAS SCT internal note
- [11] A. Grillo et al., Testing specification for the wafer screening of the ABCD3T chip, Version V1.3, ATLAS SCT internal note
- [12] Mitutoyo, Quick Vision 250-PRO