Run2b Silicon Detector

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Design goals of Run2b Si system

Stave design

Silicon sensors

Schedule

Design goals of Run2b silicon

- Performance as good as/better than Run2a system
- **Simple and robust***, to be ready by summer 2004
- No changes for DAQ chains
  new (Si, chip-hybrid, mini-portcard, Junction PC)

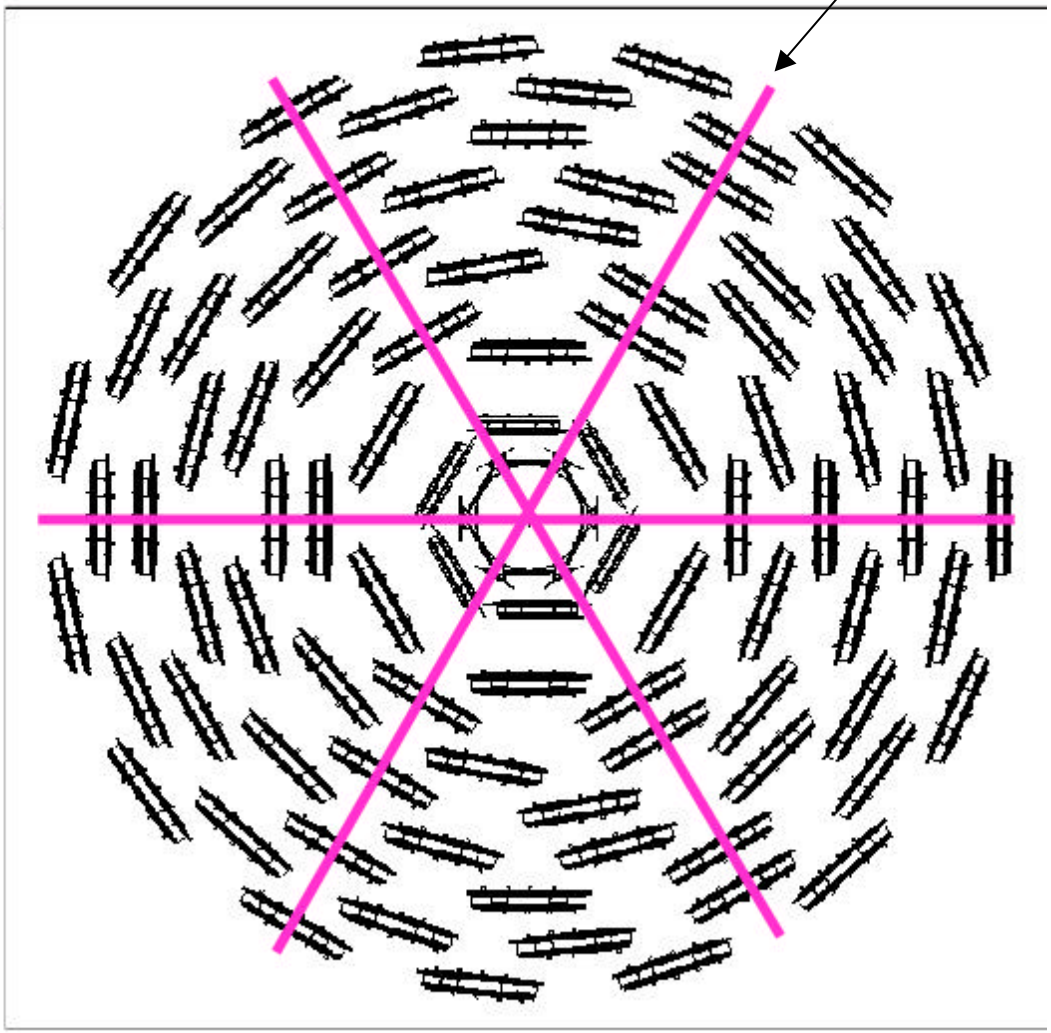
  SVX3 chips: Honeywell! (cost, yield), noise@large Cdet
  SVX4 chips: 0.25 μ m process, 2.5V, submitted before Christmas
  Fine-pitch hybrid (BeO) developed for L00
  Eliminate rad-critical (~5.7fb^{-1})DOIMs in Run2a portcard

***Uniform stave design(~90%)+special inner layer+a la L00**
Minimum use of light-weight cables

6-fold layout

106.5R(SVX2a)

163.5R



Changes from 4-fold design

- Dropped Layer 2!
- One outer layer stave design
- More symmetric
- Less overlaps
- Smaller pitch

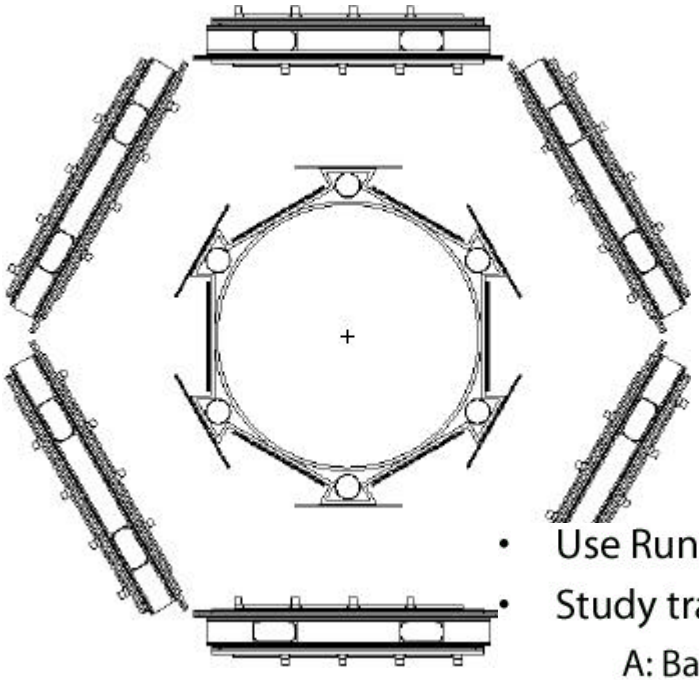
L1 axial coverage~0.7?

Layer 0: 12 fold Axial
Layer 1: 6 fold Axial-Stereo (90°)
Layer 2: 12 fold Axial-Stereo (90°)
Layer 3: 18 fold Axial-Stereo (2.5°)
Layer 4: 24 fold Axial-Stereo (2.5°)
Layer 5: 30 fold Axial–Stereo (90°)

6-fold wedge ⇨ SVT

90° @L1,3,5

Descoping?



Use outer staves for L1

Drop L4 or L5

- Use Run 2A simulation (well studied), ISAJET MC and ttbarevents.
- Study tracking (OI) and b-tagging efficiencies for different configurations
  - A: Baseline = Run 2a = L00 + 5 SVX layers + ISL and COT
  - B: Drop Layer 5 of SVXII
  - C: Inner axial and stereo layers of COT dead and drop L5
  - D: Inner COT layers dead and drop L4
- b-tag≡ 3σ Lxy for a jet. Results for 1000 events, stat. unc.~1.3%
- Fake track ≡ (MC d0 – found d0)>3σ for a prompt track. 100Evts,stat. unc. ~0.5%

	B-tag Eff. (%)	% Change
A	58.8	-
B	56.3	-4
C	51.3	-12.6
D	51.0	-13.3

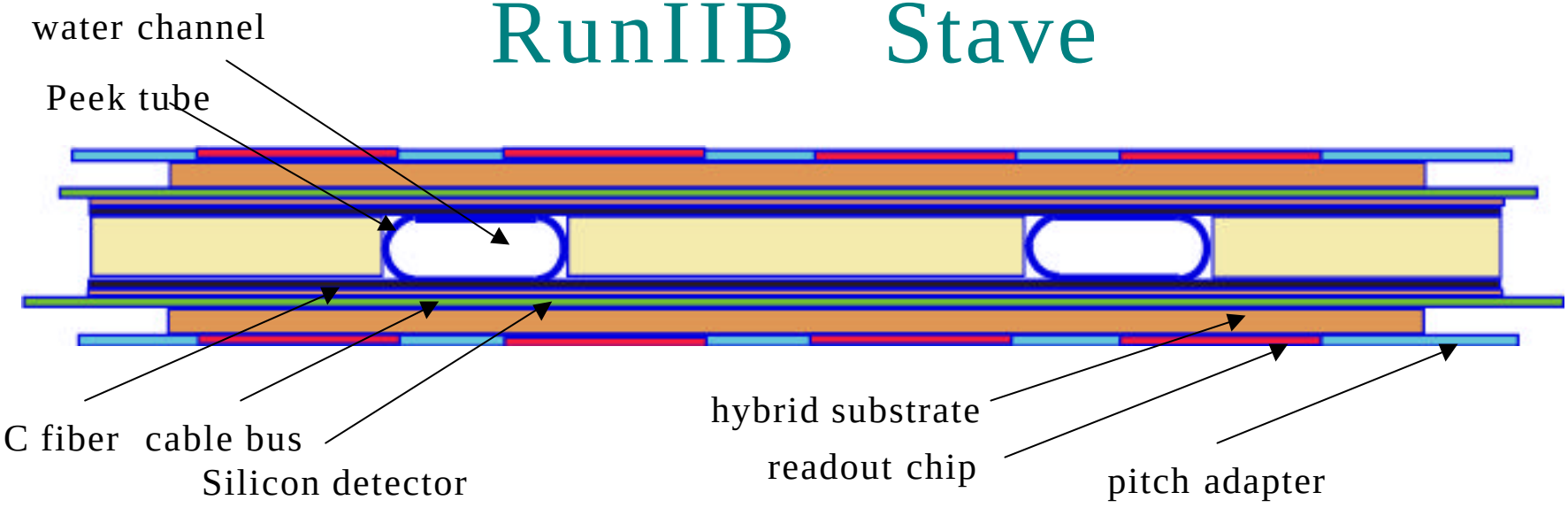
	% Fake Tracks	% Change
A	7.7	-
B	8.9	+16%
C	9.5	+23%
D	8.7	+ 13%

4%change

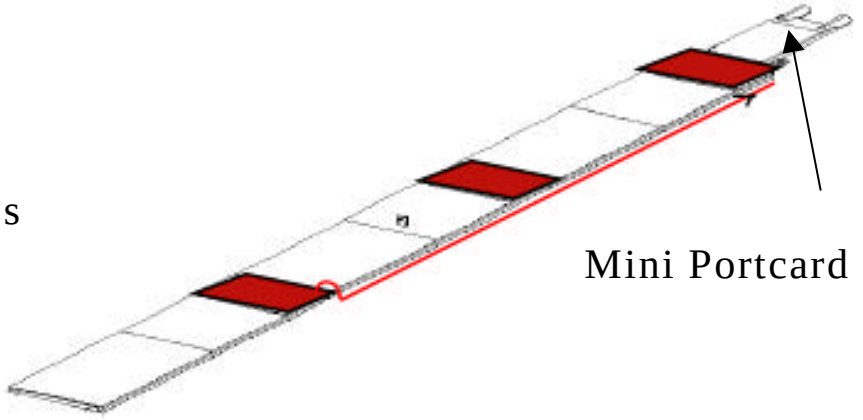
~3 GeV less M_H reach

~14% more *L*

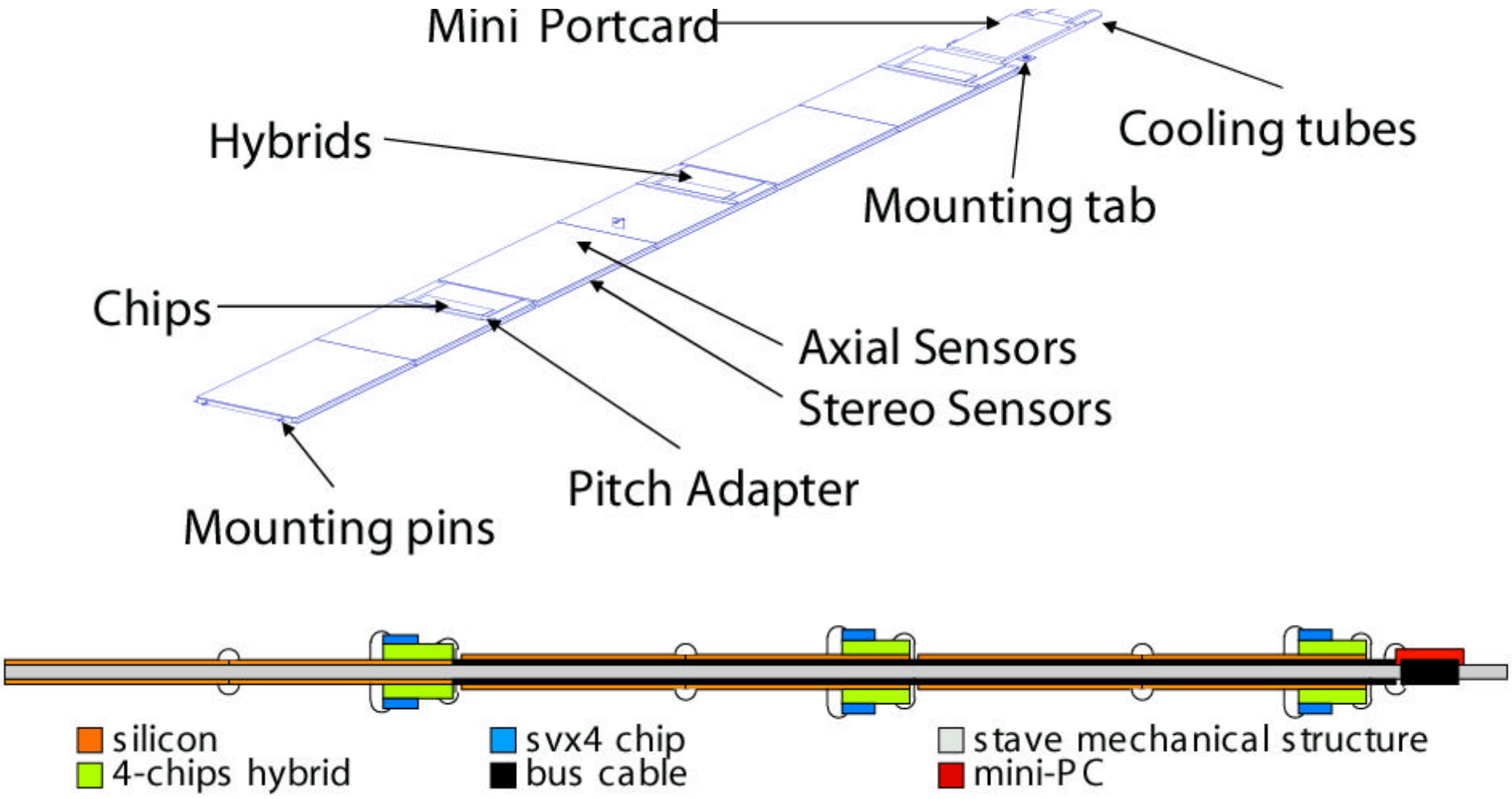
RunIIB Stave



- Stave structure (60 cm long, supported at z=0 and ±60cm):
  - Carbon fiber – rohacell structure with ~2x6 mm peek cooling pipes
  - On each side:
    - 6 single sided silicon sensors
    - 3 hybrids glued to the silicon.
  - Silicon glued to copper-kapton bus cables
  - Hybrids wirebonded to bus cables



RunIIB Stave



Number of Sensors

Layer	Fold	#staves	(axial)	(90 °)	(2.5 °)
L5	30	60	360	360	
L4	24	48	288		288
L3	18	36	216		216
L2	12	24	144	144	
L1	6	12	72	72	
L0	12	24	144		

Outer axial (75um) 1008
90 ° (93um) 504
2.5 ° (80um) 504
3 types 2016

Inner axial 144
axial' 72
90 ° 72
3 types 288

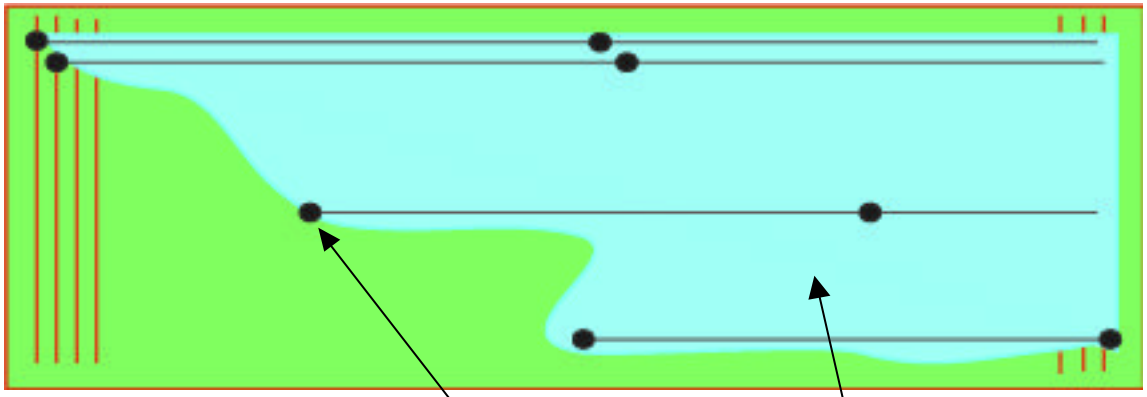
?

Micron

HPK:2300+spares=2700 → (13+ α)months @+200/mo

Si sensor : R&D issue

- Axial and SAS sensors are similar to ATLAS
- 90 ° on 6” process is new



SiO_2 insulator

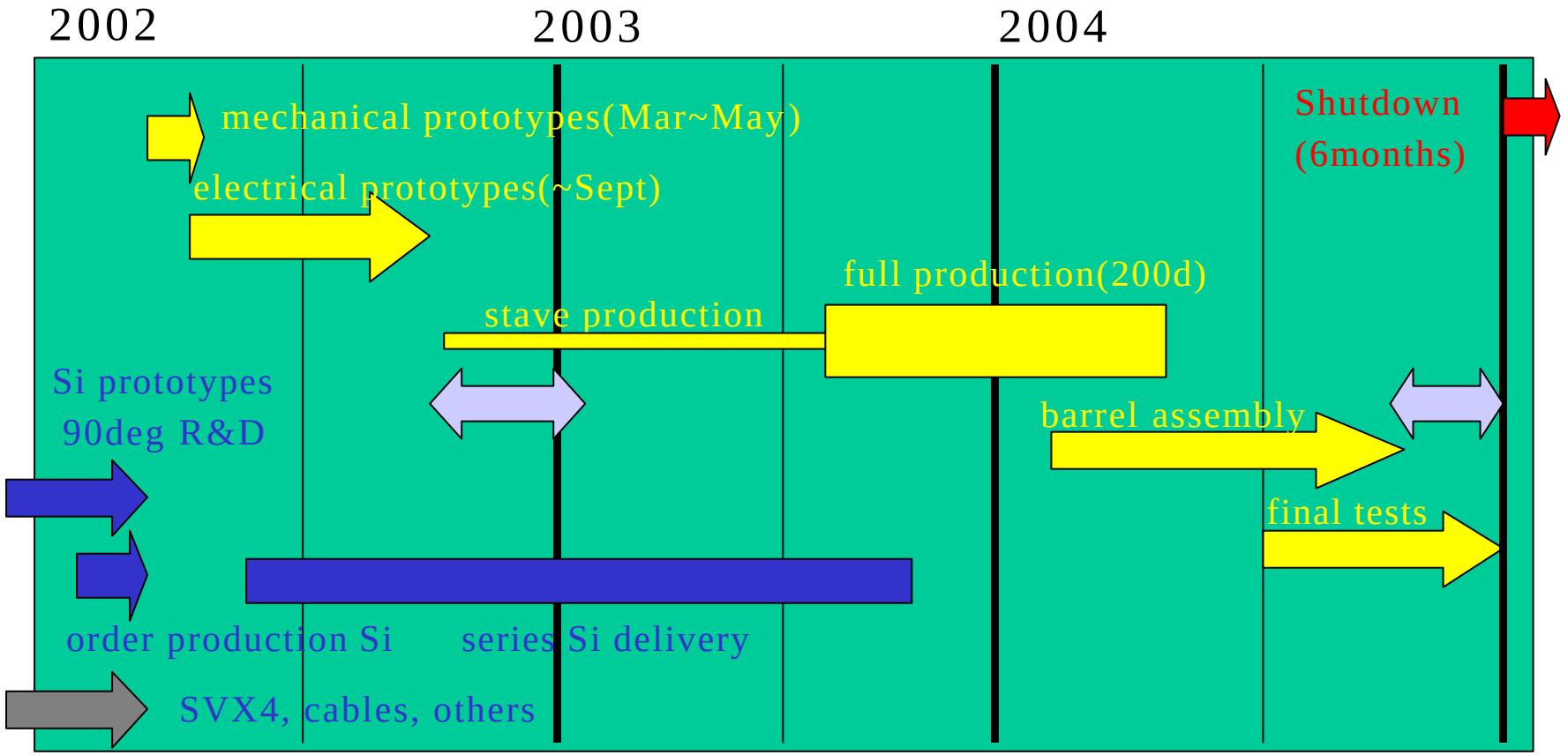
Previously achieved:

~4 μ m (4” SSDM)

~5 μ m (4” DSDM)

? (6” SSDM)

Schedule



Schedule risks: (1) SVX4 chip (for electrical prototyping, reliability)
successful operation w/ bus cable
(2) installation in 6-mon shutdown

Contingency ~6 months