

SOI (Silicon-On-Insulator) 技術を用いたピクセル検出器の開発



筑波大学
University of Tsukuba



原 和彦 (数理物質系)

- 素粒子実験でのPixel 検出器
- 読出し一体型SOI Pixel 検出器
- 筑波大のSOI Pixel開発経緯
 - 最初の放射線耐性
 - 薄型化(INTPIX)とテストビーム試験
 - 2重 SOI の導入
 - TrTEG6, INTPIXh2
 - FPIX2
 - 放射線耐性の向上化
 - SOFIST
- KEK MPWと新学術
- まとめ

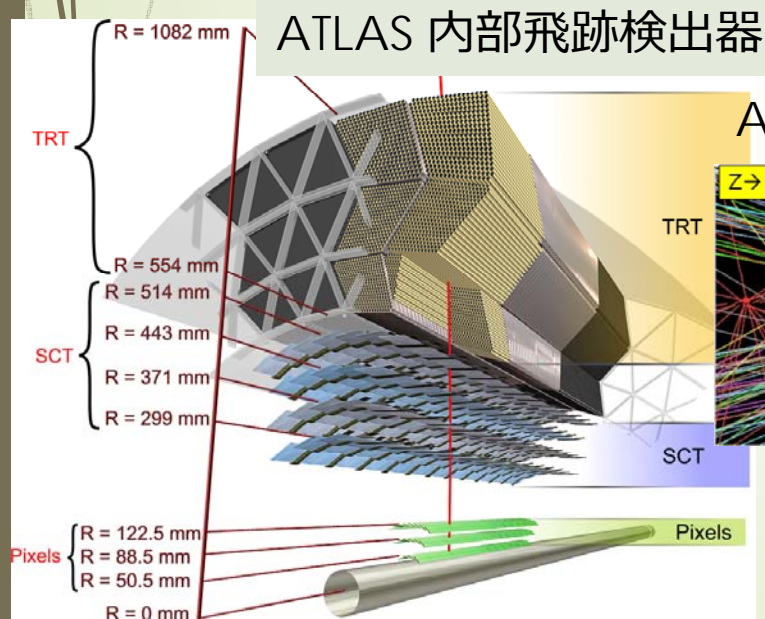
素粒子実験でのピクセル検出器

衝突点の近傍で飛跡検出

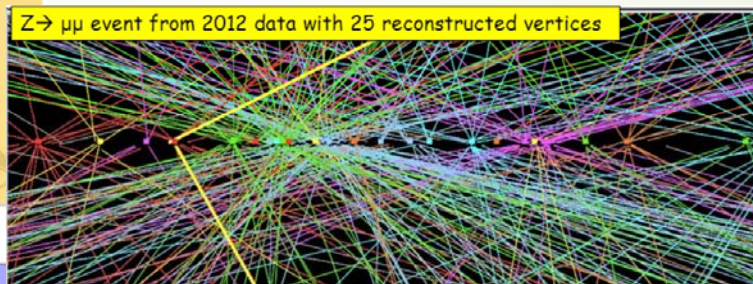
LHC-ATLAS: 3層⇒4層⇒5層(HL-LHC)

ILC-ILD: 5層(double layer)

	ATLAS (LHC⇒HL-LHC)	ILC
微細ピクセル	50x450um(⇒ 50x250um)⇒ 50x50um? (ハイブリッド)	5umの位置分解能 (読出し回路一体型)
高速信号	25nsを分離(全空乏化)	1msを分割(~全空乏化)
低物質質量	3.5% $X_0 \perp$ /layer⇒keep or less	0.16% $X_0 \perp$ /layer(一体型)
放射線耐性	0.5MGy, $10^{15}n_{eq}/cm^2 \Rightarrow x10 @HL-LHC$	~ 1 kGy/y, $\sim 10^{11}n_{eq}/cm^2 /y$

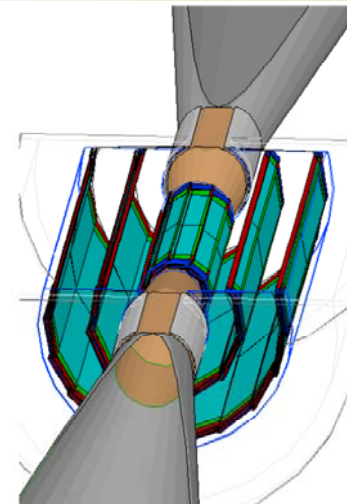


ATLAS での粒子発生(データ)



HL-LHCでは最大200 verticesへ

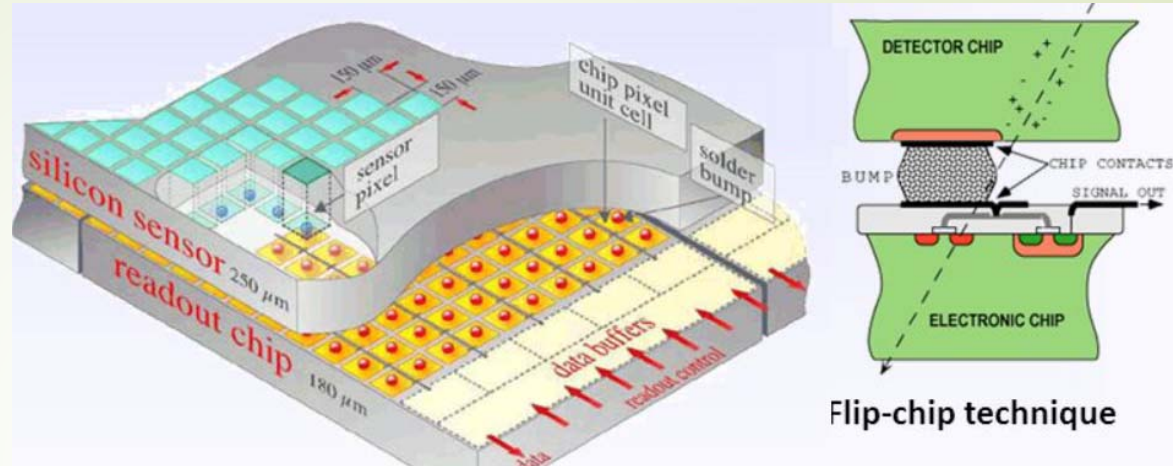
ILD pixel



HybridからMonolithicピクセル検出器へ

ATLAS Hybrid型pixel

Sensor部とR/O部を
BUMP BOND



Monolithic型pixel

CMOS

R/O circuit

全空乏化しにくい
(低抵抗)

HR-CMOS

R/O circuit

CMOS process最適化
(~高抵抗)

SOI-CMOS

R/O circuit

BOX

(~高抵抗)

R/O circuit

Deep Well
epitaxial (~高抵抗)

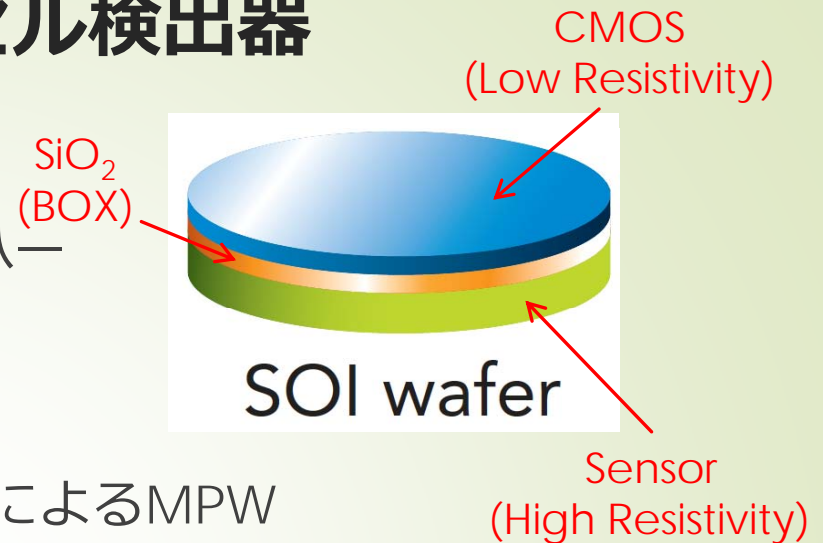
~25um

SOI-CMOSは回路プロセス、全空乏化両方に最適化されている
? 埋込酸化膜の放射線による帯電の影響

読出しー一体型SOIピクセル検出器

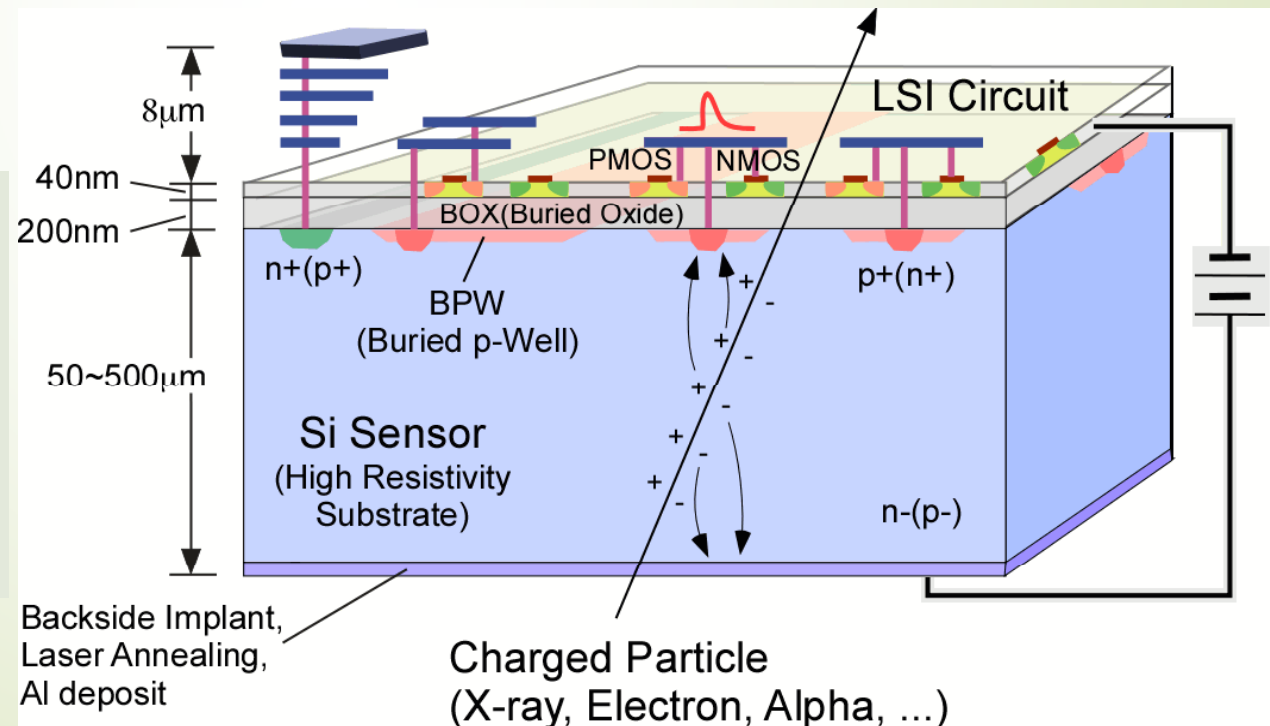
SOI Pixelの技術的特徴:

- Soitec (⇒信越化学) による張合ウェハー
従来抵抗値：CMOS回路の製作
高抵抗ウェハー：粒子検出部
→用途に応じた（全空乏型高速センサ）
- Lapis Semiconductor (0.2 μm CMOS)によるMPW
→reliable fabrication



Handle wafer:

- CZn ~ 700 $\Omega\text{-cm}$ (Default)
- FZn > 3 k $\Omega\text{-cm}$ (2009~)
- FZp ~ 25 k $\Omega\text{-cm}$ (2010~)
- Double SOI (CZn) (2012~)
- Double SOI (CZp) (2014~)



筑波大SOIピクセル検出器開発の経緯

2005年 KEK検出器開発室（幅教授）内にSOIグループ（新井教授） 発足
大学グループとして筑波大（原）が参加

K. Hara et al., Radiation Resistance of SOI Pixel Devices fabricated with OKI 0.15um FD-SOI Technology, IEEE TNS 56-5 (2009) 2896.

2009-12年 科研費「SOIピクセルによる高レート実験用薄型ピクセル」（新井-原）

M. Kochiyama et al., Radiation effects in silicon-on-insulator transistors with back-gate control method fabricated with OKI Semiconductor 0.20 um FD-SOI technology, NIM2011
K. Shinsho et al., Evaluation of Monolithic Silicon-On-Insulator Pixel Devices Thinned to 100 um, IEEE NS (2010)

2013-17年 科研費「高輝度加速器実験のための素粒子イメージング」（坪山-原）

S. Honda et al., Total Ionization Damage Compensations in Double Silicon-on-Insulator Pixel Sensors, PoS(TIPP2014)
K. Hara et al., Initial Characteristics and Radiation Damage Compensation of Double Silicon-on-Insulator Pixel Device, PoS(Vertex2014)
K. Hara et al., Development of Fine Pixel Detector for HEP Experiments Based on Innovative Double SOI Technology, IEEE2015 NS, San Diego

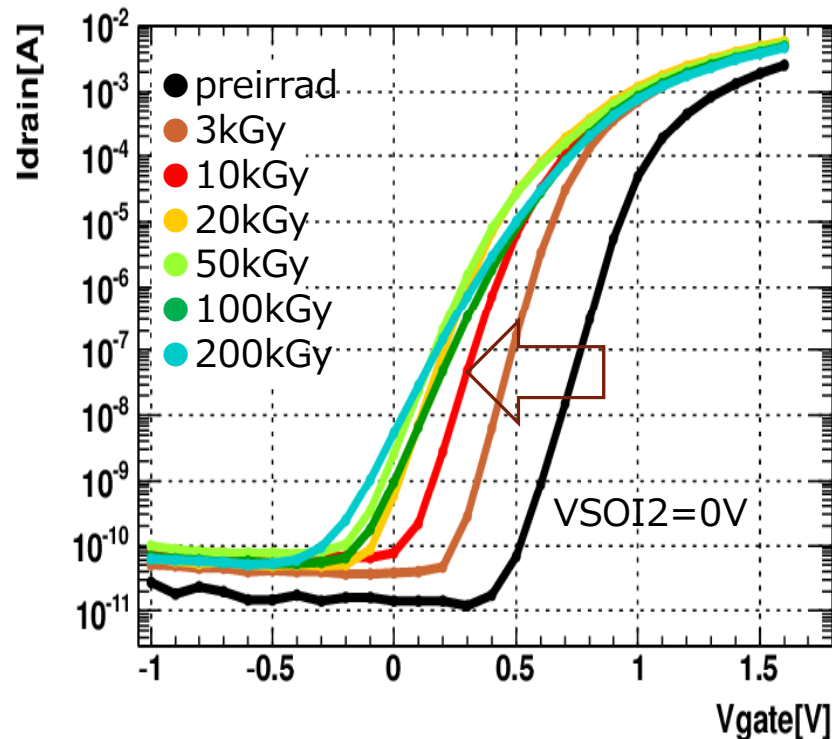
放射線耐性の評価(TrTEG,INTPIX)⇒Double SOIに焦点
微細DSOI-FPIXの製作
ILC用SOFISTの開発

放射線損傷 FETの I_D - V_{GS} 曲線

M. Kochiyama et al., NIM A636(2011)S62

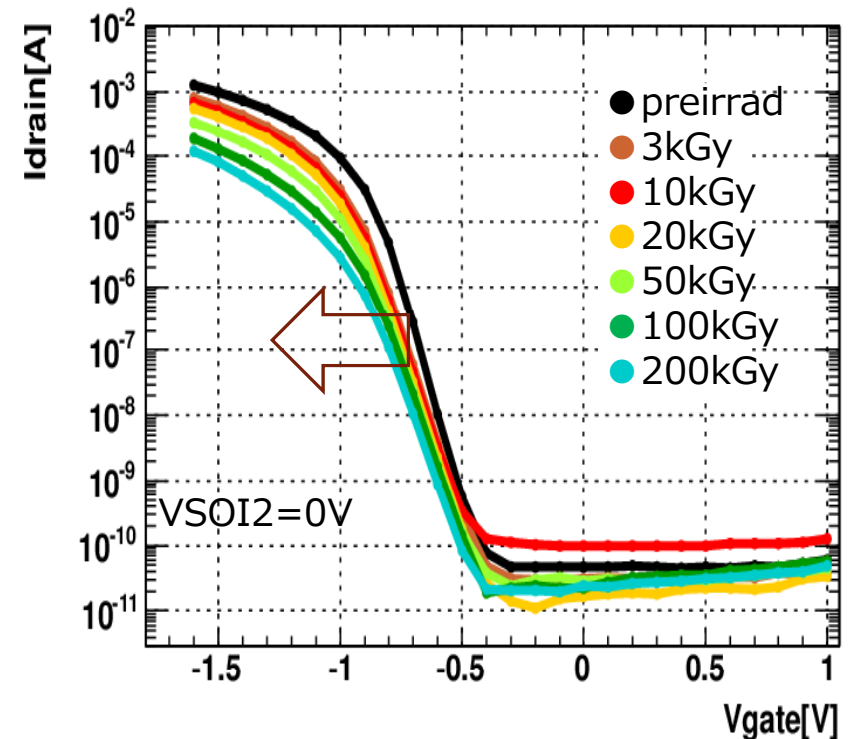
NMOS

IV curve(dose)(VSOI2=0V) tr_15_nch



PMOS

IV curve(dose)(VSOI2=0V) tr_15_pch



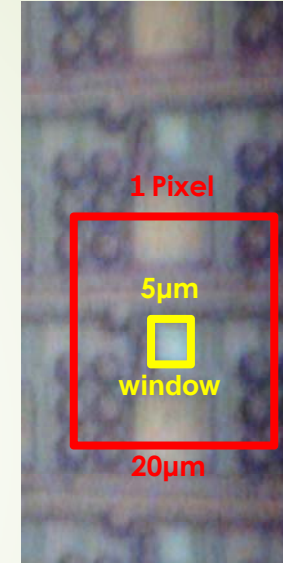
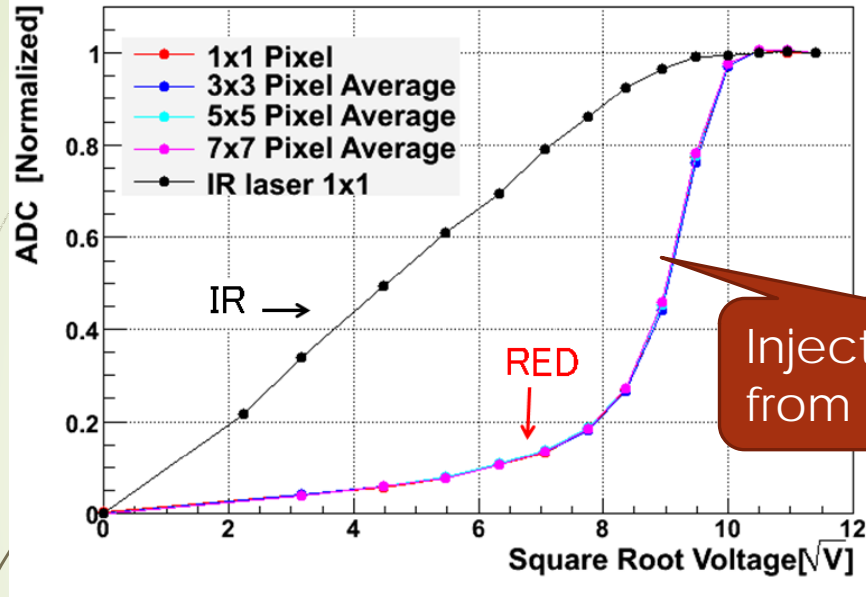
With accumulating dose, the curves shift negatively for both PMOS and NMOS, influenced by the holes accumulated in the oxide layer.

⇒ limited to a few kGy

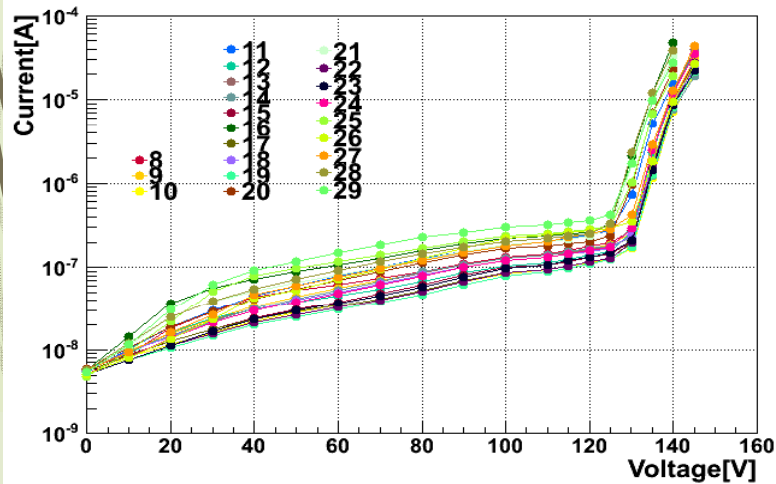
最初のSOI全空乏化ピクセル

K. Shinsho et al., IEEE2010 CR N23_2

100 um thick INTPIX3 Cz (n)

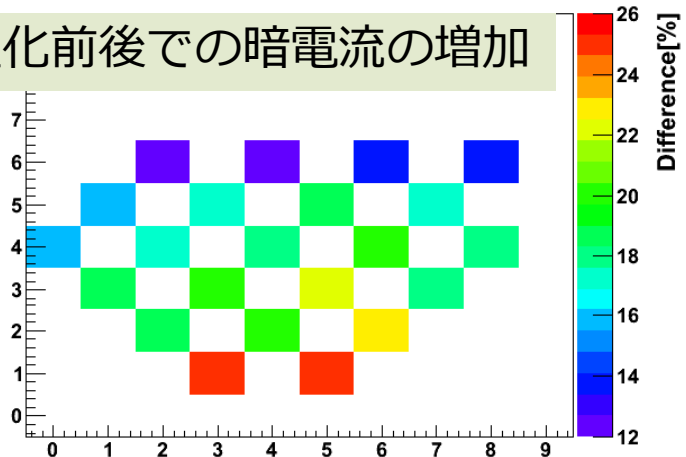


INTPIX3 IV AfterThinning



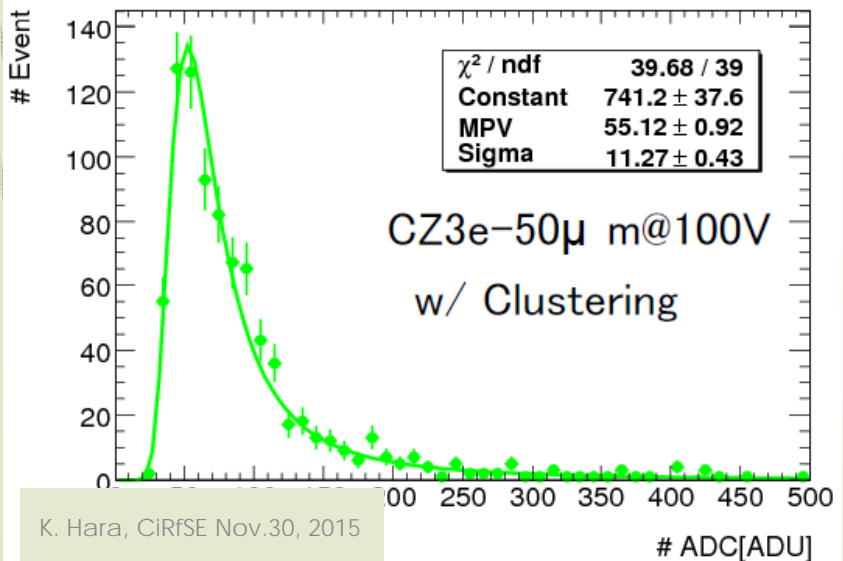
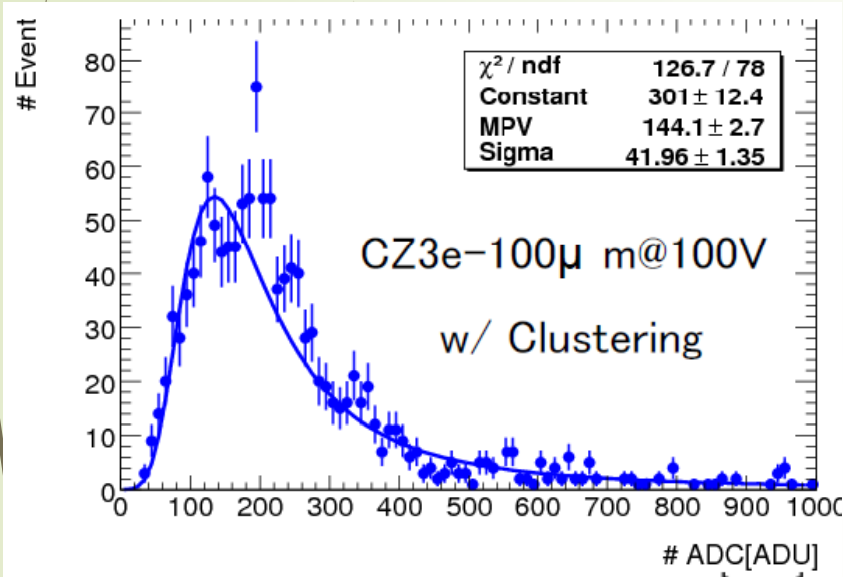
Current Map@100V

薄型化前後での暗電流の増加

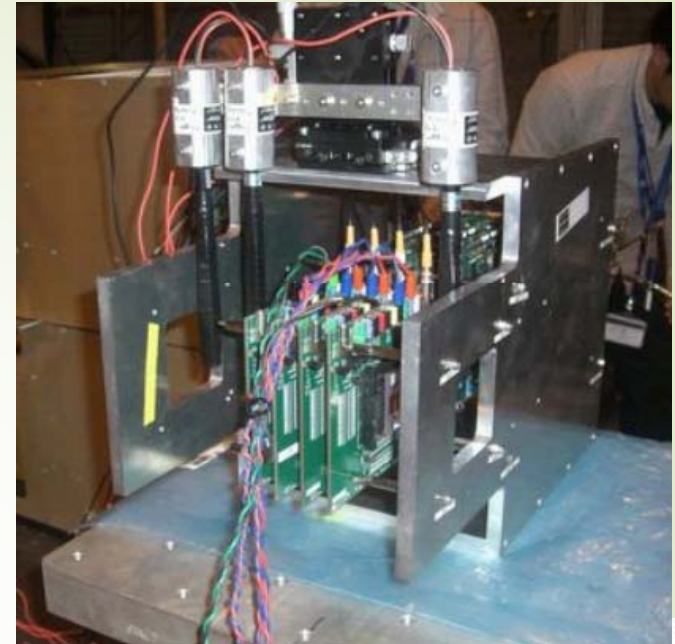


CERN Test Beam (2011)

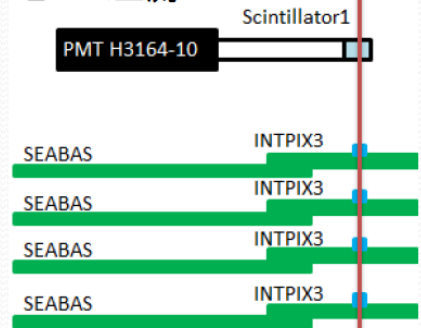
K. Shinsho 修論(2012)



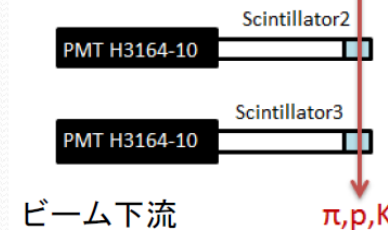
K. Hara, CiRFSE Nov.30, 2015



ビーム上流



INTPIX3:
16x16 μ m pixel size
Thinned to 100/50 μ m



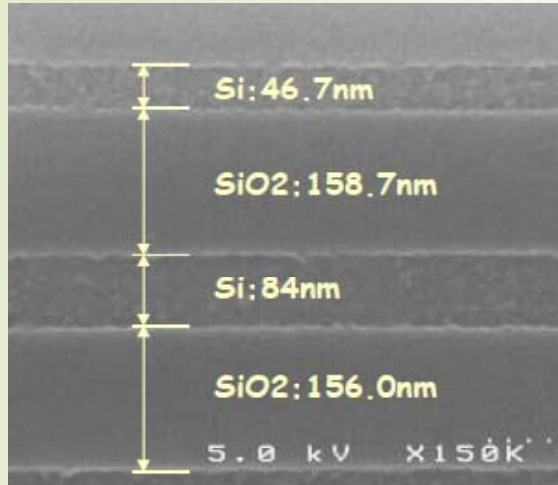
ビーム下流

π, p, K

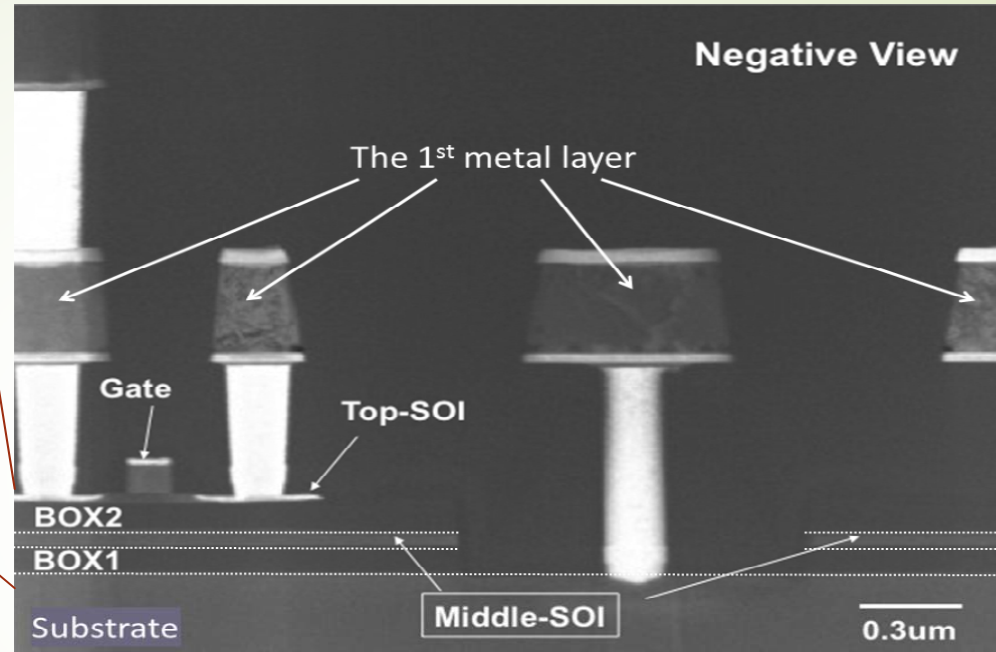
2重SOI による TID Recovery

2012~

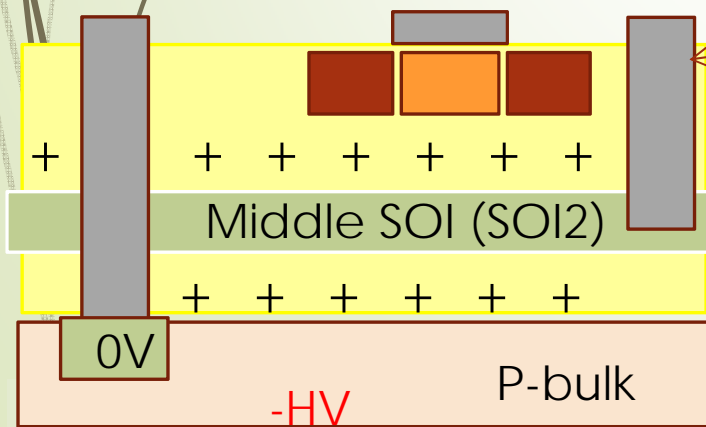
(SOITEC DSOI)



Courtesy of Lapis SemiConductor



(SHINETSU DSOI)



apply negative voltage (V_{SOI2}) to compensate positive charges in oxide layers



SOITEC nCZ



SHINETSU pCZ

Co- γ Irradiations (Double SOI): TrTEGs

Irradiation performed at RT at rate of 0.3~5kGy/h; No annealing

3kGy~2MGy (200Mrad)

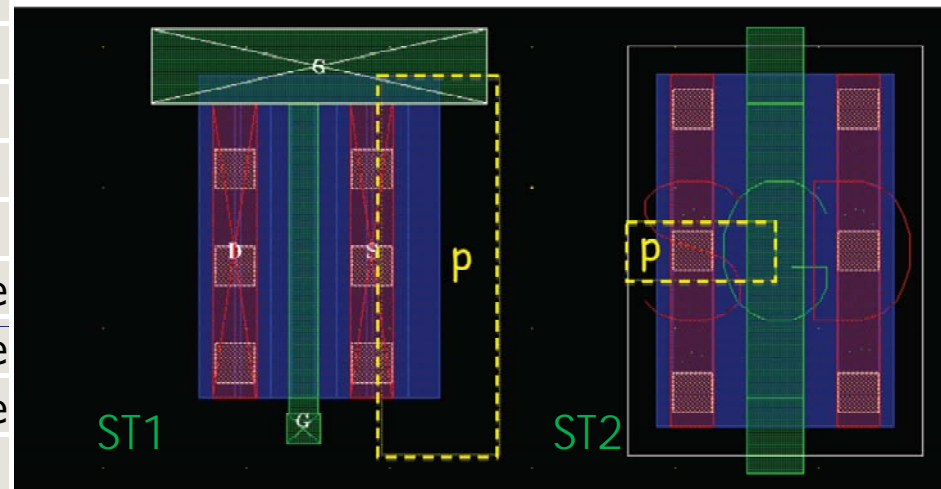
18 species each for PMOS/NMOS

tr	L[um]	W[um]	m	Comment
0	0.20	5	4	NVT
1	0.50	5	10	NVT
2	1.00	5	20	NVT
3	0.20	5	4	HVT
4	0.50	5	10	LVT
5	1.00	5	20	LVT
6	0.35	5	7	iohvt
7	0.35	5	7	iohvt
8	0.20	5	4	lvt_s-tie
9	0.50	5	10	lvt_s-tie
10	1.00	5	20	lvt_s-tie
11	0.40	10	4	nvt_s-tie2
12	0.60	6	10	nvt_s-tie2
13	1.00	5	20	nvt_s-tie2
14	0.20	5	4	nvt_multib-tie
15	0.50	5	10	nvt_multib-tie
16	1.00	5	20	nvt_multib-tie
17			20	Io_s-tie

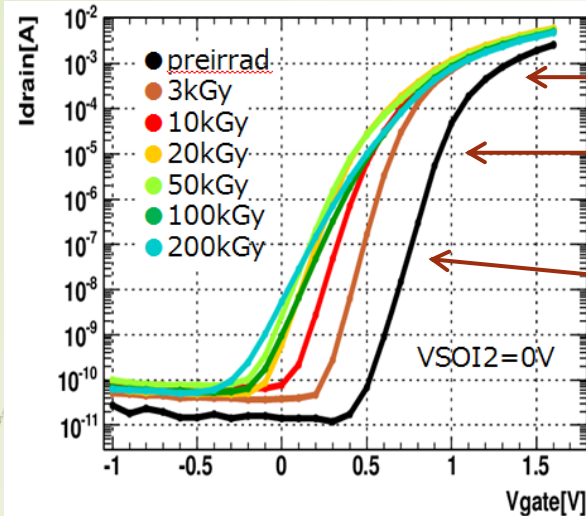
0.5kGy~100kGy (10Mrad)

11 species each for PMOS/NMOS

TR	L	W	M	COMMENT
0	0.20	5	1	LVT
1	0.20	5	1	NVT
2	0.40	5	1	NVT_S-TIE2
3	0.35	5	1	NVT_S-TIE2
4	0.20	5	1	NVT_S-TIE
5	0.35	5	1	IOHVT
6	0.35	5	1	IONVT
7	0.40	5	1	IOHVT_S-TIE2
8	0.35	5	1	IONVT_S-TIE2
9	0.35	5	1	IONVT_S-TIE
10	0.40	2.5	2	NVT_S-TIE2



Tr characteristics recovery by V_{SOI2} -Id-Vg curves: typical examples



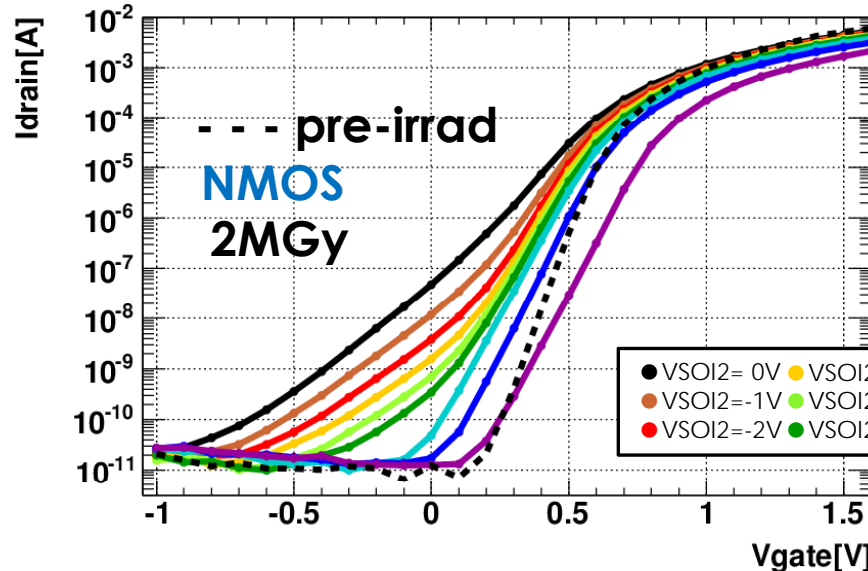
Transconductance (g_m): $I_d \sim g_m V_g$

Threshold (V_{th}): $V_{gate} @ I_d = (100nA) \times (W/L)$

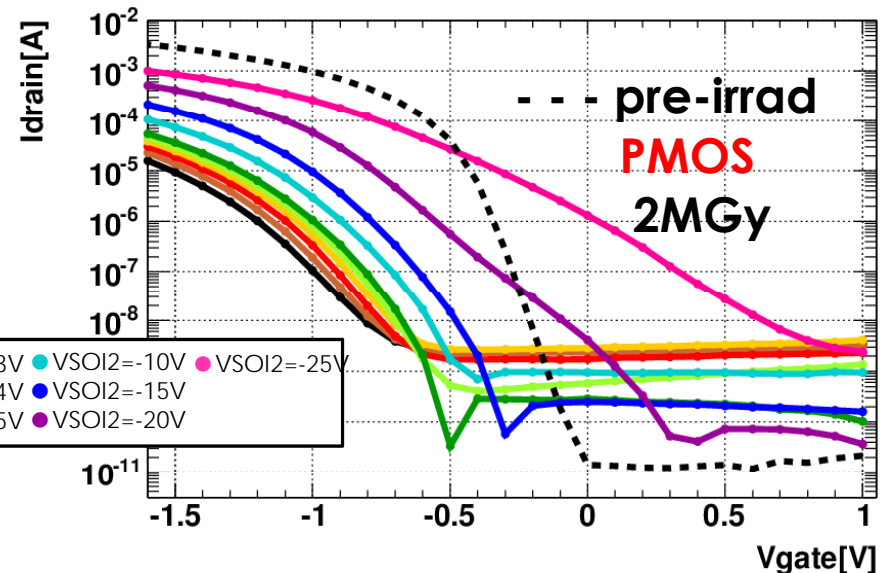
Sub-threshold Swing (S)
(I_d multiplied by 10 for V_{gate} increase by $S[V/dec]$)

S. Honda

tr10 : nch_L0.50_W5_m20_colvst

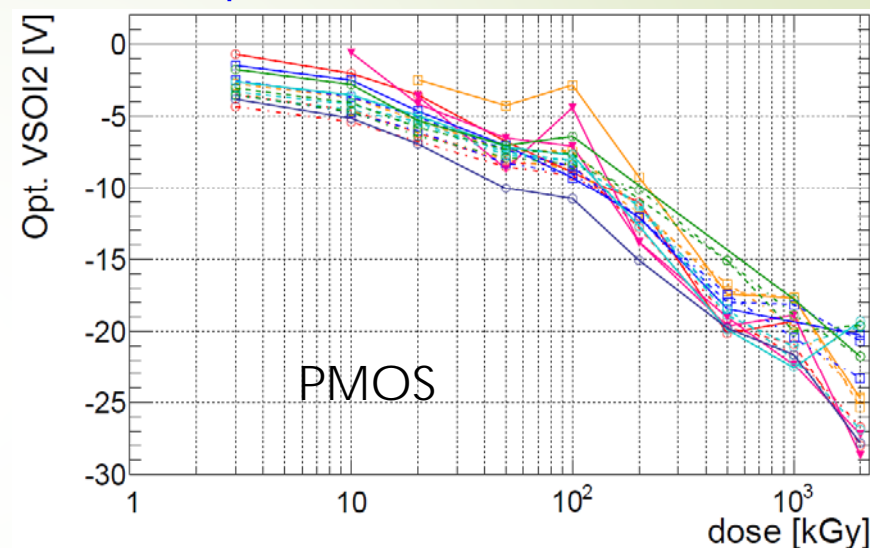
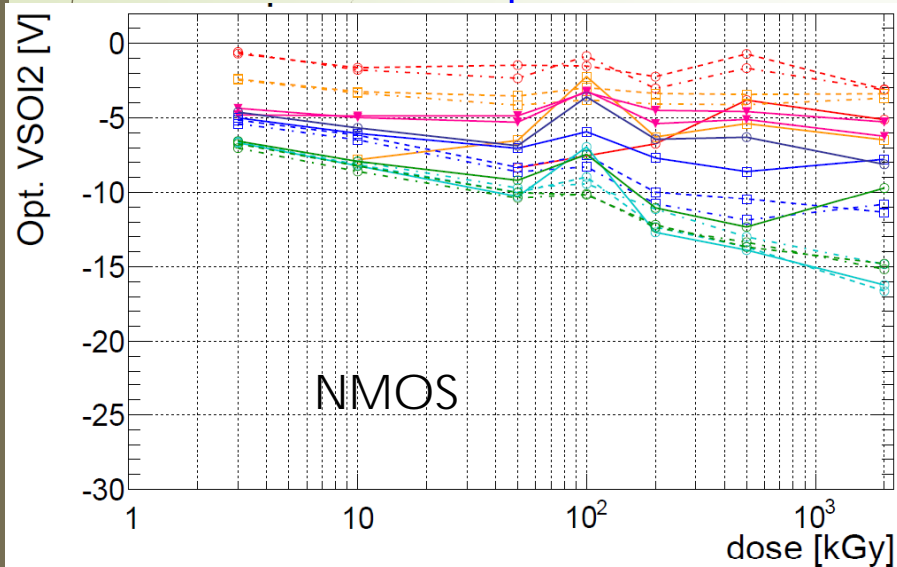


IV curve(V_{SOI2})(dose=2000kGy) tr10_pch



Optimum V_{SOI2} for V_{th} compensation

V_{SOI2} to compensate for V_{th} to back to pre-irradiation

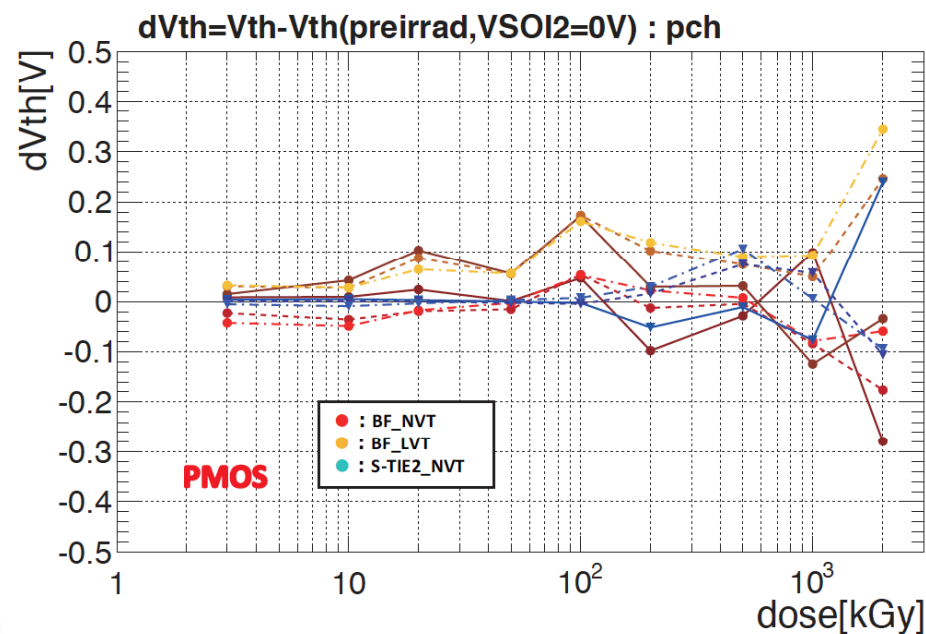
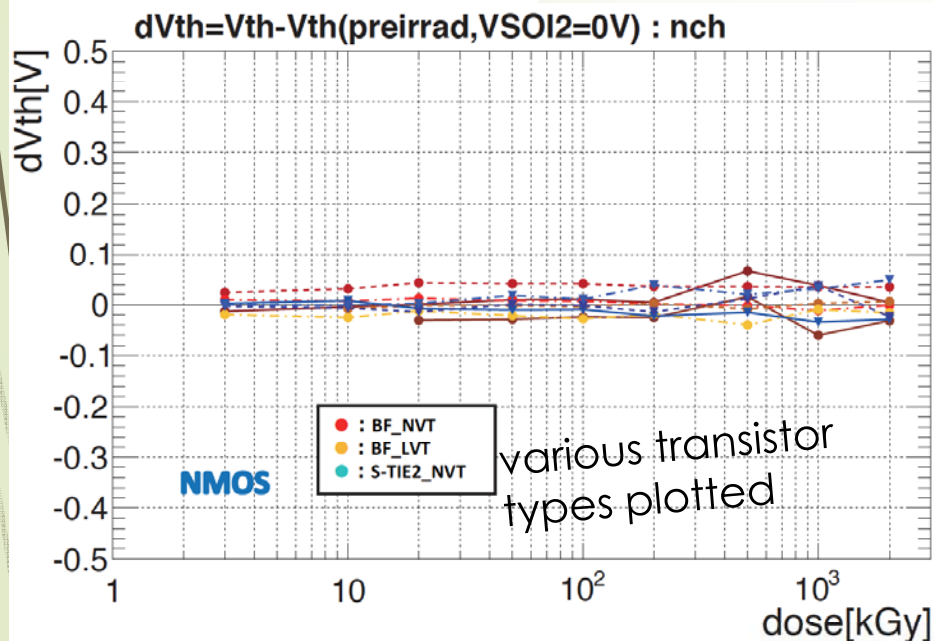


Noticeable differences are observed among various transistor types.
 → Different V_{SOI2} settings are preferred to compensate fully the TID for NMOS, PMOS and each body connections.

Example V_{th} Compensation Schema

Scheme: Average of optimum V_{SOI2} separately for BF and S-TIE2 for NMOS
 Average of optimum V_{SOI2} for all types for PMOS

Residual of V_{th} shifts



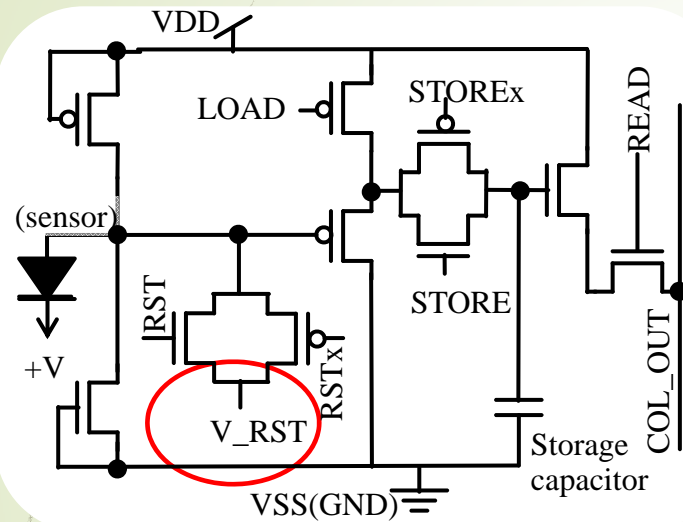
V_{th} are compensable within ± 0.05 V for NMOS
 and with ± 0.1 V for PMOS in this scheme.
 Need further consideration for PMOS~2MGy

Response of Irradiated Pixel Circuit

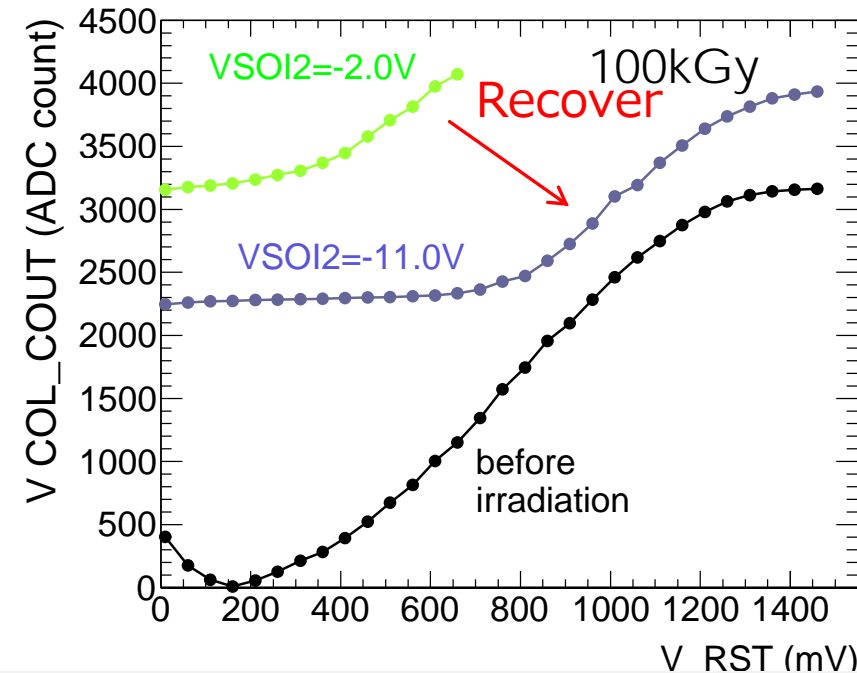
M. Asano

INTPIXh2 : Integration-type pixel sensor (single VSOI2 control)

Functionality of electronics examined utilizing RESET voltage (V_{RST}).



Bias voltage = 100V
Integration Time = 120ns



INTPIXh2 response recovered with VSOI2.

Dynamic range is degraded since optimum VSOI2 setting depends on the transistor types (NMOS, PMOS effectively).

Expect the dynamic range is recovered further if VSOI2 is set depending on the transistor types.

Pixel Evaluation

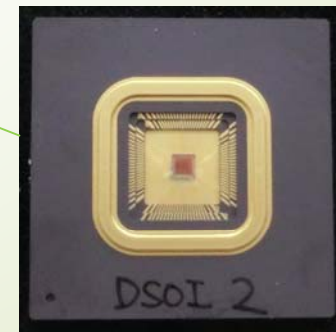


IR pulse laser (~10ns)

RED picosecond
pulse laser

SEABAS2
12b ADCx16ch

↑ 8 parallel outputs

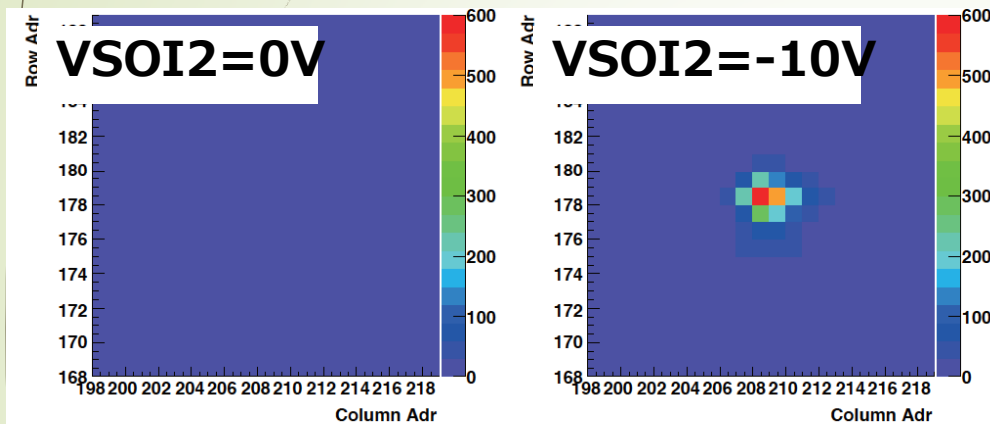


PIXEL on carrier

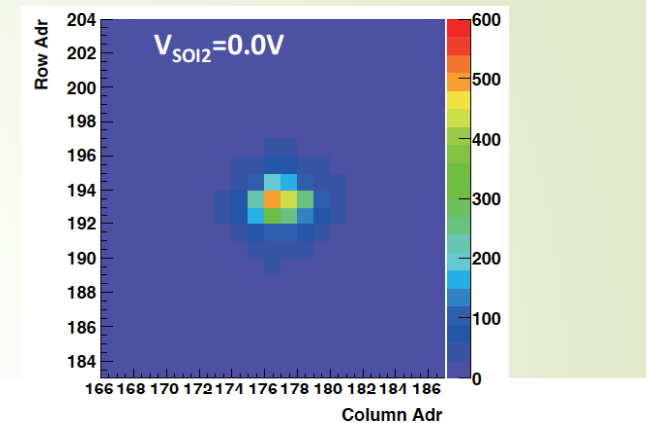
Response of irradiated DSOI Pixel

M. Asano

Response to infrared laser of 1064 nm wavelength and 20 ns pulse duration.

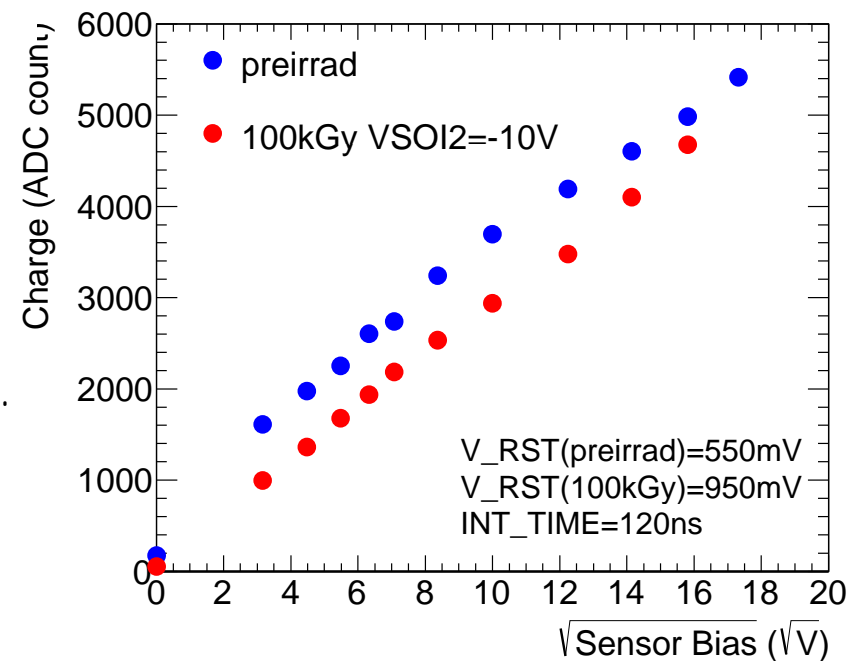


Pre-irrad



Images after 100 kGy disappeared but recovered with $V_{SOI2}=-10V$.

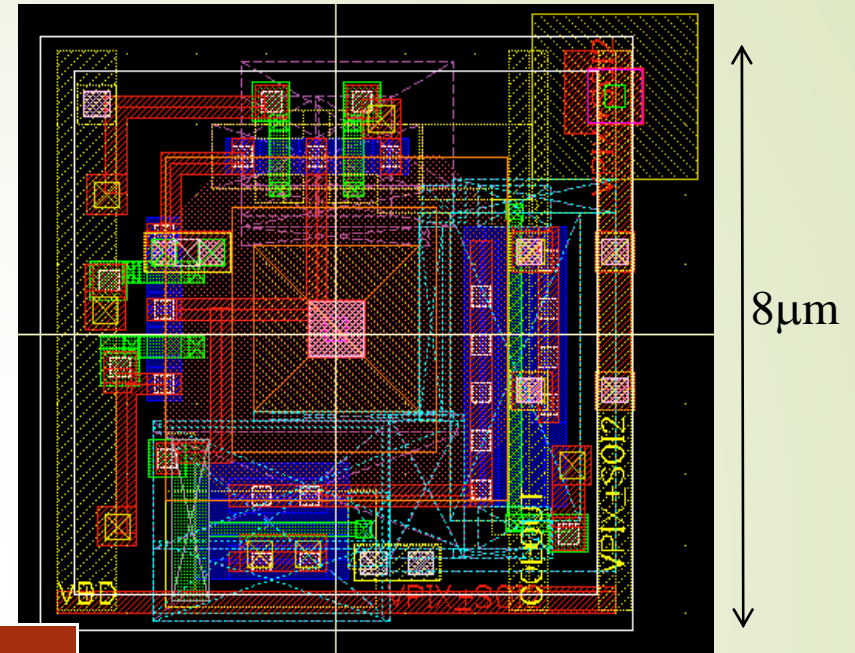
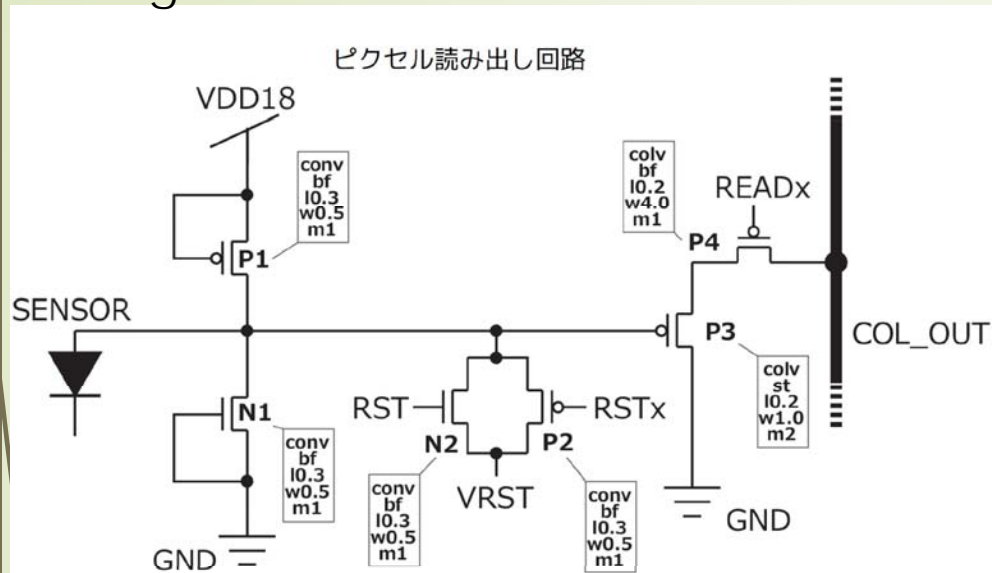
Average ADC count vs. the bias voltage.
 → Linearity and sensitivity after 100kGy (with $V_{SOI2}=-10V$) are similar to pre-irradiation



FPIX2: Pixel design

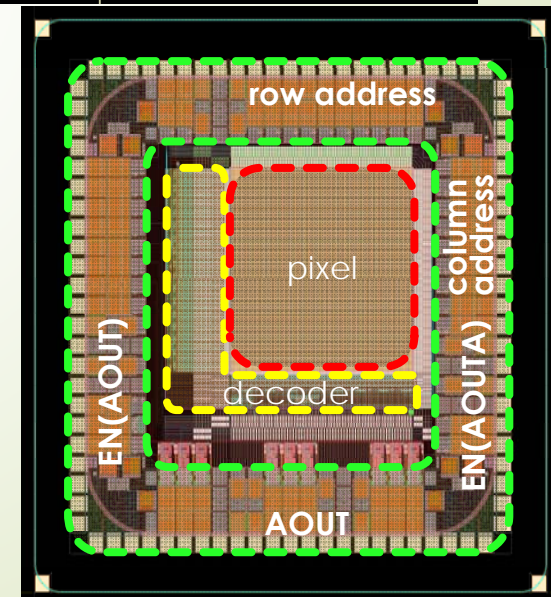
S. Honda

Rolling-shutter R/O



Item	Specifications
chip size	2.9mm x 2.9mm
Pixel size	8μm x 8μm
Number of pixels	128x128
(Rows x columns) x blocks	(128x16) x 8
Active region	1024 μm x 1024 μm
Outputs	8 parallel/1 global

3 V_{SO12} controls for pixel/decoder/IO regions

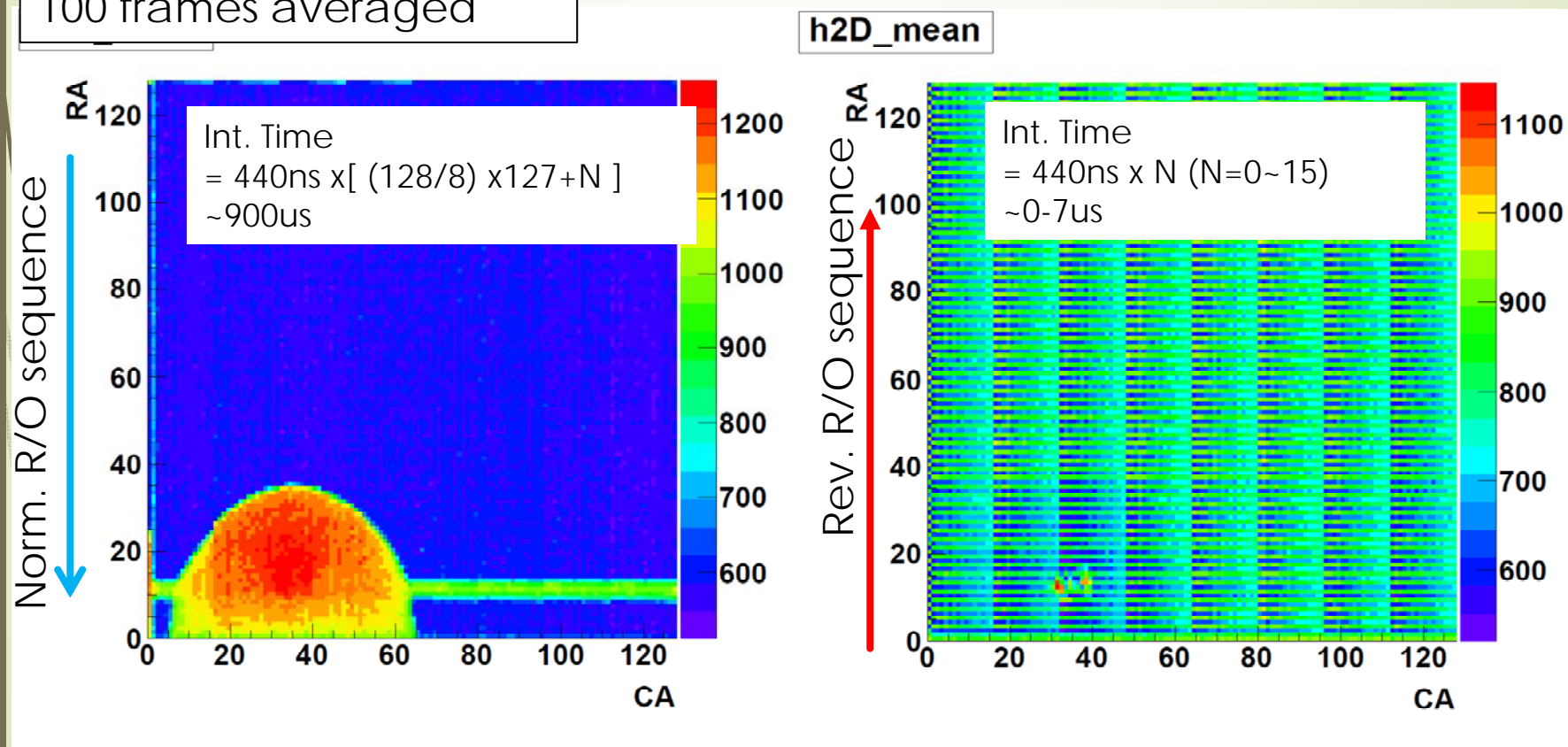


Rolling-Shutter Parallel Readout

M. Asano

ScanTime=440ns
 Bias=40V
 NFZ (single as reference)
 100 frames averaged

RED asynchronous
 laser pulse (100kHz, <1ns)



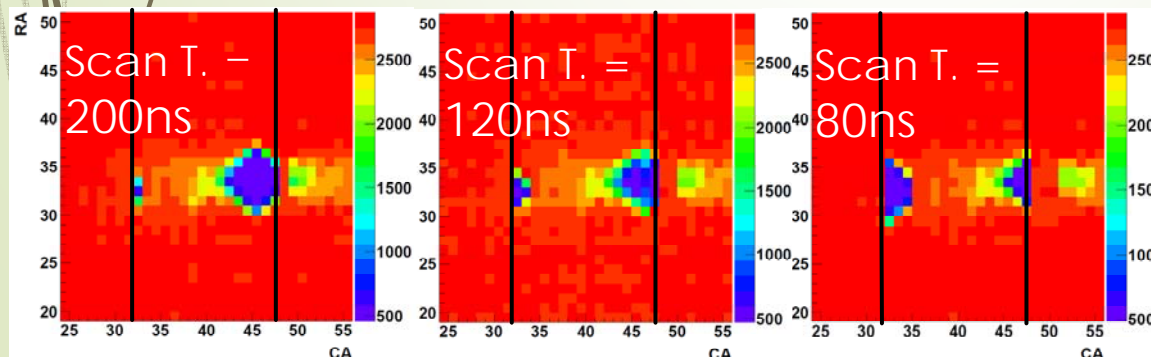
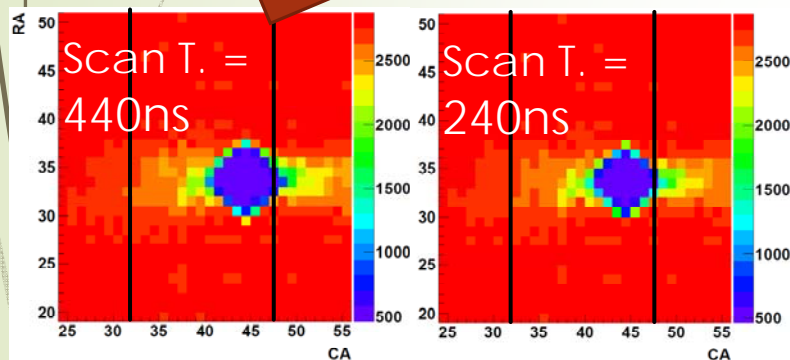
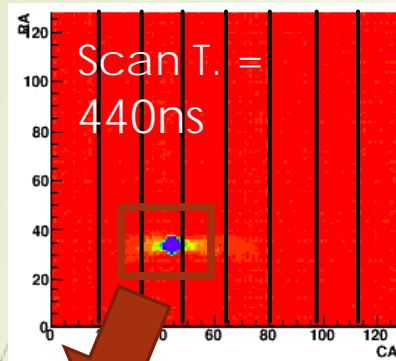
Images as expected from different Integration times
 Eight parallel readout lines active!

Scan Time

M. Asano

DSOI

RO with 8 parallel ADCs



Scan Time (digitization time for each pixel) requires $>200\text{ns}$ to keep the laser spot un-distorted.

digitization by SEABAS2 12b ADCs

FPIX2 is a working DSOI device to examine the functionality against radiation

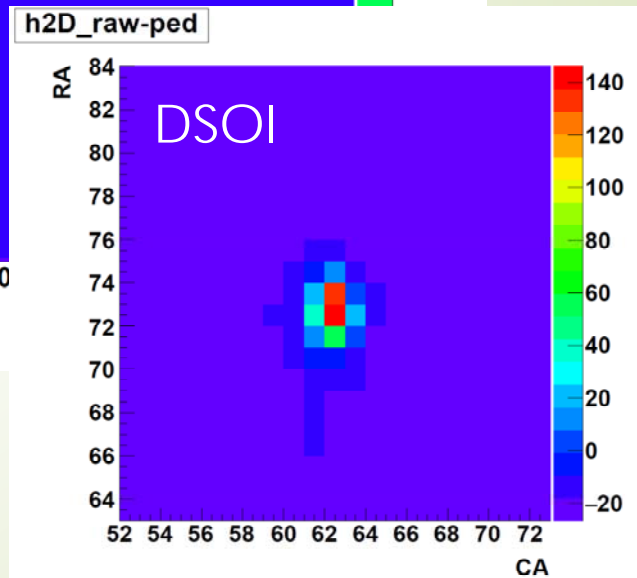
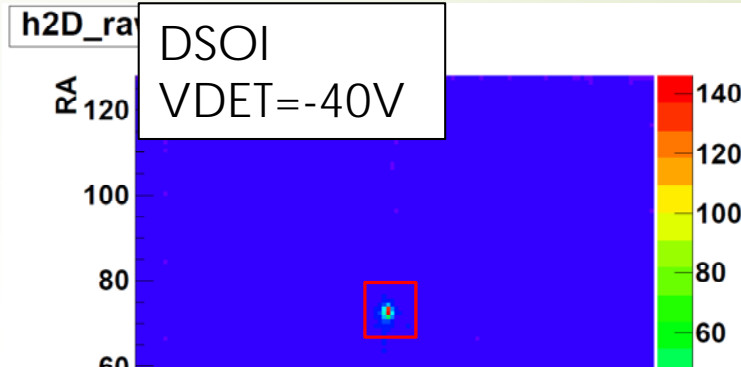
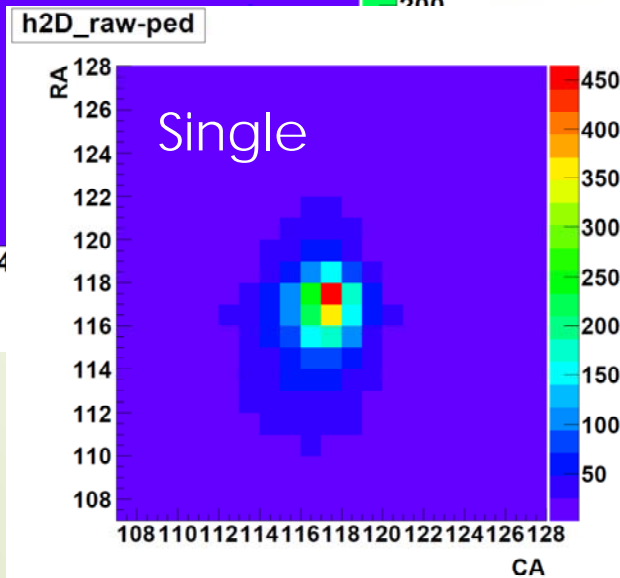
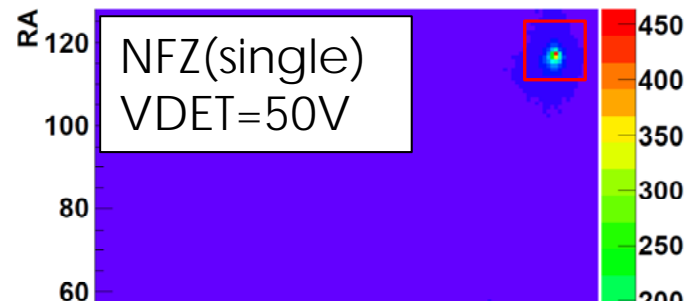
\Rightarrow another pixel device with pixel and column amps optimized for shorter scan time is in process for fast HEP application

Non-irrad sensor
 $V_{\text{det}} = -50\text{V}$
 $V_{\text{SOI2}} (\text{IO/DEC/pix}) = (0\text{v}/0\text{v}/-0.25\text{v})$
 $\text{RESETV} = 1500\text{mV}$

Response to collimated IR laser M. Asano

ScanTime=440ns
Pedestal subtracted
500 frames averaged

IR laser (~10ns) collimated on one pixel
(pixel window $2 \mu\text{m} \square$)



Similar profiles for single and double spread caused by carrier diffusion, laser angle and focusing,...

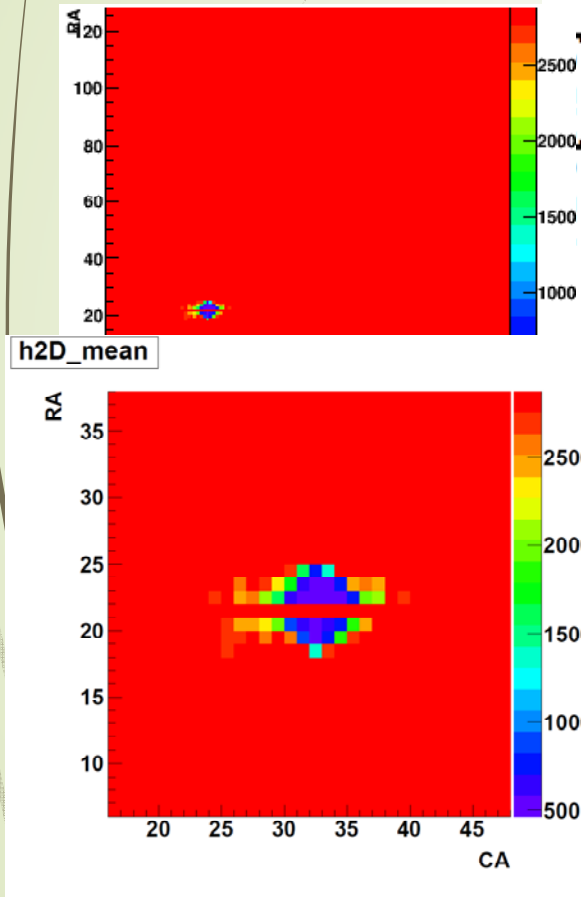
Performance after 100kGy

M. Asano

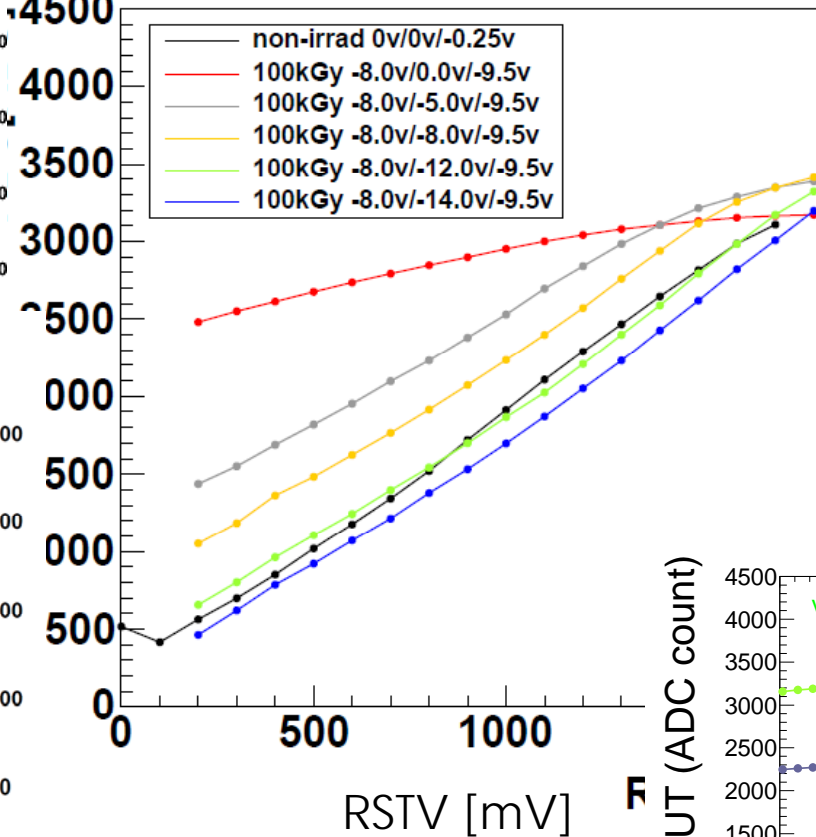
DSOI

VSOI2(IO/Dec/pix)=-12V/-12V /-9.5V

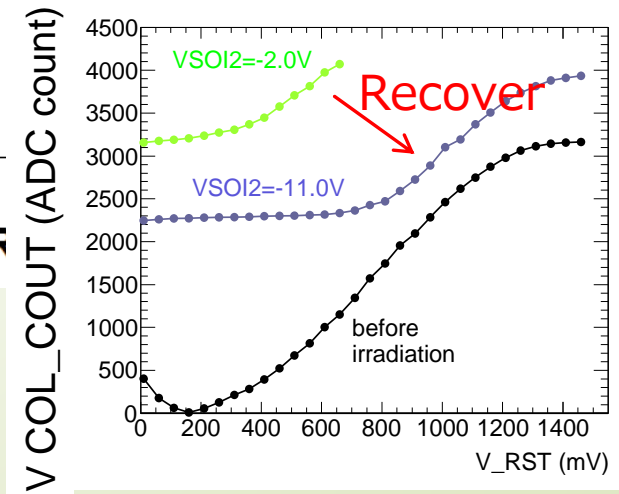
Response to RED



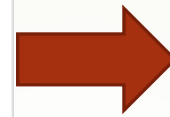
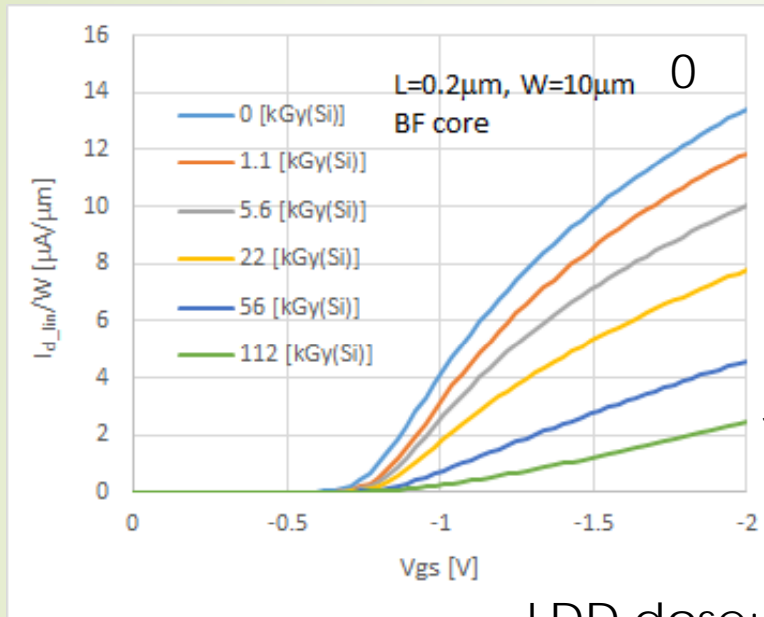
RSTV response: dependence on VSOI2(Dec)
Fully recoverable to pre-irrad



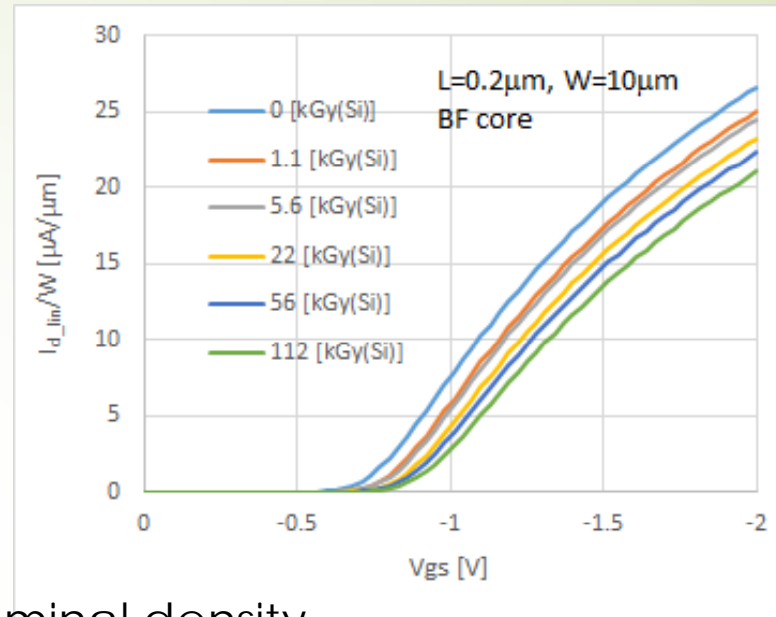
Previous DSOI
INTPIXh2 w/ a single
VSOI2 control



Improvement of PMOS g_m reduction



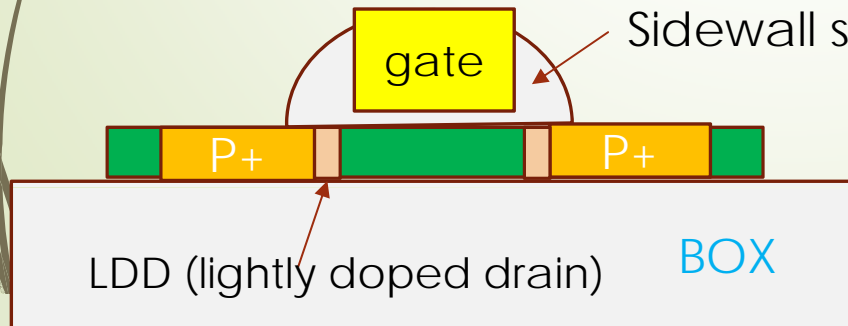
112kGy



LDD dose: \Rightarrow x6 nominal density
 g_m reduction 80% \Rightarrow 20% at 112 kGy

Effective gate length modulation by radiation

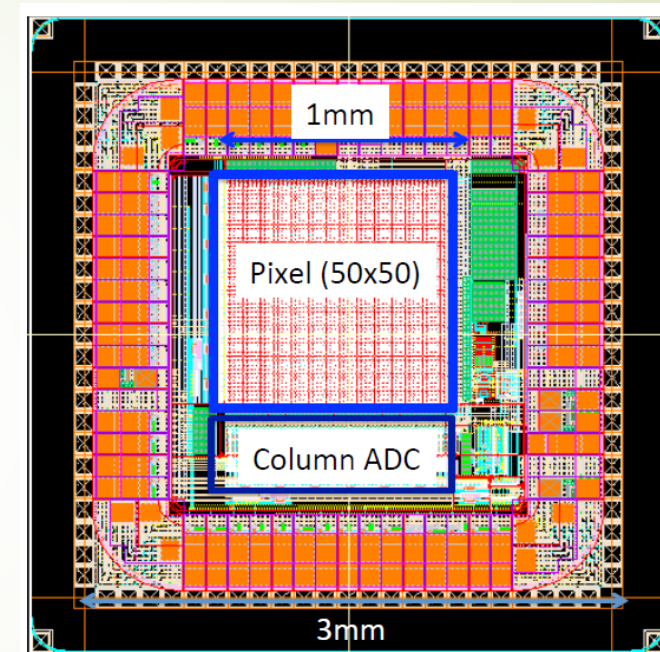
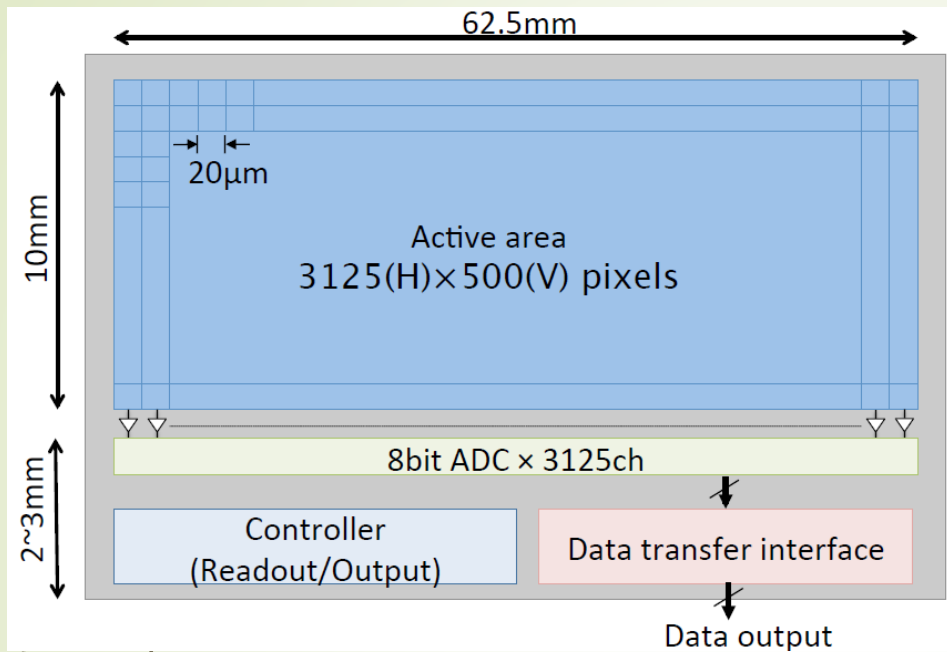
I. Kurachi,, K. Hara, et al., IEEE Trans of Elec.Dev. 62 (2015)2371.



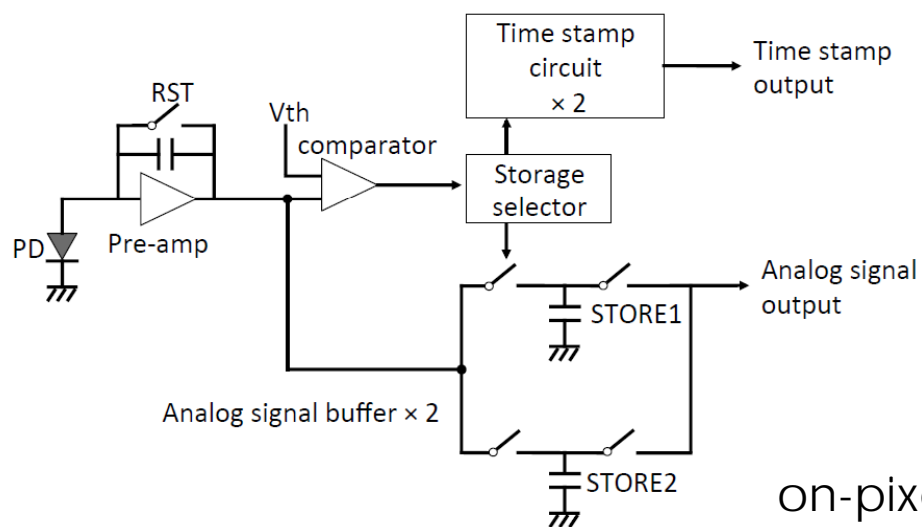
V_t of gate edges is not controlled by V_g due to hole accumulation in spacer

SOFIST (SOI sensor for fine measurement of Space and Time)

Ono(阪大)



demonstrator chip for ILC



日本物理学会誌

- 高エネルギー宇宙線観測と宇宙暗黒物質探索
- 微分方程式の縮約と包絡線
- SOI 技術を用いた放射線イメージセンサーの開発

BUTSURI

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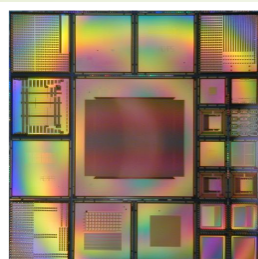
2010 VOL. 65 NO.

9



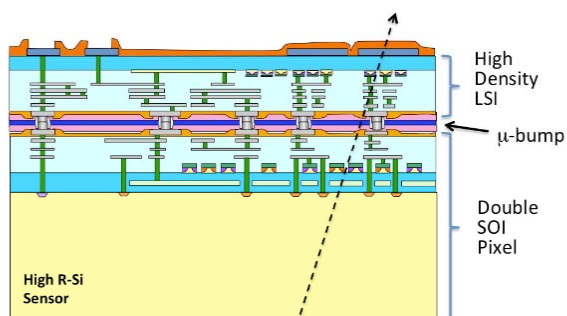
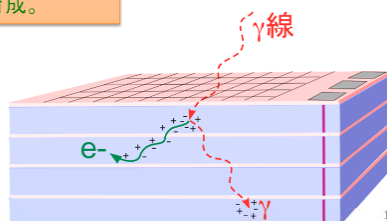
A01: 3次元ピクセル・プロセス開発

- SOI量子イメージングプロセスの性能向上。
- 高放射線耐性構造、高集積化、大面積化へ向けた研究。
- Si貫通ビアによる多層検出器の実現に向けた研究開発。
- SOI技術を発展させ、積層回路を実現する3次元回路実装技術の研究。
- 相乗りプロセス(MPW)の主催。
- 他研究班へのアドバイス、人材育成。



MPWランのマスク

多層SOI検出器のイメージ:
放射線による相互作用の素過程を全て検出し、新たな測定手法の提案を行う。



A02班: SOI技術を用いた極低ノイズ・高速イメージングデバイスの研究

B01班: 宇宙最初期ブラックホールの探査研究を実現する衛星搭載X線精密イメージングの開拓

B02班: 「ダストに隠された宇宙の物質進化を暴く 極低温SOI赤外線イメージングの開拓」

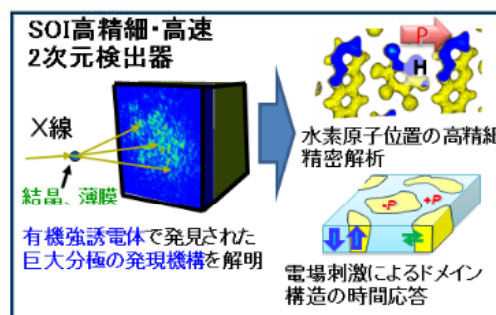
C01班: 高輝度加速器実験のための素粒子イメージング

C02班: X線自由電子レーザー(XFEL)による超高速ナノ構造解析用検出器

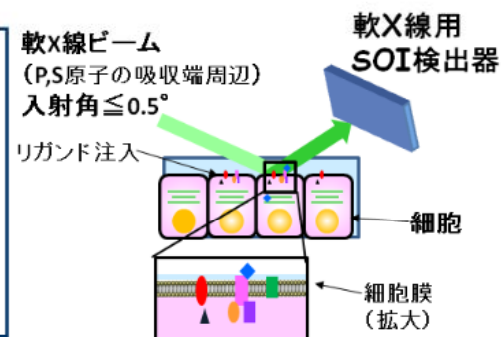
D01: 放射光を用いた空間階層構造とダイナミクス研究のためのイメージング

構造の空間・時間変化を精密に捕らえるため、高精細(30 μ mピクセル)・高速(1マイクロ秒毎に動的撮影)・高感度(軟X線)のX線検出器を開発する。

先端的機能性物質(有機強誘電体)の研究



細胞膜近傍の構造変化を捉える



D02班: 投影型イメージング質量分析による迅速で高解像度な生体内分子イメージング

まとめ

SOI Pixelの開発を初めて10年が経過

新学術科研費 進行中 2013-17

放射線耐性評価を主導的に

TID効果による限界： 数kGy

DSOIの導入 >100kGy

LDD調整 ~MG y (評価中)

FPIXの設計・製作 (最小ピクセルサイズ 8um角)

ILC用のSOFIST開発中

卒業論文	Master	Senior
2014	本多	青柳、関川、Subedi
2013		浅野、前田、飛田
2012	石橋	本多
2011	新庄	堀内、山田
2009	河内山、瀬賀	小池、新庄
2007	望月	河内山、瀬賀