



TCHoU DPPD workshop 2022





DEVELOPMENT OF FOCAL-E ELECTRONICS PROTOTYPE IN ALICE

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On the behalf of FoCal team

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Personal Introduction







Case of study: Hadrontherapy



The position of the Bragg peak can be controlled

The use of the spread-out Bragg peak



The impact of uncertainties on the dose deposit





Case of study: Hadrontherapy





The demonstrator must meet the following specifications:

- A temporal resolution less than 100 ps;
- An overall count rate that can reach the 100 MHz;
- A very high resistance to radiation;
- A very wide dynamic range (a single 250 MeV proton to 60 MeV proton packets);



Subject: Design of a continuous time Delta-Sigma modulator for energy measurement using diamond detectors





Results for the time measurement system





Developed 8 channels ASIC and its testing setup



Results for the time measurement system



Precision of the proposed model

Performance of the TIA



Results for the energy measurement system (ADC)



Exploring the use of the model based design approach



Results for the energy measurement system (ADC)



Doing analog-to-digital conversion as early as possible







"Cascaded Resonators Feedforward" or CRFF topology

Results for the energy measurement system (ADC)

Parameter	Achieved
Technology	CMOS 130 nm
Architecture	5^{th} order CT LP CRFF $\Delta\Sigma$
Sampling frequency	160 <i>MHz</i>
Signal bandwidth	10 <i>MHz</i>
MSA voltage	$-3.5 dBFS/1.2 V_{p-p}$ (differential)
SNR	51.4 <i>dB</i>
ENOB at MSA	8.3 <i>bits</i>
DR	56 <i>dB</i>
Power supply	1.2 V
Power consumption	39.43 mW

Block	power consumption details (mW)	Total (mW)
Loop filter	5×4.4	22
Summing block	1×14	14
Loop ADC	7×0.47	3.3
feedback DAC	1×0.04	0.04
TOTAL		39,34

Simulated modulator performance

Power consumption estimation 11

List of publications:

- [1] Abderrahmane Ghimouz et al. "A Preamplifier-discriminator circuit based on a Common Gate Feedforward TIA for fast time measurements using diamond detectors." In: 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS). 2018, pp. 281–284. DOI: 10.1109/ICECS.2018.8617950.
- [2] Abderrahmane Ghimouz, et al. "Systematic high-level design of a fifth order Continuous-Time CRFF Delta Sigma ADC." In: 2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS). 2021, pp. 1–4. DOI: 10.1109/LASCAS51355.2021.9459156.
- [3] Abderrahmane Ghimouz, et al. "Designing Opamp amplifiers for a 5th order CT CRFF DS ADC using Model-based design paradigm and gm/ID methodology." In: International Conference on Analog VLSI Circuits 2021.
- [4] Abderrahmane Ghimouz et al. "A multichannel front-end electronics ASIC for high-accuracy time measurements using diamond detectors." In: International Conference on Analog VLSI Circuits 2021.
- [5] Abderrahmane Ghimouz, et al. "New Design Approach of Front-End Electronics for high Accuracy Time Measurement Systems." In: 2021 28th IEEE International Conference on Electronics, Circuits and Systems (ICECS). 2021, pp. 1-4, DOI: 10.1109/ICECS53924.2021.9665533.
- [6] Abderrahmane Ghimouz, et al. "DIAMASIC: A multichannel front-end electronics for high accuracy time measurements for diamond detectors." In: TWEPP 2021 Topical Workshop on Electronics for Particle Physics. 2021

FoCal Project

FoCal-H

Main physics goal: Nucleus structure at small -x

System composition:

- FoCal-E: high-granularity Si-W sampling sandwich calorimeter for photons and π^0
 - **FoCal-H**: conventional metal-scintillator sampling calorimeter for photon isolation and jets

FoCal-E Detector

System design: Two readout granularities

- **PAD (LG) layers:** granularity 1x1 cm2, analog readout
- **PIXEL (HG) layers:** 30x30 µm2 digital readout (ALIPIDE)

Challenge:

• **Separate** γ/π^0 at high energy

FoCal–E Detector

Each module:

- 18 PAD (LG) layers with 5 aggregators boards
- 2 PIXEL (HG) layers with individual readout

- **Final structure:**
- 22 Modules

FoCal-E Detector

FoCal–E Demostrator

Final module:

- 18 5-pad layer boards (90 HGCROC with 6480 channels)
- 5 Aggregator board

Demonstrator module:

- 18 single pad board (18 HGCROC with 1296 channels)
- 1 Aggregator board

PHASE 1: Selection of the good HGCROC circuits

HGCROC TEST SUMMARY

■ Good ■ One channel issues ■ Multiple channel issues ■ Bad

PHASE 2: Characterizing E-PAD V1 and V2

Evaluating the parameters of the ADC, ToA and ToT and the noise associated to them

PHASE 2: Characterizing E-PAD V1 and V2

Test under HV

PHASE 3: Correcting the GND issue

SPS September 2021

LPSC Grenoble November 2021

Reproduction of the issue in Lab

PHASE 3: Correcting the GND issue

Solution for the E-PAD V1

PHASE 3: Correcting the GND issue

Designing a solution for the E-PAD V2

Conclusion

- A fully functional prototype of a demonstrator for FoCal-E is under development
- New calibration algorithms are optimized
- A cosmic test setup is build and will be used soon
- New beam tests of the prototype are planned (Japan, CERN)

Conclusion

Thank you for your attention

ご清聴ありがとうございました