Development of ATLAS Pixel Detector for the HL-LHC

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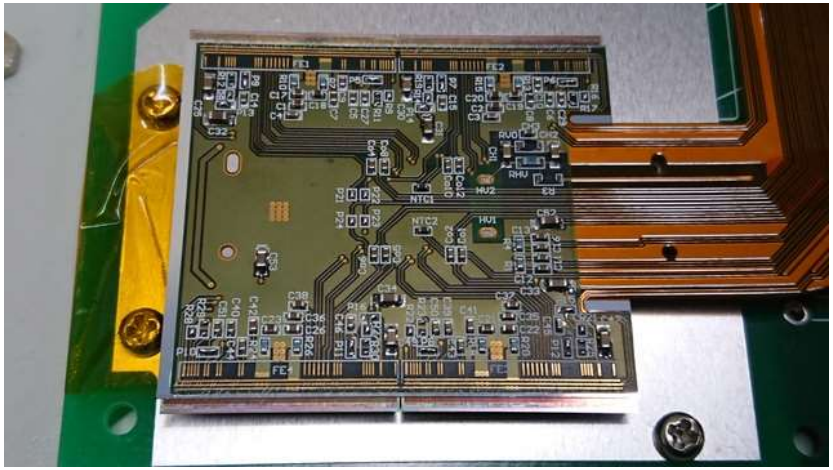
TCHOU SYMPOSIUM

Overview

- Introduction
  - High luminosity LHC
  - Radiation damage in silicon detectors
- New Pixel detector for HL-LHC
  - Detectors for HL-LHC
  - Planner pixel sensor
  - Biasing structure
- Summary



Introduction

High Luminosity LHC (2026)

- Instantaneous luminosity : 7.5×10^{34} $cm^{-2}s^{-1}$
- Integrated luminosity : 3000 fb^{-1}
- Radiation damage : 1×10^{16} 1MeV $n_{eq}cm^{-2}$
- Number of interaction : ~200 per crossing

➡ Increase Radiation damage and Pile-up

How can we maintain physics performances?

- Radiation Tolerance
- Fine Pixel
- High speed readout

} New Silicon Tracker (ITk Pixel and ITk Strip)

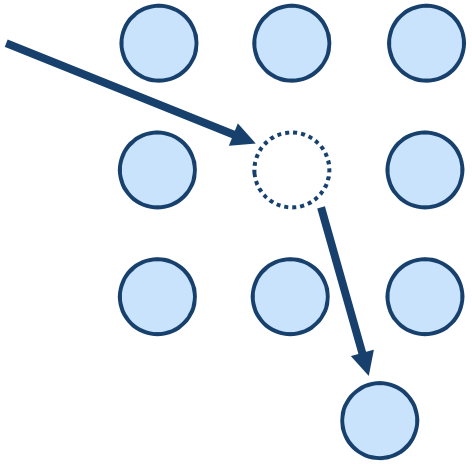
- Trigger logic upgrade

are needed.

Radiation damage in Si detectors

- **Bulk damage**
  - Main effect for Si sensors
  - Collision with particles make defects

  → Many exogenous level will be created

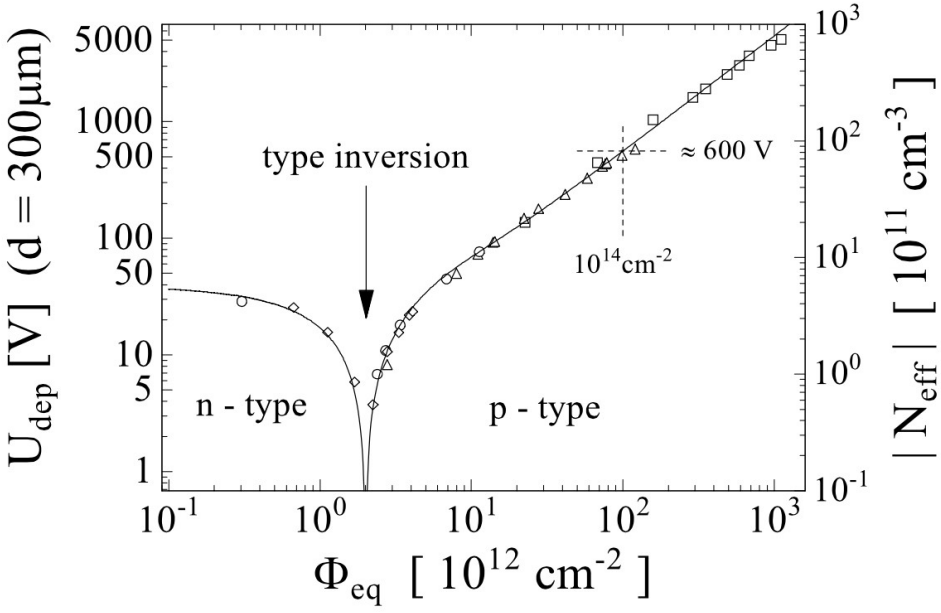


- **Defect's effect**
  - Increase p-type impurity

  → Higher depletion voltage
  - Recombination center

  → Noise, leakage current
  - Trapping center

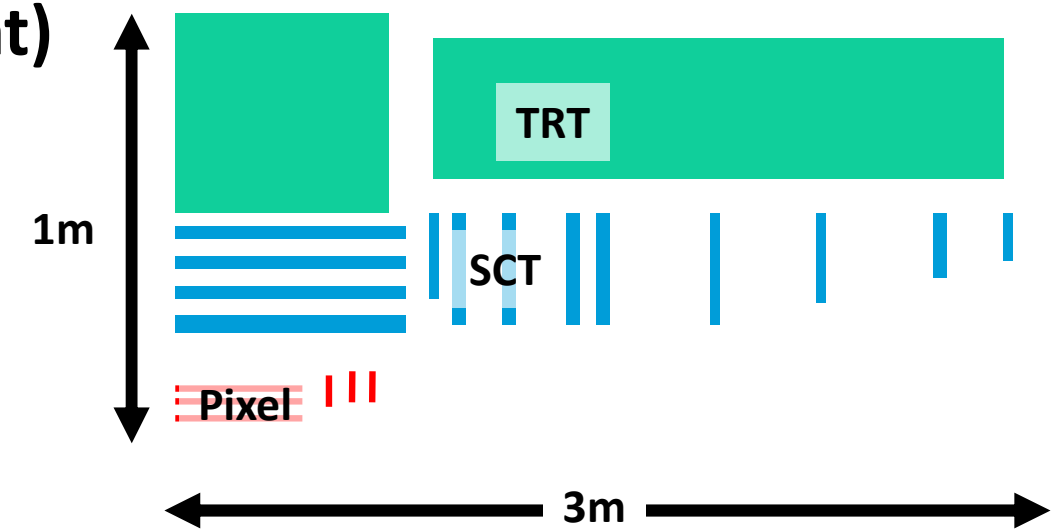
  → Charge Collection Efficiency



Detectors for HL-LHC

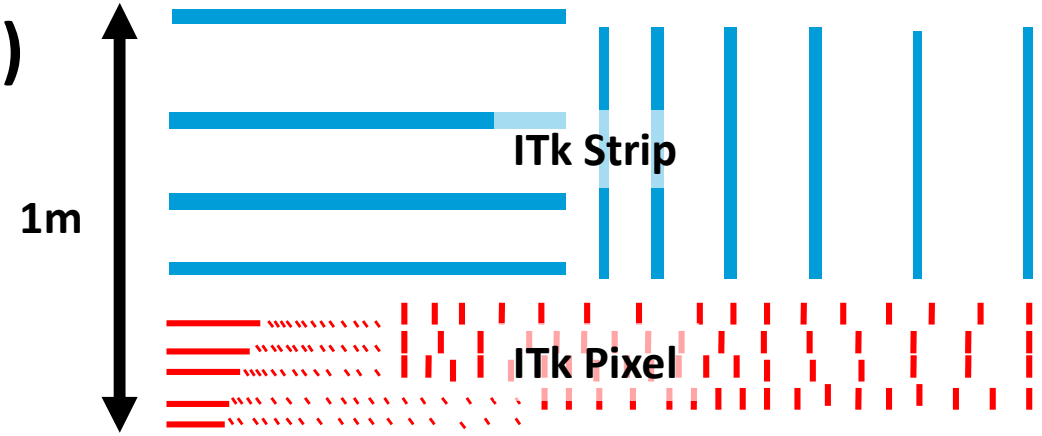
Inner Detector (current)

- Detector is composed of
  - ✓ Pixel
  - ✓ SCT
  - } Silicon
  - ✓ TRT
  - } Gas
- Silicon area : ~65m^2
- Channel : ~100M



Inner Tracker (upgrade)

- Detector is composed of
  - ✓ ITk Pixel
  - ✓ ITk Strip
  - } All Silicon
- Silicon area : ~200m^2
- Channel : ~5G

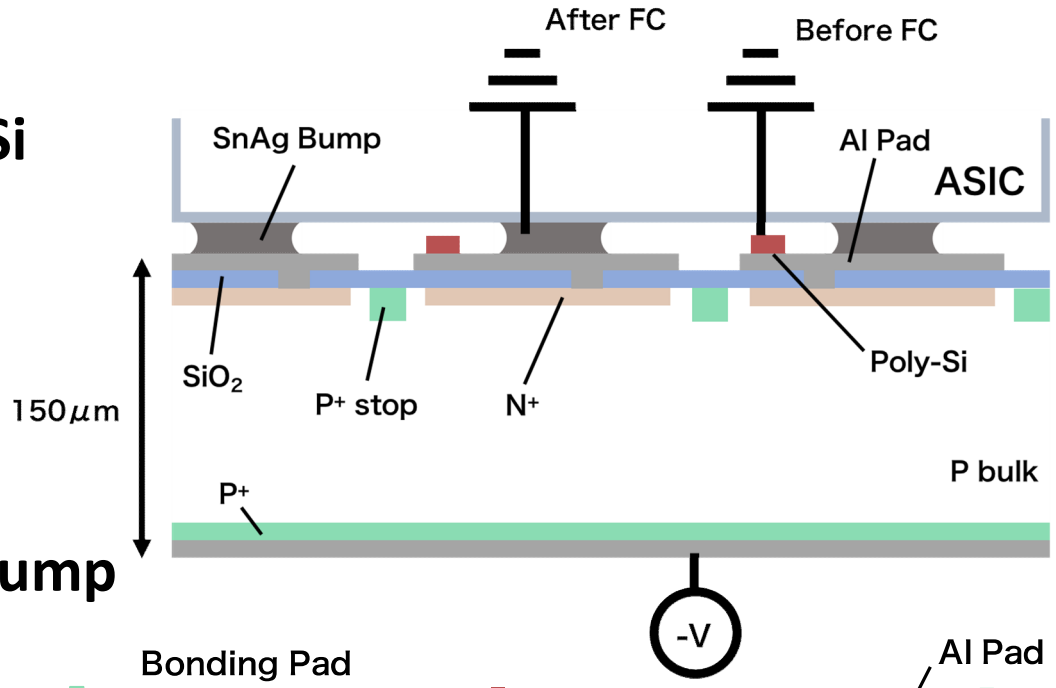


Cost is very important point

Planner Pixel Sensor

n^+-in-p pixel sensor

- Implanting n^+ into p-type Si
- Lower costs
- Radiation tolerance up to ~3×10^{15} 1MeV $n_{eq}cm^{-2}$
- No type inversion
- Bond to ASIC with metal bump



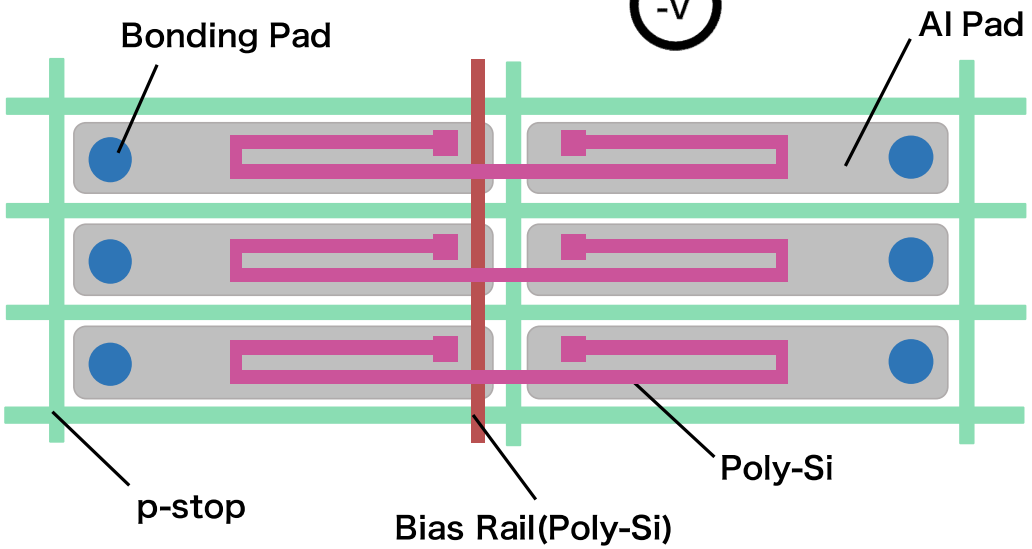
Device structure

- Pixel Size

→ 50 × 50 or 25 × 100 μm²

→ One of the most smallest planner hybrid sensor

- Biasing Structure



Biasing structures

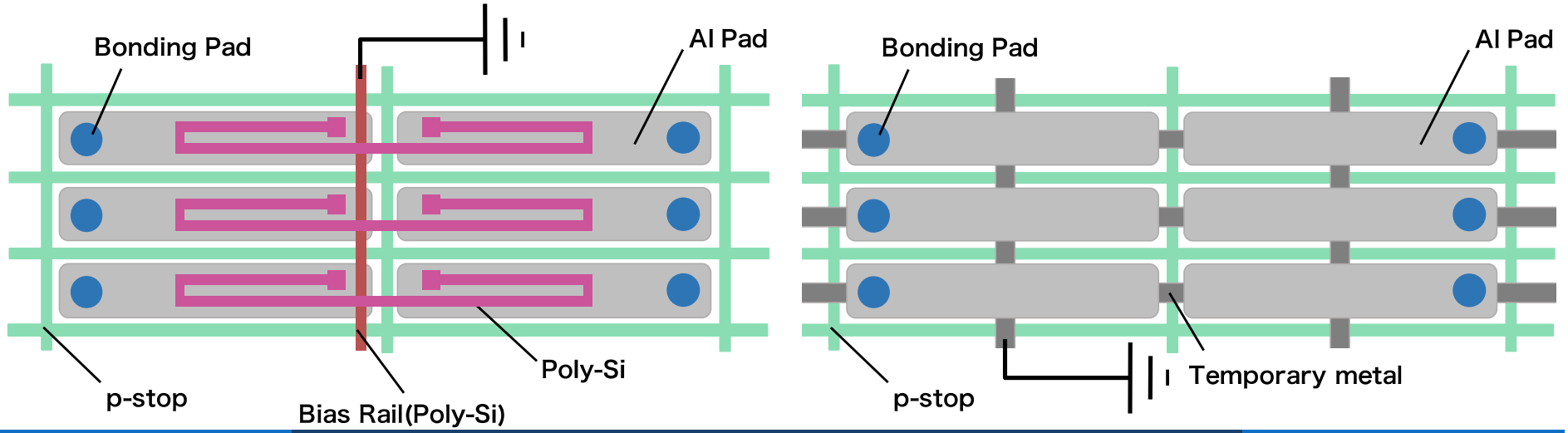
IV-testing before bump-bonding

- Cost of bump-bonding is quite high (accounted for ~50%)
- IV-testing before bump-bonding is important for good yield

→ Need to set all pixel GND for biasing

How can we do? - two choices

- Temporary metal : Metal structure (will be etching), high costs
- Bias rail : High resistivity Poly-Si rail, radiation damage issue



Bias rail structure

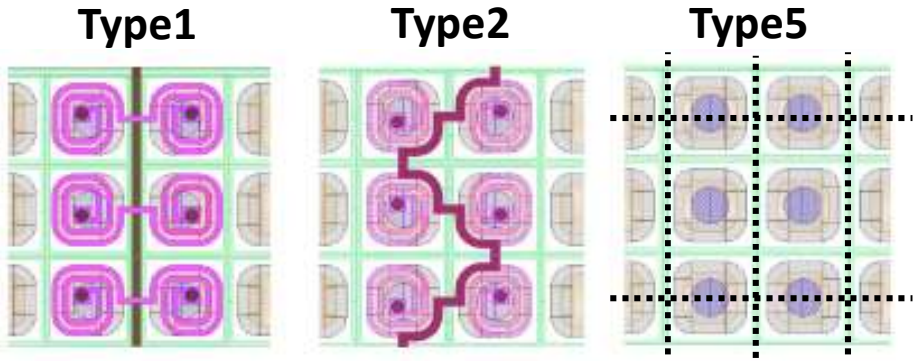
Efficiency drop after irradiation

- Typical efficiency drop observed at under biasing structure

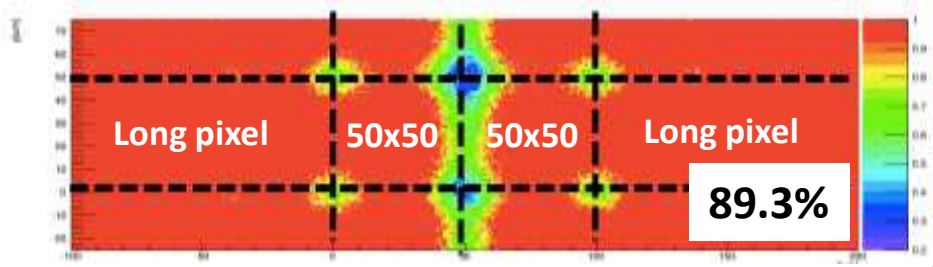
→ Changing concentrations of impurity and charge collection field

→ Some carrier induced on biasing structure (not electrode)

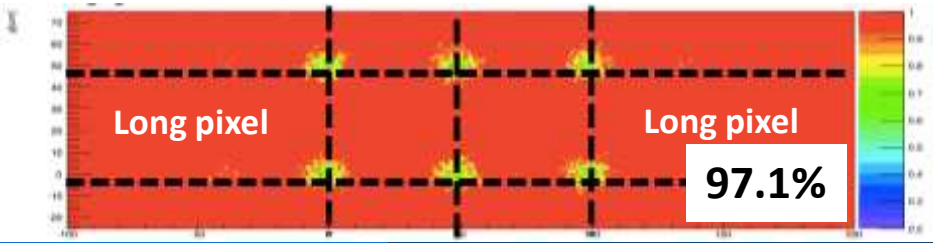
- Succeed to reduce efficiency drop by "Offset structure"



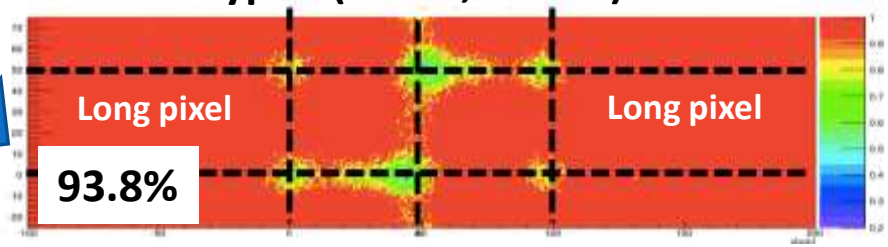
Type1 (no offset, 1000V)



Type5 (no structure, 1000V)



Type2 (offset, 1000V)



Efficiency value is improved by 4% !!

Summary

Development of ATLAS pixel detector

- ATLAS Inner detectors will be replaced with new silicon detectors for higher luminosity experiment.
  Need to maintain physics performance in high luminosity environment.
- We are developing finer pixel, with lower cost and higher radiation tolerance detector.
- Low cost can be materialized by IV-testing before bump-bonding.
- Biasing structures are needed. Efficiency drop of 3%(no-bias), 4%(with bias structure) is observed after irradiation.