# Radiation Resistance of SOI Pixel Devices Fabricated with OKI 0.15μm FD-SOI Technology

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*Abstract*–**Silicon-on-insulator (SOI) technology is being investigated for monolithic pixel device fabrication. The SOI wafers by UNIBOND allow the silicon resistivity to be optimized separately for the electronics and detector parts. We have fabricated pixel detectors using fully depleted SOI (FD-SOI) technology provided by OKI Semiconductor Co. Ltd. The first pixel devices consisting of 32×32 pixels each with 20 μm square were irradiated with $^{60}$Co γ's up to 0.60 MGy and with 70-MeV protons up to $1.3\times10^{16}$ 1-MeV $n_{eq}/cm^2$. The performance characterization was made on the electronics part and as a general detector from the response to RESET signals and to laser. The electronics operation was affected by radiation-induced charge accumulation in the oxide layers. Detailed evaluation using transistor test structures was separately carried out with covering a wider range of radiation level (0.12 kGy to 5.1 MGy) with $^{60}$Co γ's.**

## I. Introduction

MONOLITHIC pixel devices are an ultimate dream for physicists who require devices with large number of readout channels with fine segmentation though at small cost. In fact, in recent experiments, pixel-type particle detectors are required to be finely segmented and highly integrated to cope with high density particle flux generated in the luminous particle collisions. The pixel devices, such as for the LHC experiments, are based on bump bonding of the detector elements to their readout electronics. This procedure is becoming delicate and costly with increasing number of channels. The device thickness remains also an issue in view of material budget. Pixel devices utilizing UNIBOND™ [1] silicon-on-insulator (SOI) wafers can potentially solve such difficulties. Most important is that the silicon resistivity can be optimized separately for the readout electronics and SOI "handle wafer" which we adopt as the sensitive part. We are developing pixel devices [2] using 0.15-0.20 μm fully depleted SOI (FD-SOI) CMOS process provided by OKI Semiconductor Co. Ltd. The first monolithic pixel device, named TOPPIX [2], was fabricated in 2006, composed of 32×32 pixels each with 20 μm square.

Since the SOI silicon layer is substantially thin relative to bulk CMOS and fully covered by oxide, the device is less sensitive to ion strikes providing immunity to latch-up. On the other hand, the charge build-up in the buried oxide (BOX) layer and at the BOX interface is a significant issue for the total ionization dose (TID) effects in SOI devices [3]. The TID effects should present as threshold voltage shifts and increase in the leakage current. We have irradiated TOPPIX devices with $^{60}$Co γ's and 70 MeV protons. TrTEG chips [3] consisting of an array of PMOS and NMOS transistors with various L/W ratios were also irradiated to evaluate the TID effects in the basic transistor characteristics.

## II. TOPPIX and TrTEG

Three types of transistors are available in the OKI 0.15 μm FD-SOI process: low threshold voltage transistors (LVT) and high threshold voltage transistors (HVT) for core circuits both with a 2.5 nm thick gate oxide layer, and I/O transistors (IO) with a 5.0 nm thick gate oxide layer. The SOI wafers are 150 mm in diameter and 650 μm in thickness. The wafer is composed of 40 nm thick p-type SOI silicon of 18 Ωcm and n-type substrate of 700 Ωcm, separated by a 200 nm thick BOX layer. After the topside process is completed, the backside of the wafer was ground down mechanically to 350 μm thickness, and then plated with 200 nm of aluminum. The backside can be used for back gate biasing. There are two types of body control transistors, body floating and body tied. In the body-tied configuration, the body is connected at regular intervals with the source externally in the metal layer; there are five metal and one poly-silicon layers available on top of the SOI transistors.

The TOPPIX chip is 2.4 mm square in size. The analog readout chain on each pixel consists of eight HVT body-tied FETs, one functioning as input protection diode, as shown in Fig. 1. The reset voltage $V_{RST}$ is provided externally, thus the response to varied $V_{RST}$ can test the individual pixel readout chain. "$V_{RST}$ response" refers to this test in this paper. Reset switching signal (rst), row/column selections, and other commands are provided by IO transistors located surrounding the pixels at center. The selected analog output is recorded by

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a digital oscilloscope. The entire electronics part is surrounded by bias (at ground) and guard (floating) rings. At the edge region, an $N_{sub}$ ring (HV ring) is located allowing to bias from the topside to the n substrate.

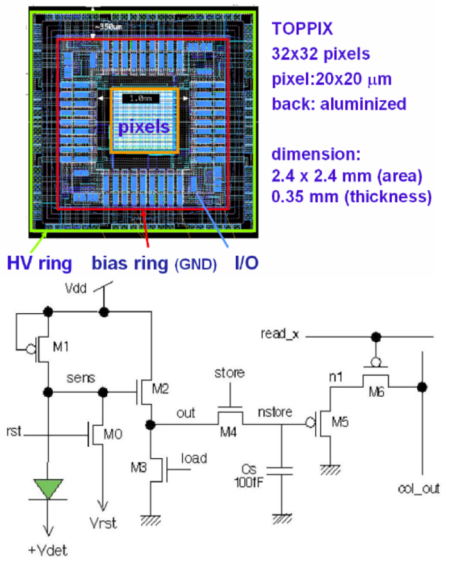


Fig. 1. Schematics of the TOPPIX chip and a readout chain on one pixel.

The TrTEG chip consists of 16 NMOS and 16 PMOS transistors. With fixing the W/L ratio to 2000, we chose two to four length combinations for each transistor type and body control. The selected 16 parameters are listed in Table I. The shortest gate length for LVT and HVT transistors is 0.14 μm, and that for IO is 0.3 μm.

TABLE I
16 TRTEG TRANSISTORS SHOWING TYPES, TYPICAL THRESHOLD VOLTAGES, W/L SIZES (IN MICRONS) AND BODY CONTROLS, (F) FLOATING OR (BT) BODY TIE.

| W/L | 280/0.14 | 400/0.20 | 600/0.30 | 1000/0.50 |
|---|---|---|---|---|
| LVT (0.2V) | F, BT | BT | F, BT | BT |
| HVT (0.4V) | F, BT | BT | F, BT | BT |
| IO (0.5V) | | | F, BT | F, BT |

## III. IRRADIATION

The proton irradiation was carried out at Cyclotron and Radioisotope Center (CYRIC), Tohoku University. Details of irradiation and fluence calibration are described elsewhere [3]. The fluence target was taken from the radiation level at the super LHC [4], where $10^{16}$ 1-MeV $n_{eq}/cm^2$ is the expectation at the pixel detector. Two TOPPIX chips were irradiated to $1.4\times10^{15}$ and $1.3\times10^{16}$ 1-MeV $n_{eq}/cm^2$.

The irradiation with $^{60}$Co γ's was performed at Takasaki Institute of Japan Atomic Energy Agency. Three TOPPIX chips were irradiated to 0.12 kGy to 0.60 MGy at 1-5 kGy/h. providing data at six dose values (dosage was added after characterization measurements were made). Fifteen TrTEG chips were irradiated each to 0.01 kGy to 5.1 MGy at 0.2-20 kGy/h. Alanine rod dosimeters Aminogray™, available from Hitachi Cable, Ltd., were attached to several samples to examine the dose calibration. The absorbed dose is derived from the yield of radiation induced stable radicals in alanine, which is measured using ESR spectroscopy. The measured values agreed with the doses provided by the facility to 10%: there was a massive sample of other user next to our samples. We assign an uncertainty of 10% to the dose. In the exposure, the samples were kept at room temperature with their terminals shorted using conductive sponge.

In comparing the TID for 70-MeV protons with $^{60}$Co γ's, the absorbed dose to $SiO_2$ is 8.4 MGy ($SiO_2$) for the proton fluence corresponding to $1\times10^{16}$ 1-MeV $n_{eq}/cm^2$.

## IV. TOPPIX γ-IRRADIATION RESULTS

The primary goal of TOPPIX irradiation is to examine the functionality of the electronics part and as a particle detector. The $V_{RST}$ response, I-V characteristics, and response to laser were measured for this purpose. While the laser test was made after completion of irradiation, the other two were measured between irradiations. The irradiated chips were placed at 60°C for 20 min before starting the evaluation to promote quick recovery (annealing) from the extra damage caused by irradiation at accelerated rate. The annealing time was shortened from the recommended duration, 80 min at 60°C, since the majority of the annealing should complete in 20 min. At some dose points, we obtained the data right after the irradiation was completed and evaluated the effect of annealing.

### *A. I-V characteristics*

Fig. 2 shows the I-V characteristics of one of the TOPPIX chips irradiated up to 0.60 MGy. The leakage current refers to the total detector current when the reverse bias was applied to the detector back with the bias ring grounded, measured at room temperature. Plotted are the data taken after 1.1, 66, and 596 kGy, and before irradiation. For the two dose points, I-V curves measured immediately after the irradiation are also plotted. The leakage current at biases below 50 V tends to decrease with radiation. This can be explained by the PMOS transistor threshold shift, described later, suggesting the leakage current through the pixels only should decrease with the dose.

The breakdown voltages, defined as the bias where the leakage exceeds 1 μA, are summarized in Fig, 3 for all the three chips. The annealing contribution is moderate as the breakdown voltage is shifted by approximately 5 V only. Although the individual difference may be large, the breakdown voltage tends to decrease with the dose. This can

be seen also in Fig. 2 where the slope of the curves becomes steeper with radiation.

Abrupt leakage current increases are often caused by avalanche multiplication due to local high electric field. We can localize such points, "hot spots", by detecting associated infrared lights with a cooled infrared sensitive CCD camera. We identified that the breakdown is located at the corners of the bias ring both for pre and post irradiated samples. Since the bias ring is p-implanted ($P_{SUB}$) against the n-bulk, the field is largest especially around the corners. The ions trapped in the BOX generate additional field lines to the $P_{SUB}$ implant and hence lower the breakdown voltage.

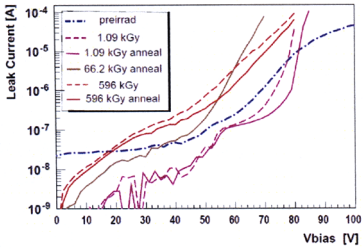


Fig. 2. Leakage current of TOPPIX chip3 as a function of the detector bias. The data right after the irradiation are shown in dashed curves.

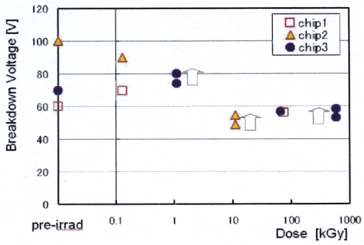


Fig. 3. Breakdown voltages of TOPPIX chips as a function of dose. The marks correspond to the chip number 1 to 3. The two same marks at the same dose points are the data before and after annealing with the arrows showing the chorological order.

### B. $V_{RST}$ response

The $V_{RST}$ response was measured for a $V_{RST}$ range from 0 to 1 V at a 0.1 V step, with changing the bias up to 20 V at a step of 1 V. The electronics working range is influenced by biasing since the bias voltage couples to the electronics via BOX layer, known as a back-gate effect.

Fig. 4 shows the $V_{RST}$ response of chip 3 before and after 0.60 MGy irradiation. The output voltage should increase linearly with $V_{RST}$ in optimum region. Although modified by irradiation, there remain conditions where the electronics is functioning properly. The tendency is that the working region is shifted to lower biases with irradiation. This is explained by threshold voltage shifts, as discussed later. To numerate the functionality of individual pixel channels, we chose the ranges of $V_{RST}$ (0.4:0.7 V, 9V bias) and (0.3:0.6 V, 0V bias) for the data before and after 0.60 MGy irradiation, respectively, where the first:second values in parentheses are the two reference $V_{RST}$ values to calculate the slope

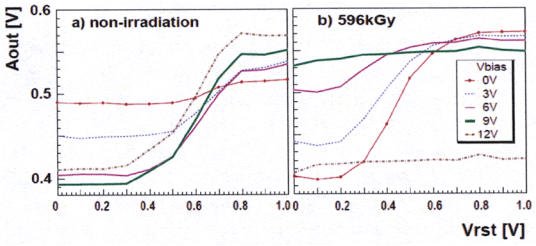


Fig. 4. TOPPIX output voltage averaged over 1024 channels as a function of $V_{RST}$ for (a) before and (b) after 0.60 MGy irradiation. The curves are shown for selected bias settings up to 12 V.

Histograming the slopes provides a clear separation of sick channels against genuine ones. For chip 3 in Fig. 4, the number identified as dead is 16 pixels both before and after irradiation with their location unchanged. We conclude that no dead channel is created up to 0.6 MGy we tested. Note that the fraction of dead pixels has been significantly reduced to a 0.1% level in the 2007 fabrication.

### C. Laser response

The TOPPIX chips have a window on each pixel to allow testing the functionality as a photon detector. We injected continuous 670 nm laser over the entire device face. The output voltage differences between laser on and off were histogrammed to judge abnormal channels. The histogram shown in Fig. 5 is TOPPIX laser response after 0.60 MGy with a bias of 1 V. The 16 abnormal channels found in the $V_{RST}$ response measurement are clustered in the low response group. Additionally one channel is found dead near the arrow. This channel is leaky giving a large OFF signal and could not detected in the $V_{RST}$ response measurement. We conclude that no defect channels are created by irradiation.

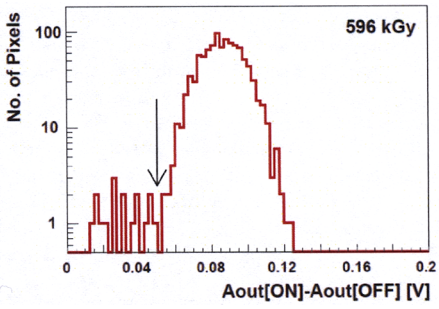


Fig. 5. Histogram of response differences with laser on and off for TOPPIX irradiated to 0.6 MGy.

## V. TOPPIX PROTON IRRADIATION RESULTS

Two TOPPIX chips were irradiated with protons up to $1.3\times10^{16}$ 1-MeV $n_{eq}/cm^2$ to investigate the radiation effects to

the substrate. The electronics damage that is caused by 70-MeV protons and by $^{60}$Co γ's is also to be compared.

### *A. I-V characteristics*

Fig. 6 plots the I-V curves for the two TOPPIX samples. The curves obtained at pre-irradiation are identical irrespective whether the bias is provided through the HV ring in front or from the backside. However, the I-V curves of proton irradiated samples turn different as plotted in the figure. The I-V characteristics is moderated if biased from the HV ring. This is explained by the radiation induced bulk damages that effectively increase the silicon ohmic resistance. The backside potential is dropped accordingly by the voltage drop through. The drop is larger with increasing the leakage current.

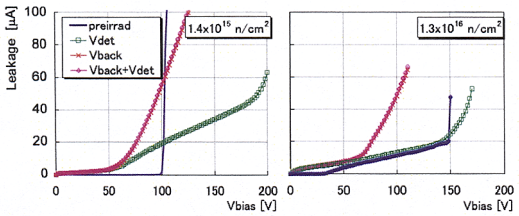


Fig. 6. I-V curves of TOPPIX samples irradiated to protons of (left) 1.4 $\times 10^{15}$ $n_{eq}/cm^2$ and (right) $1.3\times10^{16}$ $n_{eq}/cm^2$, overplayed with pre-irradiation curve. The data are shown when biased through the HV ring (**Vdet**) and from the backside (**Vback**). The curves biased from both and **Vback** only are overlapped each other.

We observed that pre-irradiation samples exhibit hot spots always at the corners of the bias ring, as described previously. For the irradiated samples, the hot locations are characteristic depending on the characteristics of the I-V curves. On the steepest I-**Vdet** curves (at 210 V and 170 V for 1.4 $\times 10^{15}$ and $1.3\times10^{16}$ $n_{eq}/cm^2$ samples, respectively), hot spots are observed around the HV ring (see Fig. 7 left). On the second steepest I-**Vdet** curves or on the steeper I-**Vback** curves, hot spots are seen at the corners of bias ring, similar to non-irradiated samples, but only for the 1.4 $\times 10^{15}$ $n_{eq}/cm^2$ sample (see Fig. 7 right). This supports that the n-bulk is not inverted up to this fluence, which is also confirmed from the laser response described below.

The $1.3\times10^{16}$ $n_{eq}/cm^2$ sample had an early leakage current increase for bias between 40 and 150 V since pre-irradiation. The hot spots could not be identified with the CCD camera, probably because infrared emission is not strong enough for such a slow increase. Judging from the forward bias I-V behavior in the negative voltage side, the bulk of this sample seems to stay un-inverted. Conclusive result could not be derived from the laser response, since this device did not respond properly to laser as explained by that the electronics was radiation damaged.

It is reported [5] that n-type MCZ wafers, which we use for the detector, will not invert up to proton fluence of $3.4\times10^{15}$ 1-MeV $n/cm^2$ they tested. The type inversion of n-type FZ wafers after a few $\times$ $10^{13}$ $/cm^2$ [6] is established. The present observation is not inconsistent with [5].

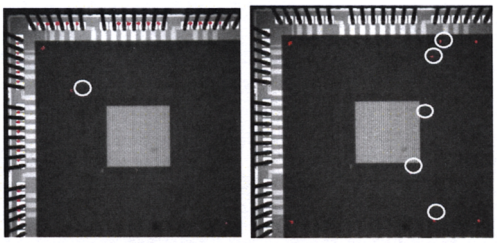

Fig. 7. Hot spots observed on the sample irradiated to $1.4\times10^{15}$ $n_{eq}/cm^2$ measured at (left) **Vdet**=210 V and (right) **Vdet**=150 V. The spots with circle are confirmed to be noise.

### *B. $V_{RST}$ response*

As observed in the γ irradiation, the $V_{RST}$ response is affected also by proton irradiation. Figure 8 shows the $V_{RST}$ response for selected bias values. The electronics working region became narrow at $1.4\times10^{15}$ $n_{eq}/cm^2$, and disappeared at $1.3\times10^{16}$ $n_{eq}/cm^2$. The reset is not properly transferred. This is most probably caused by damage in the IO transistors, since the IO transistor threshold shift is substantial (see Sec. V).

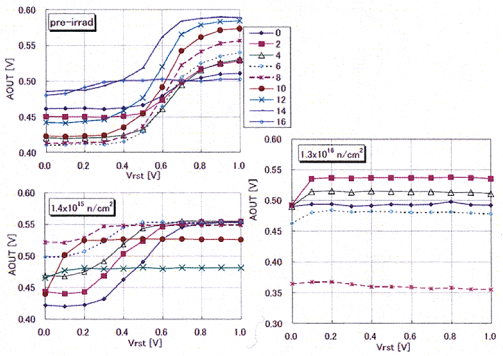


Fig. 8. $V_{RST}$ response for the pre- and two proton irradiated samples. The curves are shown for selected Vback values.

### *C. Laser response.*

The TOPPIX chip irradiated to $1.4\times10^{15}$ $n_{eq}/cm^2$ is examined for the laser response since we observed that the electronics is working. Figure 9 shows the response of three consecutive pixel signals to laser ON and OFF. The readout channels are switched every 64 μs. The signal shape is characteristic showing the output corresponding to the reset voltage, followed by accumulation of charge. The irradiated sample exhibits substantial contributions from the leakage, but the response to laser is obviously seen. A mask pattern was properly reproduced. The measurement was made at room temperature.

The dead channels were evaluated by laser injection while the chip was cooled to 11°C to reduce the noise contribution. There was no new dead channel created from the proton irradiation.

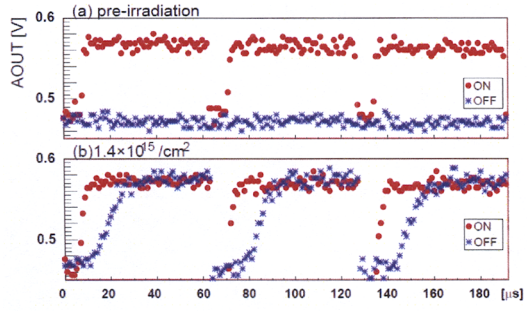


Fig. 9. Response to laser ON (red) and OFF (blue) for (a) pre-irradiation and (b) after $1.4\times10^{15}$ 1-MeV $n_{eq}/cm^2$, with bias at 2 V.

## VI. TrTEG Results

Radiation effects in transistor characteristics were evaluated independently in the TrTEG chips by measuring the drain current as a function of the gate-source voltage $V_{GS}$. The drain-source voltage $V_{DS}$ was fixed at 0.5 V and –0.5 V for NMOS and PMOS transistors, respectively. The results obtained from proton irradiation are already reported in [3].

### A. Leakage Current

Figure 10 shows the leakage current defined as $I_D$ at $V_{GS}$ =0 for the transistors with shortest gate lengths (see Table I). As the threshold voltage shifts negatively to compensate the positive charges trapped in the gate oxide, the leakage current increases with dose for NMOS. The effect is opposite for PMOS resulting that the dose dependence is small.

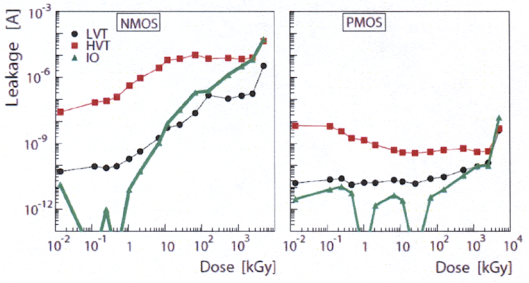


Fig. 10. Leakage current $I_D$ defined at $V_{GS}$ =0 as a function of dose, shown for three transistor types with the shortest gate lengths. The uncertainty dominates the measured values below $10^{-11}$ A.

### B. Threshold voltage shift

The radiation induced threshold voltage shift is well studied [7] for bulk CMOS devices. The shift is explained by interplay of holes trapped in the gate oxide and the charges created at the oxide-silicon interface. The charge state of interface traps is negative at the p-type silicon to oxide interface (NMOS) and positive at n-type (PMOS). The contributions from the BOX layer need to be considered in addition for the SOI devices, especially for FD-SOI, where the larger coupling should make the transistors much sensitive to the BOX charge trapping [8]. The hole trapping and interface charge creation should also be affected by manufacturing processing techniques and wafer quality.

Figure 11 shows the radiation induced shifts of the threshold voltage $V_T$, $V_T$ defined as $V_{GS}$ where $I_D$ =0.5 mA. The data are for the transistors with the shortest gate lengths and body-floating. Since the holes are the main contributor, the shifts are negative for both PMOS and NMOS. The data obtained from the proton irradiation are compared. The both sets of data are in reasonable agreement. The shifts are different among LVT, HVT and IO, resulting larger shifts for IO transistors with thicker gate oxide. The positive charges in the gate oxide are considered to act as the primary contributor for the threshold shifts.

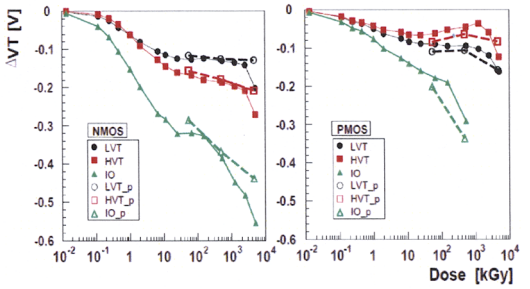


Fig. 11. Dose dependence of the threshold voltage shift for NMOS and PMOS transistors. The transistors are with the smallest gate length and body floating (see Table I). Open marks are the data obtained from proton irradiation.

For bulk CMOS, the absolute voltage shift for NMOS becomes smaller with dose, since the contribution of the negative interface traps increases with dose to cancel the positive charges in the oxide. The present data, especially for the larger threshold HVT and IO, show an opposite tendency. The difference should be attributed to the charge creation at the BOX interface. This contribution should be larger in FD-SOI and numerical evaluation to breakdown the contribution is underway.

The body tie effects are expected to be not substantial in FD-SOI. The measured shifts are typically larger in magnitude by 10 mV for body tied samples than body floating. The difference is smaller at lower doses.

### C. Gate length dependence

The threshold shifts are plotted in Fig. 11 as a function of gate length. The graphs are given for two dose values, 0.54 and 5.1 MGy. We recognize a small short-gate length effect.

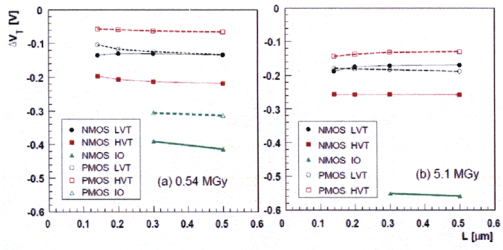


Fig. 11. Voltage shifts as a function of gate length L, compared at (a) 0.54 and (b) 5.1 MGy. W/L=2000. PMOS IO has no data at 5.1 MGy, since the voltage compliance is exceeded.

### *D. Back Gate Compensation*

Substantial threshold voltage shifts are inherent. In SOI devices, the voltage applied to the back side Vback affects the top gate transistor operation and may provide a possibility to recover the transistor performance. In fact, the irradiated Ids-Vgs characteristics is substantially different from the pre-irradiation at Vback = 0 but becomes almost identical if an appropriate Vback is applied. Figure 12 shows the optimum Vback as a function of the dose when the threshold of the irradiated transistor is compensated back to the pre-irradiation value. The data shown are for the transistors with the shortest gate lengths and body floating.

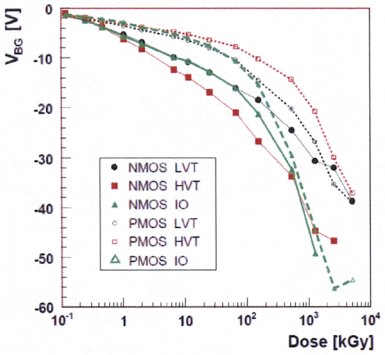


Fig. 12. Optimum Vback voltages for the transistors with shortest gate lengths to compensate the threshold voltage shifts.

The optimum backside voltages show a spread among different transistor types, and between NMOS and PMOS. However the LVT transistors show a smallest difference, which are preferred for the analog part of the circuit.

## VII. Summary

We have evaluated radiation resistance of monolithic pixel devices fabricated with OKI 0.15-μm FD-SOI process. The pixel devices and arrays of individual transistors were irradiated with 70-MeV protons and $^{60}$Co γ's to understand the effects and mechanism of radiation damage.

The pixel irradiated to $1.4\times10^{15}$ 1-MeV $n_{eq}/cm^2$ responded to laser light, although the electronics operation region is modified by irradiation. This result indicates that the n-bulk adopted in our SOI wafers is not inverted up to this fluence. Another sample irradiated to $1.3\times10^{16}$ 1-MeV $n_{eq}/cm^2$ did not transfer the reset signal, which is explained by a radiation induced large threshold shift in the IO transistors.

Detailed characterization was performed of the transistors with different threshold types and W/L ratios. The primary effect appears in the threshold voltage shift. The low threshold type transistors are suitable in view of radiation resistance, showing smallest deviations among NMOS and PMOS threshold shifts. Such shifts may be compensated by applying appropriate negative voltage to the backside.

The fabricated pixel devices utilized n-type silicon for the sensitive part and require positive voltages to the back to deplete. We have started investigating p-type silicon so that negative voltage to back compensates the threshold shifts. The optimum compensation voltages to the back are at most about 50 V for the dose range exceeding 1 MGy. Such a voltage should be applicable to the back, as the present devices can sustain up to 70 V even after irradiation.

## Acknowledgments

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