Radiation Resistance of SOI Pixel Devices Fabricated With OKI 0.15 μm FD-SOI Technology

Kazuhiko Hara, Mami Kochiyama, Ai Mochizuki, Tomoko Sega, Yasuo Arai, Koichi Fukuda, Hirokazu Hayashi, Minoru Hirose, Jiro Ida, Hirokazu Ikeda, Yoichi Ikegami, Yukiko Ikemoto, Yasuaki Kawai, Takashi Kohriki, Hirotaka Komatsubara, Hideki Miyake, Toshinobu Miyoshi, Morifumi Ohno, Masao Okihara, Susumu Terada, Toru Tsuboyama, and Yoshinobu Unno

***Abstract*—Silicon-on-insulator (SOI) technology is being investigated for monolithic pixel device fabrication. The SOI wafers by UNIBOND allow the silicon resistivity to be optimized separately for the electronics and detector parts. We have fabricated pixel detectors using fully depleted SOI (FD-SOI) technology provided by OKI Semiconductor Co. Ltd. The first pixel devices consisting of 32×32 matrix with 20 μm$\times$ 20 μm pixels were irradiated with ^{60}Co γ's up to 0.60 MGy and with 70-MeV protons up to 9.3×10^{15} p/cm^2. The performance characterization was made on the electronics part and as a photon detector from the response to reset signals and to laser. The electronics operation was affected by radiation-induced charge accumulation in the oxide layers. Detailed evaluation of the characteristics changes in the transistors was separately carried out using transistor test structures to which a wider range of irradiation, from 0.12 kGy to 5.1 MGy, was made with ^{60}Co γ's.**

***Index Terms*—FD-SOI, monolithic pixel, threshold shift.**

I. Introduction

MONOLITHIC pixel devices are an ultimate dream for physicists who require devices with large number of readout channels with fine segmentation though at small cost. In fact, in recent experiments, pixel-type particle detectors are required to be finely segmented and highly integrated to cope with high density particle flux generated in the luminous particle collisions. The pixel devices, such as for the Large Hadron Collider (LHC) experiments, are based on bump bonding of the detector elements to their readout electronics. This procedure is becoming delicate and costly with increasing number of channels. The device thickness remains also an issue in view of reducing the material to minimize the effects of multiple scatterings. Pixel devices utilizing UNIBOND™ [1] silicon-on-insulator (SOI) wafers can potentially solve such difficulties. Most important is that the silicon resistivity can be optimized separately for the readout electronics and SOI "handle wafer" which we adopt as the sensitive part. The original idea of SOI monolithic pixel can be found in [2]. Other SOI pixel devices were fabricated using non-commercial processes utilizing low resistivity SIMOX (Separation by implantation of oxygen) [3], [4] and low doping UNIBOND wafers [5]. We are developing pixel devices [6]–[9] using 0.15–0.20 μm fully depleted SOI (FD-SOI) CMOS processes commercially provided by OKI Semiconductor Co. Ltd. The first monolithic pixel device, named TOPPIX [6], was fabricated in 2006, composed of 32×32 matrix with 20 μm$\times$ 20 μm pixels.

Since the SOI silicon layer is substantially thin relative to bulk CMOS and the compact active area in the FD-SOI device is fully isolated by oxide, the device is less sensitive to ion strikes providing immunity to latch-up. On the other hand, the charge build-up in the buried oxide (BOX) layer and at the BOX interfaces is a significant issue for the total ionization dose (TID) effects in SOI devices [10]–[12]. The TID effects should present themselves as threshold voltage shifts and increase in the leakage current. We have irradiated TOPPIX devices with ^{60}Co γ's and 70 MeV protons. Transistor TEG (Test Element Group) chips, TrTEG [12], consisting of an array of PMOS and NMOS transistors with various W/L ratios were also irradiated to evaluate the TID effects in the basic transistor characteristics.

II. TOPPIX and TrTEG

Three types of transistors are available in the OKI 0.15 μm FD-SOI process: low threshold voltage transistors (LVT) and high threshold voltage transistors (HVT) for core circuits both with a 2.5 nm thick gate oxide layer, and I/O transistors (IO) with a 5.0 nm thick gate oxide layer. The main parameters are summarized in Table I. The SOI wafers were 150 mm in diameter and 650 μm in thickness, composed of Czochralski (CZ) grown 40 nm thick p-type SOI silicon of 18 Ωcm and n-type substrate of 700 Ωcm, separated by a 200 nm thick BOX layer. After the topside process was completed, the backside of the wafer was ground down mechanically to 350 μm thickness, and then plated with 200 nm of aluminum. Although the back contact is not ideal for implantation was not available, it provides

Manuscript received March 16, 2009; revised May 29, 2009. Current version published October 07, 2009. This work was supported by the KEK Detector Technology Development project.

K. Hara, M. Kochiyama, T. Sega, and H. Miyake are with the Graduate School of Pure and Applied Sciences, University of Tsukuba, Tsukuba, Ibaraki 305-8571, Japan (e-mail: hara@hep.px.tsukuba.ac.jp).

A. Mochizuki was with the Graduate School of Pure and Applied Sciences, University of Tsukuba, Tsukuba, Ibaraki 305-8571, Japan. She is now with Toshiba Company Ltd., Yokohama 247-8585, Japan.

Y. Arai, Y. Ikegami, Y. Ikemoto, T. Kohriki, T. Miyoshi, S. Terada, T. Tsuboyama, and Y. Unno are with IPNS, High Energy Accelerator Research Organization, KEK, Tsukuba, Ibaraki 305-0801, Japan.

K. Fukuda, H. Hayashi, J. Ida, Y. Kawai, and M. Ohno are with OKI Semiconductor Company Ltd., Hachioji, Tokyo 193-8550, Japan.

M. Hirose is with Osaka University, Graduate School of Science, Toyonaka, Osaka 560-0043, Japan.

H. Ikeda is with ISAS, Japan Aerospace Exploration Agency, Kanagawa 229-8510, Japan.

H. Komatsubara and M. Okihara are with OKI Semiconductor Miyagi Company Ltd., Ohira, Miyagi 981-3693, Japan.

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Digital Object Identifier 10.1109/TNS.2009.2028573

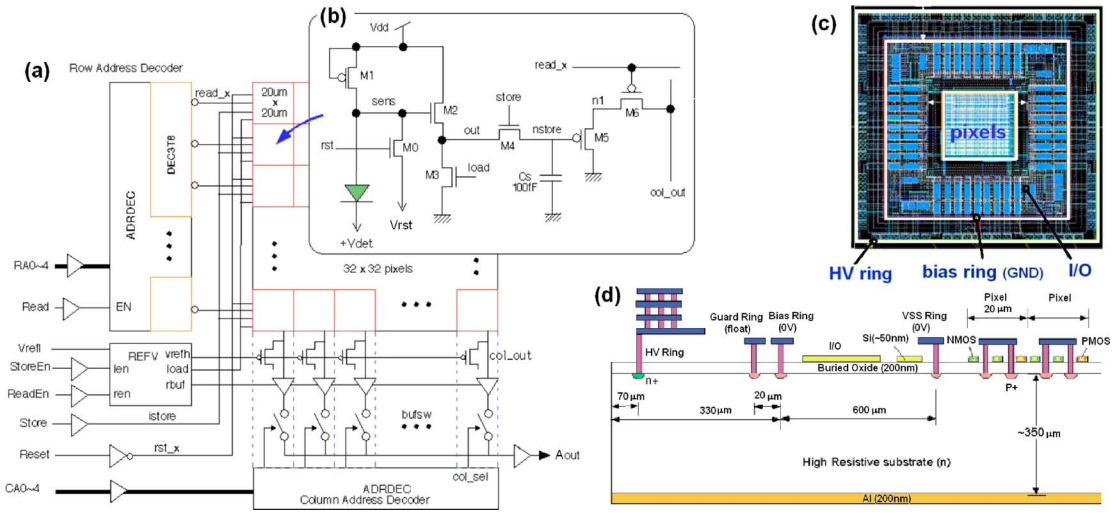


Fig. 1. TOPPIX chip. (a) Block diagram of readout electronics. (b) Readout of one pixel. (c) Top view of the overall chip. (d) Cross-sectional view of the edge region.

TABLE I
TRANSISTOR PARAMETERS AVAILABLE IN OKI 0.15 μm PROCESS

Transistor type	LVT	HVT	IO
Gate oxide thickness (nm)	2.5	2.5	5.0
Typ. threshold voltage (V)	0.2	0.4	0.5
Voltage tolerance (V)	1.0	1.0	1.8
Minimum gate length (∞m)	0.14	0.14	0.30

TABLE II
16 TRTEG TRANSISTORS SHOWING TYPES, W/L SIZES (IN MICRONS) AND BODY CONTROLS, (F) FLOATING OR (BT) BODY TIE

W/L	280/0 .14	400/0.20	600/0.30	1000/0.50
LVT	F, BT	BT	F, BT	BT
HVT	F, BT	BT	F, BT	BT
IO			F, BT	F, BT

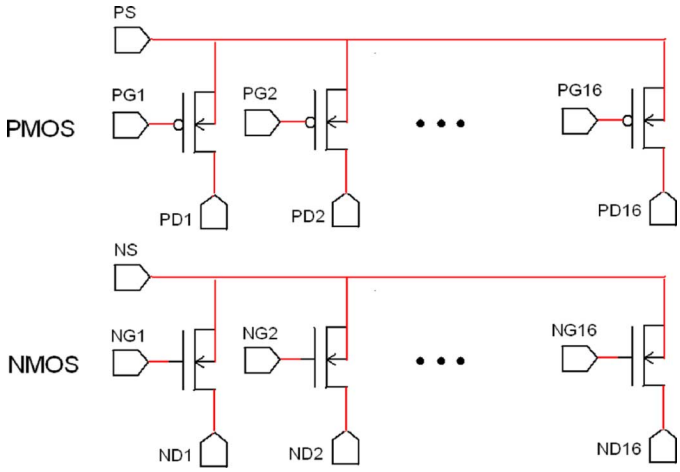


Fig. 2. TrTEG circuit for 16 NMOS and 16 PMOS transistors.

the possibility of biasing from the backside. There are two types of body control, body floating and body tie, for the transistors. In the body-tied configuration, the body contact is connected with the source contact at regular intervals externally at one of the metal layers on top of the SOI transistors. In the OKI process, there are five metal and one poly-silicon layers available.

The TOPPIX chip is 2.4 mm square in overall size. The block diagram is shown in Fig. 1(a). The analog readout chain for a pixel, Fig. 1(b), consists of eight HVT body-tied FETs, one functioning as input protection diode. The analog signal Aout selected by row and column addresses was recorded by a digital oscilloscope. The reset voltage Vrst was provided externally, which allowed us to examine the response of individual pixel readout by varying Vrst. "Vrst response" refers to this test in this paper. Reset (rst), row/column selections, and other commands were provided by IO transistors located surrounding the pixels at center, see Fig. 1(c). The entire electronics part was surrounded by bias and guard rings, both having p^+ implants underneath. The schematic view of the edge region is shown in Fig. 1(d). The bias ring was set to ground and the guard floating. In the edge region, a HV ring with n^+ implant was located allowing to bias from the topside to the n substrate. The backside contact was also used for detector biasing. We refer to the former biasing as Vdet and the latter as V_{back}.

The TrTEG chip consists of 16 NMOS and 16 PMOS transistors. With fixing the W/L ratio to 2000, we chose two to four length combinations for the three transistor types. The selected 16 parameters are listed in Table II. As shown in Fig. 2, the individual transistor characteristics can be tested by selecting the corresponding drain and source terminal pair while the source terminal is common. The back of the TrTEG chip is also aluminized providing the possibility to bias (V_{back}) to the substrate.

III. IRRADIATION

The irradiation with ^{60}Co γ's was performed at Takasaki Institute of Japan Atomic Energy Agency. Three TOPPIX chips were irradiated up to 0.12 kGy to 0.60 MGy at 1-5 kGy/h. The irradiation was interrupted by characterization measurements to obtain the data at six accumulated dose values in total. The TrTEG chips were irradiated each to 0.01 kGy to 5.1 MGy at

0.2-20 kGy/h, where the characterization was made after the irradiation was completed. Alanine rod dosimeters Aminogray™, available from Hitachi Cable, Ltd., were attached to several samples to examine the dose calibration provided by the irradiation facility. The absorbed dose was derived from the yield of radiation induced stable radicals in alanine, which was measured using ESR spectroscopy. The measured values agreed with the doses provided by the facility to 10%. During the exposure, the samples were kept at room temperature. All the readout terminals were shorted using conductive sponge while they were not grounded. This condition is not necessarily the worst case. Measurements in different bias conditions are to be performed in further study.

The proton irradiation was carried out at Cyclotron and Radioisotope Center (CYRIC), Tohoku University. Details of irradiation and fluence calibration are described elsewhere [11]. The fluence target was taken from the radiation level at the super LHC, where 1-MeV neutron equivalent fluence is evaluated to 10^{16} n/cm^2 at the pixel detector. Two TOPPIX chips were irradiated each to 1.0×10^{15} p/cm^2 and 9.3×10^{15} p/cm^2, where the irradiation time was 21 min. and 105 min., respectively. All the terminals were shorted like in the γ irradiation. The temperature was kept at -10°C during the irradiation to suppress unnecessary evolution of the bulk damage [13].

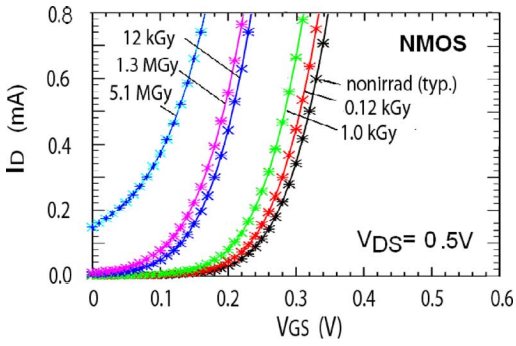
Taking the NIEL (non-ionizing energy losses) factor [14] of 1.5 for 70 MeV protons in Si, the two proton fluence values corresponded to 1.5×10^{15} and 1.4×10^{16} 1-MeV n_{eq}/cm^2. In comparing the TID by 70-MeV protons with ^{60}Co γ's, the absorbed dose to SiO_2 is 6.0 MGy (SiO_2) for the proton fluence of 1×10^{16} p/cm^2, which was calculated using a GEANT4 program [15].

IV. TrTEG Results

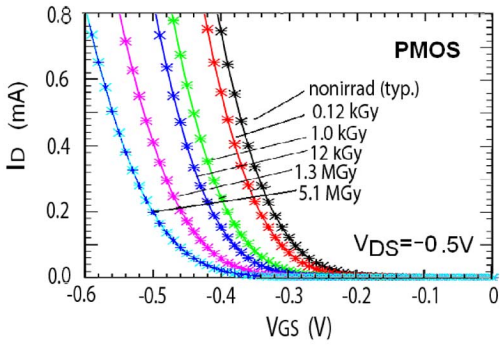
Radiation effects in individual transistor were evaluated with the TrTEG chips. We measured the drain current as a function of the gate-source voltage V_{GS} with fixing the drain-source voltage V_{DS} at 0.5 V for NMOS and -0.5 V for PMOS transistors. Fig. 3 shows a typical set of I_D-V_{GS} curves from γ irradiation, where the backside voltage V_{back} was set to 0. The radiation effects in TrTEG were first evaluated with protons [11], where we incorporated switch circuits to select one of the transistors in TrTEG matrix. Since it turned out the switches were also influenced by radiation, we repeated proton irradiation [12] for simplified TrTEG circuits, shown in Fig. 2. Main results from the proton irradiation are shown in the following in comparison with ^{60}Co γ irradiation results.

A. Leakage Current

Fig. 4 shows the leakage current defined as I_D at $V_{GS}=0$ for the transistors with the shortest gate lengths (W/L = 280/0.14 for LVT and HVT, W/L = 600/0.30 for IO, see Table II). The data are for γ irradiation. As the threshold voltage shifts negatively to compensate the positive charges trapped in the gate oxide, the leakage current increases with dose for NMOS. The effect is opposite for PMOS resulting that the dose dependence is small.

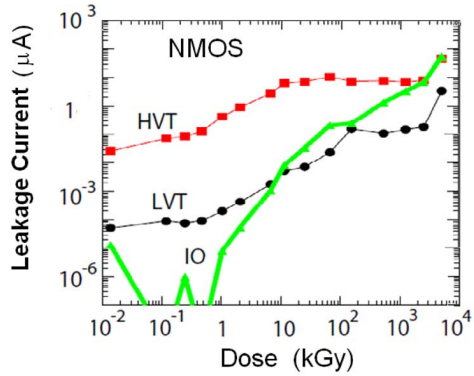


(a)



(b)

Fig. 3. I_D-V_{GS} curves of γ irradiated and typical non-irradiated TrTEG (LVT, W/L = 280/0.14, Body floating) samples, (a) NMOS and (b) PMOS.



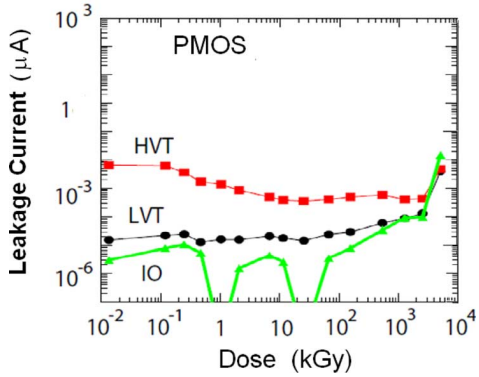


Fig. 4. Leakage current I_D defined at $V_{GS}=0$ as a function of dose (γ irradiation), shown for three transistor types with the shortest gate lengths. The uncertainty dominates the measured values below 10^{-6} μA.

B. Threshold Voltage Shift

According to the studies for bulk CMOS devices [16], the radiation induced threshold voltage shift is explained by interplay of holes trapped in the gate oxide and the charges created at the

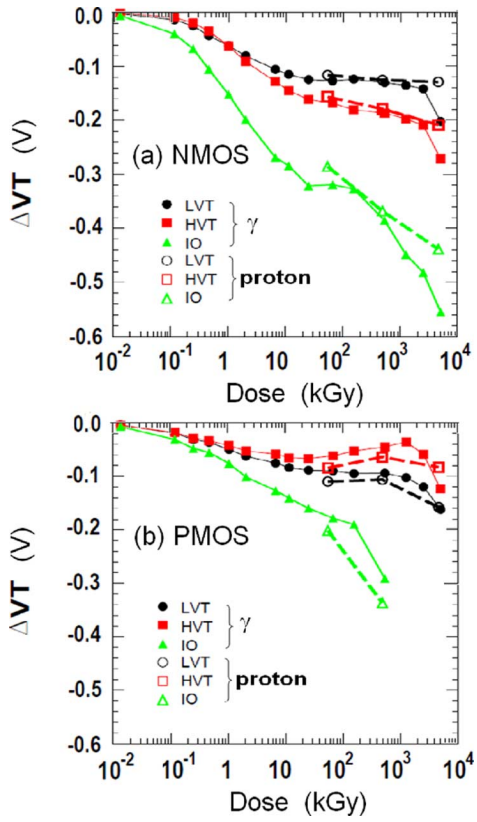


Fig. 5. Dose dependence of the transistor threshold voltage shifts. The transistors are with the smallest gate length and body floating (see Table II). Filled (open) marks are the data obtained from γ (proton) irradiation.

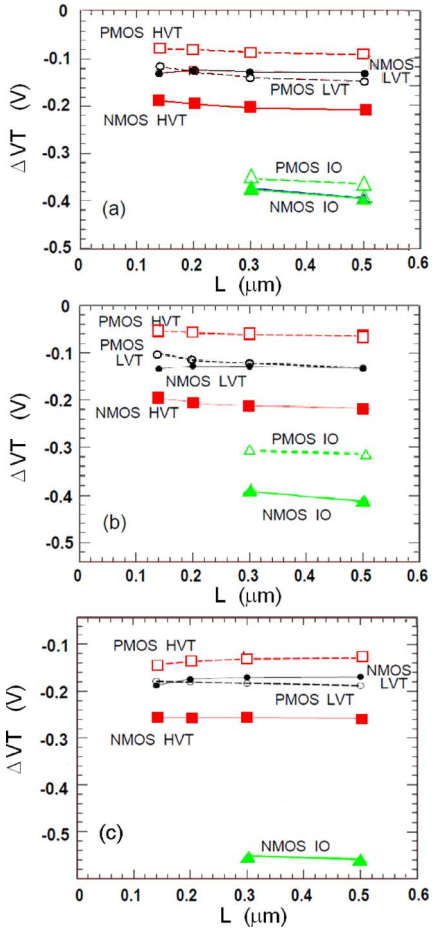


Fig. 6. Voltage shifts as a function of gate length L, compared among (a) 0.25 MGy (proton), (b) 0.54 MGy (γ) and (c) 5.1 MGy (γ) irradiated samples. W/L ratio is fixed to 2000. PMOS IO has no data at 5.1 MGy for exceeded voltage compliance.

oxide-silicon interface. The charge state of interface traps is negative at the p-type silicon to oxide interface (NMOS) and positive at n-type (PMOS). The contributions from the BOX layer need to be considered in addition for the SOI devices, especially for FD-SOI, where the larger coupling should make the transistors much sensitive to the BOX charge trapping [12]. The hole trapping and interface charge creation should also be affected by device processing and wafer quality. Therefore it is of prime importance to evaluate the effects in the devices from the same process we are employing.

Fig. 5 shows the radiation induced shifts of the threshold voltage $\mathrm{V_T}$, $\mathrm{V_T}$ defined as $\mathrm{V_{GS}}$ where $\mathrm{I_D} = 0.5\ \mathrm{mA}$. The data are for the transistors with the shortest gate lengths and body-floating. Since the holes are the main contributor, the shifts are negative for both PMOS and NMOS. The data obtained from the proton irradiation are compared. The two sets of data are in reasonable agreement. The shifts are different among LVT, HVT and IO, being largest for IO transistors which have thicker gate oxide. The positive charges in the gate oxide are considered to act as the primary contributor for the threshold shifts.

For bulk CMOS, the standard behavior of NMOS FETs is that the threshold voltages keeps decreasing up to a certain dose value, whereas for higher doses it exhibits a rebound due to the effect of interface states. This may lead to a positive threshold shift. The present data, especially for HVT and IO, show an opposite tendency. The difference should be attributed to the charge creation at the BOX interface. This contribution should be larger in FD-SOI and numerical evaluation to breakdown the contribution is underway.

The body tie effects are expected to be not substantial in FD-SOI. The measured shifts are typically larger in magnitude by 10 mV at most for body tied samples than body floating. The difference is smaller at lower doses.

C. Gate Length Dependence

The threshold shifts are plotted in Fig. 6 as a function of gate length. The graphs are given for two dose values, 0.54 and 5.1 MGy by γ irradiation in comparison with $4.1 \times 10^{14}\ \mathrm{p/cm^2}$ irradiation, corresponding to 0.25 MGy. We recognize small short-gate length effects both for γ and proton irradiations.

D. Back Gate Compensation

Substantial threshold voltage shifts are inherent. In SOI devices, the voltage applied to the backside, $\mathrm{V_{back}}$, affects also the top gate transistor operation and may provide a possibility to recover the transistor performance. In fact, the irradiated $\mathrm{I_D}$-$\mathrm{V_{GS}}$ characteristics at $\mathrm{V_{back}} = 0$ is substantially different from the non-irradiated sample at $\mathrm{V_{back}} = 0$ (see Fig. 3) but became similar if an appropriate $\mathrm{V_{back}}$ was applied. Fig. 7 shows the $\mathrm{V_{back}}$ value as a function of the γ dose where the threshold voltage of

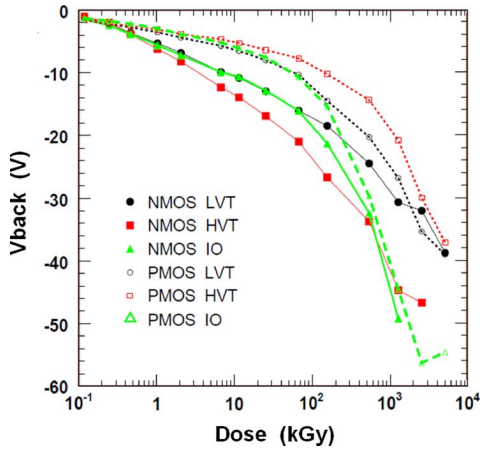


Fig. 7. The voltage to the backside Vback where the threshold voltage is compensated back to the non-irradiated value with $\mathrm{Vback} = 0$. The transistors are γ irradiated samples with the shortest gate lengths.

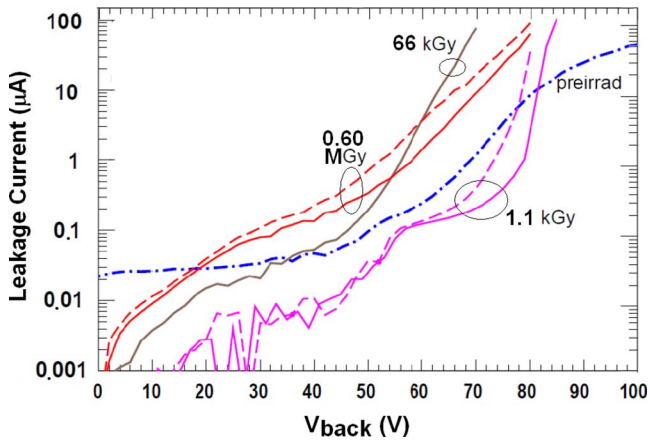


Fig. 8. Leakage current of TOPPIX chip3 as a function of the detector bias on the backside, Vback. The data taken right (20 min.) after the irradiation (at 60°C) are shown in dashed (solid) curves.

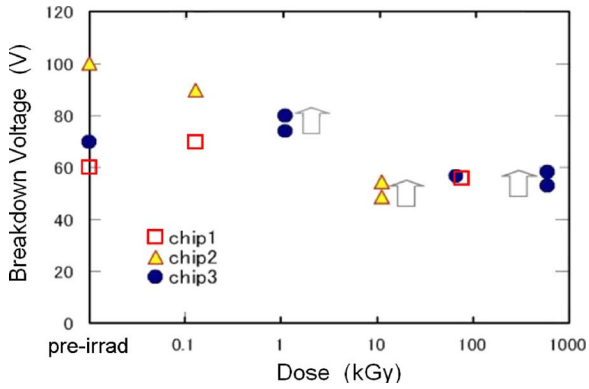


Fig. 9. Breakdown voltages of three TOPPIX chips as a function of dose. The two same marks at the same dose points are the data before and after annealing with the arrows showing the chronological order.

the irradiated transistor was compensated back to the non-irradiation value measured at $\mathrm{V_{back}} = 0$. The data shown are for the transistors with the shortest gate lengths and body floating. The compensation backside voltages are negative and show a spread among different transistor types, and between NMOS and PMOS. Difference between the LVT transistors is smallest. The implication to the pixel device is discussed in the TOPPIX irradiation results, described in the following.

V. TOPPIX γ-Irradiation Results

The primary goal of the TOPPIX irradiation was to examine the functionality of the electronics part and of TOPPIX as a photon detector. The Vrst response, I-V characteristics, and response to laser were measured for this purpose. Among these, the laser test was made after completion of irradiation, while the other two were measured between irradiations as well. It is reported [13] that the damages to silicon bulk by hadrons, which are dependent on the irradiation fluence, rate and others, evolve with post-irradiation time depending on temperature, and that annealing at 60°C for 80 min. provides consistent damage results irrespectively of various irradiation rates. Since the γ irradiation damages are primarily in the insulator, the same procedure may not be applicable as for the bulk. We however adopted the annealing procedure in order to compare with the proton irradiation results. In practice we found small differences in the threshold voltage shifts before and after the annealing. For the measurements between irradiations, we shortened the time to 20 min and examined the differences from the results obtained right after the irradiation.

A. I-V *Characteristics*

Fig. 8 shows the I-V characteristics of the TOPPIX chip irradiated up to 0.60 MGy. The leakage current refers to the total detector current when the reverse bias ($\mathrm{V_{back}}$) was applied to the detector back with the bias ring grounded, measured at room temperature. Plotted are the data taken after dose accumulation of 1.1 kGy, 66 kGy, and 0.60 MGy, and before irradiation. For the two dose points, I-V curves measured immediately after the irradiation are also plotted to compare with the data taken after 20 min. of annealing. The leakage current at biases below 50 V tends to decrease with radiation. This can be explained by the PMOS transistor threshold shifts, described previously, suggesting that the leakage current through the pixels only decreases with the dose.

The breakdown voltages, defined as the bias where the leakage current exceeded 1 μA, are summarized in Fig. 9 for all the three chips. The annealing contribution is moderate as the breakdown voltage increased by approximately 5 V only. Although the individual difference may exist, the breakdown voltage tends to decrease with the dose.

Abrupt leakage current increases are often caused by avalanche multiplication due to local high electric field. We can localize such points, "hot spots", by detecting associated infrared lights with a cooled infrared sensitive CCD camera [17], as images are given later for the proton irradiated samples. We identified that the breakdown is located at the corners of the bias ring both for pre and post irradiated samples. The electric field is largest at the corners of the bias ring which is p-implanted against the n-bulk. The dose dependent increase in I-V curves in the bias region $\mathrm{V_{back}} < 50$ V could be attributed to the holes trapped in the BOX generating additional field lines to the bias ring and hence decreasing the breakdown voltage.

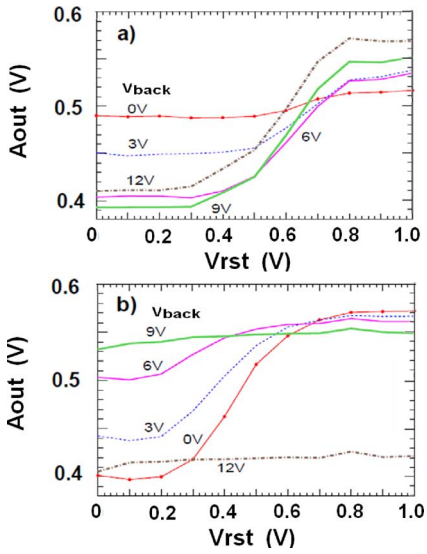


Fig. 10. TOPPIX output voltage Aout averaged over 1024 channels as a function of Vrst (a) before and (b) after 0.60 MGy irradiation. The curves are shown for selected Vback settings up to 12 V.

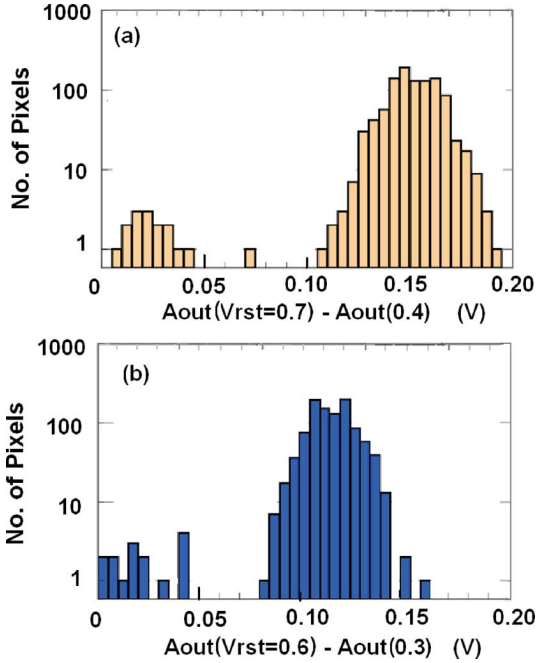


Fig. 11. TOPPIX output voltage Aout differences for two Vrst values, (a) before irradiation measured at $V_{back} = 9$ V and (b) after 0.60 MGy irradiation measured at $V_{back} = 0$.

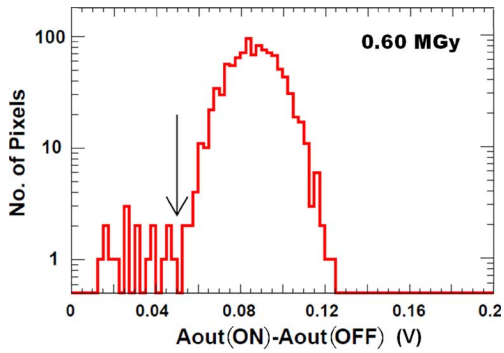


Fig. 12. Response differences with laser ON and OFF for TOPPIX irradiated to 0.6 MGy. The bias was 1 V.

The leakage current becomes moderate for $V_{back} > 50$ V at 0.60 MGy. Different contribution should be in effect at this dose, such as electrons attracted to the holes which weaken the overall electric field around the bias ring become more effective. We are carrying out TCAD simulation to understand the mechanisms involved.

B. Vrst *Response*

The Vrst response was measured for a Vrst range from 0 to 1 V at a 0.1 V step, with changing the bias V_{back} up to 20 V at a step of 1 V. The electronics working range is influenced by the bias since the backside voltage couples to the electronics via BOX layer, known as a back-gate effect [6].

Fig. 10 shows the Vrst response of chip 3 before and after 0.60 MGy irradiation. The output voltage Aout should increase linearly with Vrst in the working region. Although modified by irradiation, there remain conditions where the electronics is functioning. The tendency is that the working region is shifted to lower biases with irradiation. This is explained by threshold voltage shifts of the amplifier transistors. To numerate the functionality of individual pixel channels, we chose the ranges of Vrst (0.4:0.7 V) at $V_{back} = 9$ V and (0.3:0.6 V) at $V_{back} = 0$ for the data before and after 0.60 MGy irradiation, respectively, where the two values in parentheses are the two reference Vrst values to calculate the amplifier response.

The distribution of Aout differences for two Vrst values is plotted in Fig. 11, showing a clear separation of sick pixels to genuine ones. The Gaussian distributions populated down to 0.11 V before and to 0.08 V after 0.60 MGy irradiation for genuine pixels while sick pixels located below 0.05 V typically. The number identified as dead was 16 pixels both before and after irradiation with their location unchanged. We conclude that no dead channel was created up to 0.60 MGy.

Note that the fraction of dead pixels has been significantly improved to a 0.1% level in the 2007 production.

C. *Laser Response*

We injected continuous 670 nm laser over the entire TOPPIX device face. The output voltage differences between laser on and off are shown in Fig. 12 for the sample irradiated to 0.60 MGy. The V_{back} was set to 1 V. The 16 abnormal channels found in the Vrst response measurement are clustered in the low response group below the arrow. Additionally one channel was found dead near the arrow. This channel was leaky giving a large OFF signal and could not be detected in the Vrst response measurement. We conclude that no defective pixel was created by irradiation.

VI. TOPPIX Proton Irradiation Results

Two TOPPIX chips were irradiated with 70-MeV protons up to 9.3×10^{15} p/cm^2 to investigate the radiation effects mainly to the substrate. The electronics damage is also to be compared between 70-MeV protons and ^{60}Co γ's.

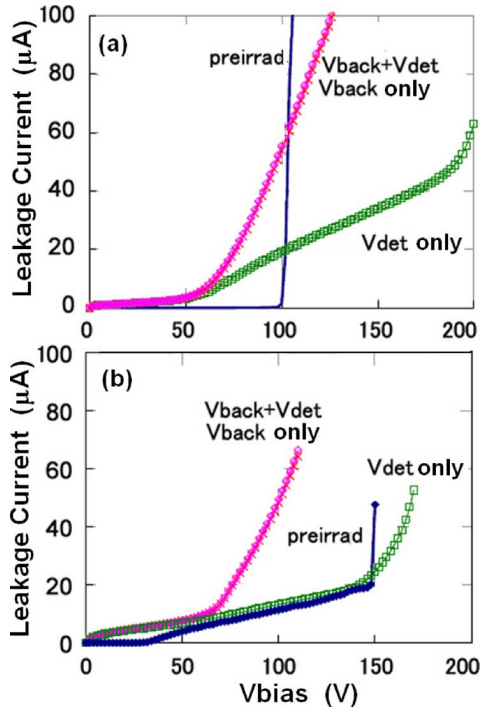


Fig. 13. I-V curves of TOPPIX samples irradiated to (a) 1.0×10^{15} p/cm^2 and (b) 9.3×10^{15} p/cm^2, overlaid with pre-irradiation curves. The data are shown for biasing from the HV ring (Vdet) and from the backside (V_{back}). The curves biased by both Vdet and V_{back}, and Vback only are overlapped each other.

A. I-V *Characteristics*

Fig. 13 plots the I-V curves for the two samples. The curves measured at pre-irradiation were identical irrespective whether the bias was fed through the HV ring (Vdet) in front or from the backside (V_{back}). However, a dependence on biasing is observed for the irradiated samples as plotted in the figure. The leakage current is lower if the sensor is biased from the HV ring (Vdet only in the figure).

The I-V should be a result of various mechanisms involved in generating excess leakage current, which could eventually be characterized by detecting hot locations with the CCD camera. For the sample irradiated to 1.0×10^{15} p/cm^2, hot spots were observed at the corners of the bias ring (see Fig. 14(a)) on the steeper I-V_{back} section (at 100 V) and on the second steepest I-Vdet section (at 170 V). On the steepest I-Vdet sections (at 210 V), the spots were observed around the HV ring (see Fig. 14(b)) in addition. Note that pre-irradiation samples exhibited hot spots always at the corners of the bias ring, as described previously. The observation that the electric field is maximum around the bias ring (p^+ implanted) should lead to a conclusion that the n-bulk is not inverted up to this fluence. This is also supported from the laser response described below.

The 9.3×10^{15} p/cm^2 sample had a leakage current increase in the bias range from 40 and 150 V since pre-irradiation[1]. The hot spots could not be identified in this bias range both before and after irradiation when the bias was fed through Vdet. This is probably because infrared emission is not localized or weak

[1]The individual performance difference existed in this first production samples. The uniformity has been improved in the following productions.

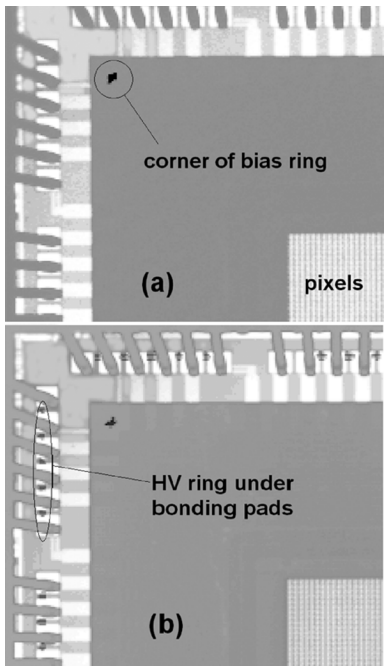


Fig. 14. Hot spot images of the sample irradiated to 1.0×10^{15} p/cm^2. (a) At Vdet = 170 V the corners of the bias ring are hot. (b) At Vdet = 210 V, the HV ring are hot in addition. Since the infrared lights are absorbed by aluminum bonding pads, the HV ring is visible as dots.

points are located outside the range of vision. At 170 V of Vdet or 100 V of V_{back}, hot spots were seen at the bias ring corners and HV rings, similar to Fig. 14(b). Although no laser response was seen for this sample due to the damages in the electronics part, the bulk seems to stay un-inverted, judging from the forward bias I-V behavior in the negative voltage side.

It is reported that n-type CZ wafers do not type invert up to proton fluence of 3.4×10^{15} 1-MeV n_{eq}/cm^2 [18], whereas n-type FZ wafers are known to invert to p-type [19] after a few $\times10^{13}$/cm^2. Since we adopt CZ wafers, the present observation is consistent with [18], extending the un-inverted range up to 9.3×10^{15} p/cm^2 (1.4×10^{16} 1-MeV n_{eq}/cm^2).

B. Vrst *Response*

Similar to the case of the γ irradiation, the Vrst response is degraded by proton irradiation. Fig. 15 shows the Vrst response for selected bias (V_{back}) values. The electronics working region became narrow at 1.0×10^{15} p/cm^2, and disappeared at 9.3×10^{15} p/cm^2. The reset (rst) is not properly transferred due to the damages in the IO transistors. As we have observed (Fig. 6), the threshold shift is largest for IO transistors.

C. *Laser Response*

The TOPPIX irradiated to 1.0×10^{15} p/cm^2 was examined for the laser response. Fig. 16 shows the response of three consecutive pixel signals to laser ON and OFF, where the readout channels were switched every 64 μs. The Aout signal shape is characterized by showing the constant output corresponding to the application of the reset voltage, followed by accumulation of charge. The measurement was made at room temperature at

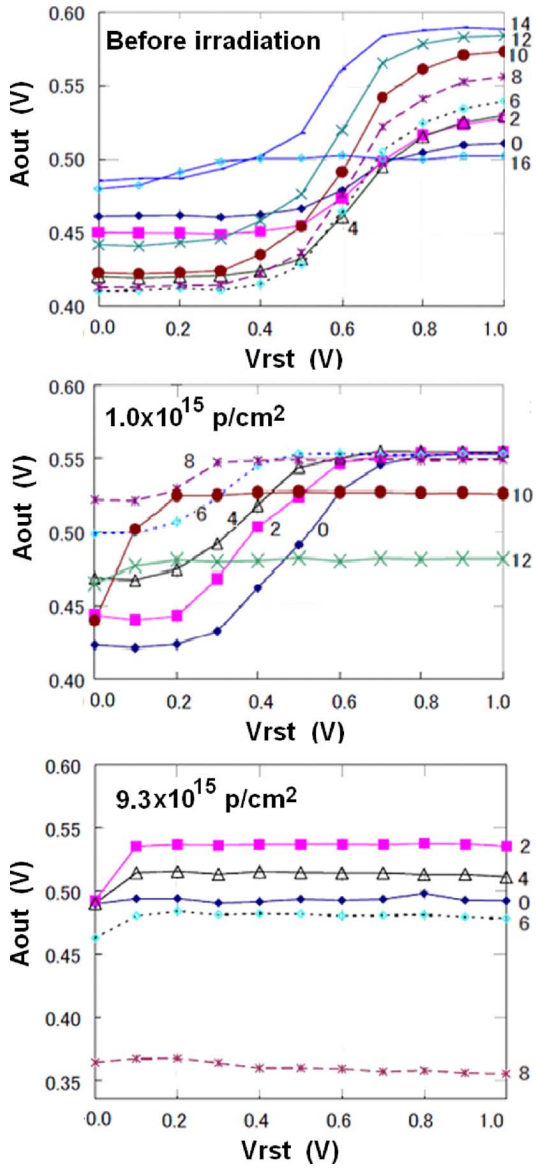


Fig. 15. Vrst response of TOPPIX before irradiation and for two proton-irradiated samples. The numbers attached to the curves are V_{back} values.

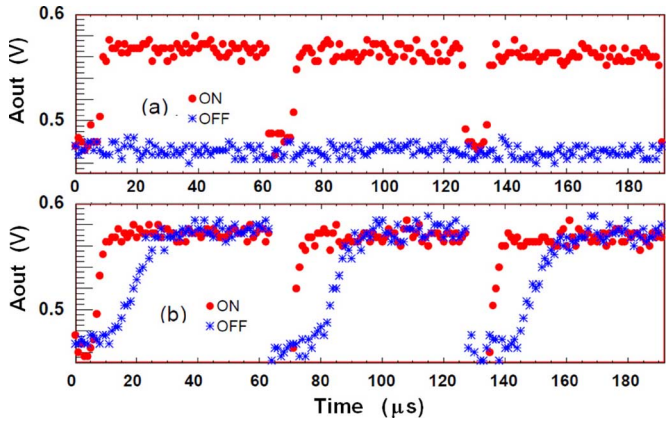


Fig. 16. Response to laser ON (circles) and OFF (stars) for (a) pre-irradiation and (b) after 1.0×10^{15} p/cm^2 with 2 V bias.

$V_{back} = 2$ V. The irradiated sample exhibited substantial contributions from the leakage current, but the response to laser was obviously seen. A mask pattern was properly reproduced.

The dead channels were evaluated by laser injection while the chip was cooled to 11°C to reduce the noise contribution. There was no new dead channel created.

VII. Summary

We have evaluated radiation resistance of monolithic pixel devices fabricated with OKI 0.15-μm FD-SOI process. The pixel devices and arrays of individual transistors were irradiated with 70-MeV protons and ^{60}Co γ's to understand the effects and mechanism of radiation damage.

A detailed characterization was performed for transistors with different thresholds and W/L ratios. The primary effect appears in the threshold voltage shift. The shifts may be compensated by applying appropriate negative voltage to the backside.

The pixel irradiated to 1.0×10^{15} p/cm^2 responded to laser light, although the electronics operation region was modified by irradiation. Another sample irradiated to 9.3×10^{15} p/cm^2 did not transfer the reset signal, which is explained by a radiation induced large threshold shift in the IO transistors. The present results indicate that the n-bulk adopted in our SOI wafers is not inverted up to this fluence.

Although the TOPPIX has been proven to work as photon detector up to 1.0×10^{15} p/cm^2, the degraded Vrst response due to transistor threshold shifts is a significant issue for application of the device to higher fluence and also to detect charged particles. The following three items are in the list of our R&D. (1) High resistivity p-type silicon for the substrate. The n-type silicon requiring positive backside voltage to deplete worsens the threshold shifts due to back gate effects. Since the shifts can be compensated by negative V_{back} voltages, p-type substrates should behave better. (2) Buried p-well underneath the BOX layer. The back gate effects should be minimized by adding an electrode underneath the BOX layer. (3) 3D electronics fabrication to separate the substrates for the detector and electronics.

Acknowledgment

The authors acknowledge Dr. R. Yamagata of JAEA Takasaki for performing ^{60}Co irradiation. Professors T. Shinozuka and T. Wakui, and the team of CYRIC are also acknowledged for much help and conducting excellent proton irradiation.

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